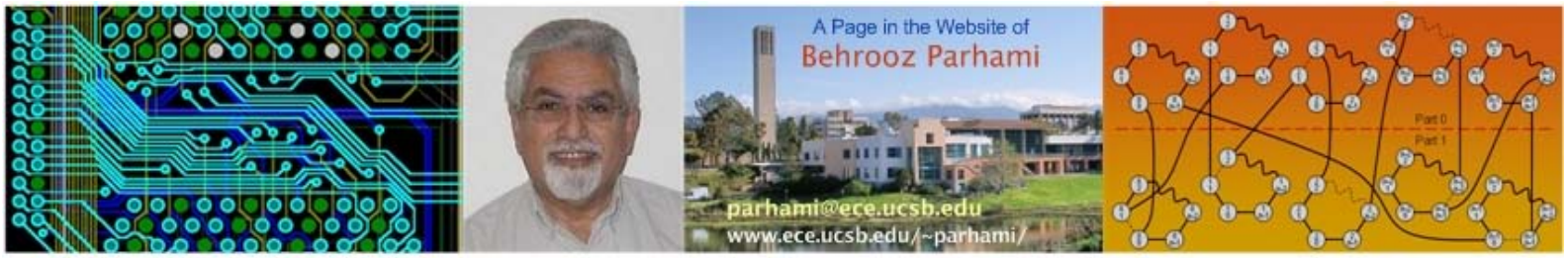


Behrooz Parhami's ECE 252B Course Page for Spring 2010

Computer Arithmetic

Enrollment code: 11601
Prerequisite: ECE 152A and ECE 152B (or equivalents)
Class meetings: TR 12:00-1:30, Arts 1251
Instructor: Professor Behrooz Parhami
Open office hours: M 11:00-12:30, R 5:00-6:30, HFH 5155
Course announcements: Listed in reverse chronological order
Course calendar: Schedule of lectures, homework, and exams
Homework assignments: Four assignments, worth a total of 20%
Exams: Closed-book midterm, worth 30%
Research paper: Report and short oral presentation, worth 50%
Research paper guidlines: Brief guide to format and contents
Poster presentation tips: Brief guide to format and structure
Grade statistics: Range, mean, etc. for homework and exam grades
References: Textbook and other sources (**Textbook's web page**)
Lecture slides: Available on the textbook's web page
Miscellaneous information: Motivation, catalog entry, history

Course Announcements

2010/06/15: The spring 2010 offering of ECE 252B is now officially over. Grades have been reported to the Registrar's office and feedback on each student's research paper and poster presentation has been sent via e-mail. The list of research topics has been updated to reflect the final topic choices and paper titles. Have a pleasant summer!
2010/05/26: A brief guide for preparing your research poster has been added in a separate section below (there is a link to it in the table of contents above).
2010/05/18: Homework 4 has been posted below. It will be due on T 6/1.
2010/05/17: The latest updates to lecture slides for Parts IV and V of the textbook (division and real arithmetic) have been posted to the textbook's Web page.
2010/05/07: Homework 3 has been posted below. A minor update to the lecture slides for Part IV of the textbook (addition of one slide showing convergence of the partial quotient to *q* in restoring and norestoring division, immediately after Fig. 13.8) has also been posted to the textbook's Web page.
2010/05/04: The solution supplied for part c of Problem 12.19 was a duplicate of the part b soltuion. The correct solution is given below, in the "Homework Assignments" section. Also, grade stats for HW2 and midterm exam have been posted. An e-mail message has been sent to four students with overdue preliminary list of research references. They should contact the instructor ASAP.
2010/04/29: Our miderm exam on Tuesday 5/4 will be closed book. The use of a simple calculator (not pocket PC) is allowed. For three of the four doubly assigned research topics, I have not yet heard back from you regarding how you will divide the work so that there is minimal overlap between the two research papers. Please inform me by Monday, 5/3. For the fourth such topic, I have added a comment about how the work is to be divided.
2010/04/19: Homework 2 has been posted below. Research topics have been assigned. In most cases, I was able to honor your first or second perference. However, because a large number of your choices were concentrated in a few of the topics, with the most popular topic chosen by 8 students, I was forced to assign 2 students to each of the topics 3, 13, 15, 16. Ideally, I would like one of each pair of students above to switch to one of the unselected and unassigned topics (1, 8, 10, 14). Please see me about this, and bring along a list of the four unassigned topics in order of your preference. Alternatively, we can leave some topics with 2 assinged students, provided we can meet together to agree on a course of research that would minimize the overlap. For

Blog & books
Favorite quotations
Poetry
Pet peeve
Virtual retirement
CE Program
ECE Department
UCSB Engineering
UC Santa Barbara

example, different aspects of the topic can be emphasized by each student. The 8 students with duplicate assignments should see me ASAP.

2010/04/13: Presentation slides for Part III of the textbook have been updated. Research topics are now available for discussion and selection. Please e-mail me your first, second, and third choices by F 4/16. We will then finalize the topic assignments by T 4/20.

2010/04/04: Homework 1 has been posted below. Presentation slides for Parts I and II of the textbook have been updated for spring 2010.

2010/03/19: Welcome to the ECE 252B web page for spring 2010. The course textbook is available at the campus bookstore. Please make sure that you get the 2nd (2010) edition of the textbook, as it is significantly different from the 1st (2000) edition. Also, bear in mind that you can usually get a much better price from on-line sources. Those planning to audit the class should see me before or at the start of the first lecture on Tuesday 2010/03/30.

Course Calendar

Course lectures, homework assignments, exams, and research milestones have been scheduled as follows. This schedule will be strictly observed. Please review the first two chapters in the textbook (before the first class, if possible). These chapters contain material that you should already know. PowerPoint and pdf files of course lectures, including the skipped material in Chapters 1-2, can be found on the **textbook's web page**.

Day & Date (book chapters) Lecture/discussion topic [Homework posted/due] {Special notes}

T 03/30 (ch. 3-4) Redundant and residue representations {Introductory survey}
R 04/01 (ch. 5) Basic addition and counting

T 04/06 (ch. 6) Carry-lookahead adders [HW1 posted, ch. 1-8]
R 04/08 (ch. 7) Variations in fast adders

T 04/13 (ch. 8) Multioperand addition {Research topic defined}
R 04/15 (ch. 9) Basic multiplication schemes [HW1 due]

T 04/20 (ch. 10) High-radix multipliers [HW2 posted, ch. 9-12]
R 4/22 (ch. 11) Tree and array multipliers

T 04/27 (ch. 12) Variations in multipliers {Preliminary research references due}
R 04/29 (ch. 13) Basic division schemes [HW2 due]

T 05/04 (ch. 1-12) Midterm exam, closed book, 12:00-2:00 {Note the extended time}
R 05/06 (ch. 14) High-radix division

T 05/11 (ch. 15) Variations in dividers [HW3 posted, ch. 13-16]
R 05/13 (ch. 16) Division by convergence

T 05/18 (ch. 17-18) Floating-point numbers and operations {Research title and references due}
R 05/20 (ch. 19-20) Errors, precision, and certifiability [HW3 due] [HW4 posted, ch. 17-22]

T 05/25 (ch. 21) Square-rooting methods
R 05/27 (ch. 22) CORDIC algorithms {Research paper abstract and outline due}

T 06/01 (ch. 23-24) Other topics in function evaluation [HW4 due] {Instructor/course evaluation survey}
R 06/03 Research poster presentations

R 06/10 {Final research paper due by midnight}

W 06/16 {Course grades to be submitted by midnight}

Homework Assignments

-Turn in solutions in class before the lecture begins.
-Because solutions will be handed out on the due date, no extension can be granted.

-Use a cover page that includes your name, course name, and assignment number.
-Staple the sheets and write your name on top of each sheet in case they are separated.
-Although some cooperation is permitted, direct copying will have severe consequences

Homework 1: Number systems and addition (ch. 1-8, due R 2009/04/15, 12:00 noon)
Do the following problems from the textbook: 3.12, 5.2, 6.14, 7.5, 8.18

Homework 2: Multiplication (ch. 9-12, due R 2009/04/29, 12:00 noon)
Do the following problems from the textbook: 9.14abc, 9.20, 10.14, 10.18, 11.6, 12.19
Solution to Problem 12.19c: After applying three 4-by-4 multipliers, the least-significant 4 bits of the 16-bit product are at hand. Forming the remaining 12 bits requires a 12-bit adder, which can be built of three 4-bit adders.

Homework 3: Division (ch. 13-16, due R 2009/05/20, 12:00 noon)
Do the following problems from the textbook: 13.6b, 13.12ab, 14.10, 15.13, 16.13

Homework 4: Floating-point and function evaluation (ch. 17-22, due T 2009/06/01, 12:00 noon)
Do the following problems from the textbook: 17.4, 18.6bc, 19.7, 20.2, 21.11, 22.20

Sample Exams and Study Guide

The following sample exam (from spring 2007) is meant to indicate the types and levels of problems, rather than the coverage (which is outlined in the course calendar). Students are responsible for all sections and topics (in the textbook and class handouts) that are not explicitly excluded in the study guide that follows the sample exam, even if the material was not covered in class lectures.

Sample Midterm Exam (105 minutes)
Problem 1 [15 points] Defining concepts and terms. Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inches per term) [3 points each]: Manchester carry chain; Multiplier recoding; *ulp*; Conditional-sum adder; Parallel prefix graph
Problem 2 [10 points] Number representation. Show that flipping (complementing) the sign bit of k-bit numbers in 2's-complement format results in biased representation and determine the bias amount that characterizes this new representation.
Problem 3 [20 points] Basic design concepts. Draw diagrams showing each of the following. No explanation is necessary; the diagrams should be self-explanatory.
a. How an ordinary binary adder can be augmented to perform addition or subtraction of 2's-complement numbers under the control of an add'/sub signal (0 means "add", 1 means "subtract").
b. How 2-bits-at-a-time or radix-4 sequential multiplication might be performed at high speed without Booth's recoding and without precomputing 3 times the multiplicand.
Problem 4 [15 points] Carry-skip addition.
a. Show that the optimal block width b in a fixed-block carry-skip adder is proportional to the square root of the word width k. [10 points]
b. Briefly discuss why carry-skip adders are of interest at all, given that faster logarithmic-time adders are available. [5 points]
Problem 5 [15 points] Multioperand addition. The following describes a multioperand addition process in tabular form:
0 0 8 8 8 8 8 8 8
0 2 6 6 6 6 6 6 4
0 4 4 4 4 4 4 3 2
1 3 3 3 3 3 3 2 1
2 2 2 2 2 2 2 1 1
a. Explain the process described by this table. [5 points]
b. In the hardware implementation implied by the table, what component types are used and how many of each? Be as precise as possible in specifying the components used. [10 points]
Problem 6 [25 points] Two's-complement multiplication.
a. Represent $x = 3$, $y = -3$, and $z = 5$ as 4-bit 2's-complement numbers. [5 points]

b. Using the right-shift algorithm, perform x times z, using the representations of part a, to get the 8-bit product p = 15. [10 points]
c. Using the left-shift algorithm, perform y times z, to get the 8-bit product p' = −15. [10 points]

Midterm Exam Study Guide
The following textbook sections are excluded from the midterm exam: 3.4-3.6, 4.4-4.6, 6.3, 7.2, 10.5

Research Paper and Presentation

Each student will review a subfield of computer arithmetic or do original research on a selected and approved topic. A tentative list of research topics is provided below; however, students should feel free to propose their own topics for approval. A publishable report earns an "A" for the course, regardless of homework and midterm grades. See the course calendar for schedule and due dates and **Research Paper Guidlines** for formatting tips.

01. Modulo-(2^a+1) Number Representations and Arithmetic (Not selected)

H. T. Vergos and C. Efstathiou, "Efficient Modulo 2^n + 1 Adder Architectures," *Integration, the VLSI J.*, Vol. 42, pp. 149-157, 2009.

G. Jaberipur and B. Parhami, "Unified Approach to the Design of Modulo-$(2^n \pm 1)$ Adders Based on Signed-LSB Representation of Residues," *Proc. 19th IEEE Int'l Symp. Computer Arithmetic*, 8-10 June 2009, to appear. [Preprint available via B. Parhami's publications Web page.]

02. Number Representation with Discrete Logarithms (Not selected)
A. Fit-Florea, L. Li, M. A. Thornton, and D. W. Matula, "A Discrete Logarithm Number System for Integer Arithmetic Modulo 2^k: Algorithms and Lookup Structures," *IEEE Trans. Computers*, Vol. 58, No. 2, pp. 163-174, February 2009.

03. A Comparison of Hardware Multipliers in Microprocessors (Assigned to: **Joshua Fierro**)
G. Colon-Bonet and P. Winterrowd, "Multiplier Evolution: A Family of Multiplier VLSI Implementations," *Computer J.*, Vol. 51, No. 5, pp. 585-594, 2008.

04. Design Methodologies for Implementing Wider Multipliers Using Embedded Multipliers in FPGAs (Assigned to: **Sagar Nataraj**)
S. Gao, D. Al-Khalili, and N. Chabini, "Efficient Realization of Large Size Two's Complement Multipliers Using Embedded Blocks in FPGAs," *Circuits, Systems, and Signal Processing*, Vol. 27, No. 5, pp. 713-731, October 2008.
J.-L. Beuchat and A. Tisserand, "Small Multiplier Based Multiplication and Division Operators for Virtex-II Devices," *Proc. 12th Int'l Conf. Field-Programmable Logic and Applications*, 2002, pp. 513-522.

05. Radix-16 SRT Division in Intel's New Penryn Processor (Not selected)
[Intel's] New Radix-16 Divider

06. Augmenting FPGAs for Faster Arithmetic Operations (Assigned to: **Nikolas Sumikawa**)
H. Parandeh-Afshar, A. K. Verma, P. Brisk, and P. Ienne, "Improving FPGA Performance for Carry-Save Arithmetic," *IEEE Trans. VLSI Systems*, Vol. 18, No. 4, pp. 578-590, April 2010.

07. Cube Roots: Hardware Algorithms and Applications (Assigned to: **Michael Bowling**)
A. Pineiro, J. D. Bruguera, F. Lamberti, and P. Montuschi, "A Radix-2 Digit-by-Digit Architecture for Cube Root," *IEEE Trans. Computers*, Vol. 57, No. 4, pp. 562-566, April 2008.
Cube-Roots via Newton-Raphson Method

08. Accurate Summation of Sets of Floating-Point Numbers (Assigned to: **Karthick Santhanam**)
A. Eisinberg and G. Fedele, "Accurate Floating-Point Summation: A New Approach," *Applied Mathematics and Computation*, Vol. 189, pp. 410-424, 2007.
T. Ogita, S. M. Rump, and S. Oishi, "Accurate Sum and Dot Product," *SIAM J. Scientific Computing*, Vol. 26 , No. 6, pp. 1955-1988, 2005.

09. Function Evaluation by Piecewise Linear Approximation (Not selected)

N. Takagi, "Powering by a Table Look-Up and A Multiplication with Operand Modification," *IEEE Trans. Computers*, Vol. 47, No. 11, pp. 1216-1222, Nov. 1998.
O. Gustafsson and K. Johanson, "Multiplierless Piecewise Linear Approximation of Elementary Functions," *Proc. 40th Asilomar Conf. Signals, Systems, and Computers*, October 2006.

10. Smaller Lookup Tables by Exploiting Symmetry and Nonuniform Segmentation (Assigned to: **George Leming**)
D.-U Lee, R. C. C. Cheung, W. Luk, and J. D. Villasenor, "Hierarchical Segmentation for Hardware Function Evaluation," *IEEE Trans. VLSI Systems*, Vol. 17, No. 1, pp. 103-116, January 2009.
T. Sasao, S. Nagayama, and J. T. Butler, "Numerical Function Generators Using LUT Cascades," *IEEE Trans. Computers*, Vol. 56, No. 6, pp. 826-838, June 2007.

11. Sign/Logarithmic Arithmetic and the European Logarithmic Microprocessor (Assigned to: **Manik Chugh**)
J. N. Coleman, et al., "The European Logarithmic Microprocessor," *IEEE Trans. Computers*, Vol. 57, No. 4, pp. 532-546, April 2008.
J. N. Coleman, E. I. Chester, C. I. Softley, and J. Kadlec, "Arithmetic on the European Logarithmic Microprocessor," *IEEE Trans. Computers*, Vol. 49, No. 7, pp. 702-715, July 2000.

12. Arithmetic and Energy Economy Provisions in IBM's Blue Gene/L Parallel Supercomputer (Assigned to: **Samantha Alt**)
J. Lorenz, S. Kral, F. Franchetti, and C.W. Ueberhuber, "Vectorization Techniques for the Blue Gene/L Double FPU," *IBM J. Research and Development*, Vol. 49, Nos. 2/3, pp. 437-446, March/May 2005.
S. Chatterjee, et al., "Design and Exploitation of a High-Performance SIMD Floating-Point Unit for Blue Gene/L," *IBM J. Research and Development*, Vol. 49, Nos. 2/3, pp. 377-391, March/May 2005.

13. Arithmetic in Graphic Processors (Not selected)
D. De Caro, N. Petra, and A. G. M. Strollo, "High-Performance Special Function Unit for Programmable 3-D Graphic Processors," *IEEE Trans. Circuits and Systems I*, Vol. 56, No. 9, pp. 1968-1978, September 2009.
D. Blythe, "Rise of the Graphics Processor," *Proc. IEEE*, Vol. 96, No. 5, pp. 761-778, May 2008.

14. Argument Reduction for Faster, More Accurate Function Evaluation (Not selected)
S. Boldo, M. Daumas, and R.-C. Li, "Formally Verified Argument Reduction with a Fused Multiply-Add," *IEEE Trans. Computers I*, Vol. 58, No. 8, pp. 1139-1145, August 2009.
N. Brisebarre, et al., "A New Range-Reduction Algorithm," *IEEE Trans. Computers*, Vol. 54, No. 3, pp. 331-339, March 2005.

15. Low-Power Full-Adder Cells and Their Applications (Assigned to: **Royce Newcomb**)
K. Navi, et al., "A Novel Low-Power Full-Adder Cell for Low Voltage," *Integration, the VLSI J.*, Vol. 42, No. 4, pp. 457-467, September 2009.
M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications," *IEEE Trans. VLSI Systems*, to appear [downloadable from IEEE Explore].

16. Parallel-Prefix Ling Adders (Assigned to: **Prashant Sanjay**)
N. Burgess, "Implementation of Recursive Ling Adders in CMOS VLSI," *Proc. 43rd Asilomar Conf. Signals, Systems, and Computers*, November 2009, pp. 1777-1781.

17. Elliptic Curve Operations in GF(p) (Proposed by, and assigned to: **Jeffrey Tikkanen**)
C. K. Koc (ed.), *Cryptographic Engineering*, Springer, 2009.
S. Kumar, *Elliptic Curve Cryptography for Constrained Devices*, VDM Verlag, 2008.
J. Solinas, "Generalized Mersenne numbers," Tech. Report CORR 99-39, Dept. C&O, U. Waterloo, 1999.

18. Low-Power Arithmetic Circuits Using Lateral NEMFETs (Proposed by, and assigned to: **Shantanu Samant**)
H. Dadgour and K. Banerjee, "Hybrid NEMS-CMOS Integrated Circuits: A Novel Strategy for Energy-Efficient Designs," *IET Computers and Digital Techniques*, Vol. 3, No. 6, pp. 593-608, November 2009.
G. Dimitrakopoulos and D. Nikolos, "High-Speed Parallel-Prefix VLSI Ling Adders," *IEEE Trans. Computers*, Vol. 54, No. 2, pp. 225-231, February 2005.

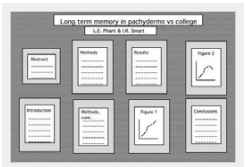
19. Low-Power Design Techniques for Multipliers (Assigned to: **Urmish Shah**)
I. S. Abu-Khater, A. Bellaouar, and M. I. Elmasry, "Circuit Techniques for CMOS Low-Power High-Performance

Multipliers," *IEEE J. Solid-State Circuits*, Vol. 31, pp. 1535-1546, October 1996.
S. S. Mahant-Shetti, P. T. Balsara, and C. Lemonds, "High Performance Low Power Array Multiplier Using Temporal Tiling," *IEEE Trans. VLSI Systems*, Vol. 7, No. 1, pp. 121-124, March 1999.

20. Survey of Multiplier Circuits in Digital Signal Processors (Assigned to: **Ravi Zende**)
J. M. Jou, S. R. Kuang, and R. D. Chen, "Design of Low-Error Fixed-Width Multipliers for DSP Applications," *IEEE Trans. Circuits and Systems II*, Vol. 46, pp. 836-842, June 1999.
S. J. Jou, M.-H. Tsai, and Y.-L. Tsao, "Low-Error Reduced-Width Booth Multipliers for DSP Applications," *IEEE Trans. Circuits and Systeme I*, Vol. 50, No. 11, pp. 1470-1474, November 2003.

21. Dedicated Hardware Multipliers on FPGA Chips (Not selected)
Using Embedded Multipliers in Spartan-3 FPGAs

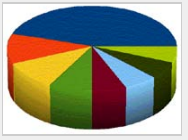
Poster Presentation Tips



Here are some guidelines for preparing your research poster. The idea of the poster is to present your research results and conclusions thus far, get oral feedback during the session from the instructor and your peers, and to provide the instructor with something to comment on before your final report is due. Please send a PDF copy of the poster via e-mail by midnight on the poster presentation day.

Posters prepared for conferences must be colorful and eye-catching, as they are typically competing with dozens of other posters for the attendees' attention. Here is an **example of a conference poster**. Such posters are often mounted on a colored cardboard base, even if the pages themselves are standard PowerPoint slides. In our case, you should aim for a "plain" poster (loose sheets, to be taped to the wall in our classroom) that conveys your message in a simple and direct way. Eight to 10 pages, each resembling a PowerPoint slide, would be an appropriate goal. You can organize the pages into 2 x 4 (2 columns, 4 rows), 2 x 5, or 3 x 3 array on the wall. The top two of these might contain the project title, your name, course name and number, and a very short (50-word) abstract. The final two can perhaps contain your conclusions and directions for further work (including work that does not appear in the poster, but will be included in your research report). The rest will contain brief description of ideas, with emphasis on diagrams, graphs, tables, and the like, rather than text which is very difficult to absorb for a visitor in a very limited time span.

Grade Statistics



Homework grades are in the [0, 4] range; other grades are in percent.
HW1 grades: Range = [2.0, 4.0], Mean = 3.6, SD = 0.7, Median = 4.0
HW2 grades: Range = [3.0, 4.0], Mean = 3.7, SD = 0.3, Median = 3.7
HW3 grades: Range = [2.0, 4.0], Mean = 3.5, SD = 0.7, Median = 3.7
HW4 grades: Range = [3.0, 4.0], Mean = 3.6, SD = 0.4, Median = 3.7
Midterm grades: Range = [34, 83], Mean = 60, SD = 13, Median = 62
Research & presentation grades: Range = [65, 85], Mean = 76, SD = 7, Median = 75

References

Primary textbook (required):
Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*, Oxford, 2nd ed., 2010.

Verilog descriptions of arithmetic circuits (recommended):
This course does not involve a lab component or implementation projects. For those interested in pursuing practical circuit implementations, the following book may be useful:
Cavanagh, *Computer Arithmetic and Verilog HDL Fundamentals*, CRC Press, 2010.

Other useful books (not required):
Ercegovac/Lang, *Digital Arithmetic*, Morgan Kaufmann, 2004 (QA76.9.C62E73)
Koren, *Computer Arithmetic Algorithms*, 2nd ed., A K Peters, 2002 (QA76.9.C62K67)
Swartzlander, *Computer Arithmetic*, vols. 1-2, IEEE Computer Society Press, 1990 (QA76.6.C633)
Deschamps/Bioul/Sutter, *Synthesis of Arithmetic Circuits: ...* , Wiley, 2006 (TK7895.A65D47)
Omondi, *Computer Arithmetic Systems: ...* , Prentice-Hall, 1994 (QA76.9.C62O46)
Ercegovac/Lang, *Division and Square Root: ...* , Kluwer, 1994 (QA76.9.C62E73)

Oklobdzija, *High-Performance System Design*, IEEE Press, 1999 (TK7871.99.M44037)
Waser/Flynn, *Intro. Arithmetic for Digital Systems Designers*, HR&W, 1982 (TK7895.A65W37.1982)
Knuth, *The Art of Computer Programming: Seminumerical Algorithms*, Wiley, 1981 (QA76.6.K64 vol 2)
Kulisch/Miranker, *Computer Arithmetic in Theory and Practice*, Academic Press, 1981 (QA162.K84)

Research resources:
Proc. IEEE Symp. Computer Arithmetic, 1969, 72, 75 78, 81 and subsequent odd years; ARITH-19, June 2009
On-line proceedings for IEEE Symp. Computer Arithmetic, 1969-2007
IEEE Trans. Computers, particularly special issues or sections on computer arithmetic (8/70, 6/73, 7/77, 4/83, 8/90, 8/92, 8/94, 7/98, 7/00, 3/05, 2/09)
UCSB library's electronic journals, collections, and other resources
UCSB library's research guide in ECE

Miscellaneous Information

Motivation: Computer arithmetic is a subfield of digital computer organization. It deals with the hardware realization of arithmetic functions to support various computer architectures as well as with arithmetic algorithms for firmware/software implementation. A major thrust of digital computer arithmetic is the design of hardware algorithms and circuits to enhance the speed of various numeric operations. Thus much of what is presented in this course complements the architectural and algorithmic speedup techniques covered as part of the advanced computer architecture (ECE 254A/B/C) sequence.

Catalog entry: **252B. Computer Arithmetic. (4) PARHAMI.** *Prerequisites: ECE 152A-B. Lecture, 4 hours*. Standard and unconventional number representations. Design of fast two-operand and multioperand adders. High-speed multiplication and division algorithms. Floating-point numbers, algorithms, and errors. Hardware algorithms for function evaluation. Pipelined, digit-serial and fault-tolerant arithmetic processors.

History: Professor Parhami took over the teaching of ECE 252B from the late Dr. James Howard in the winter quarter of 1989. By covering sequential machines, computer arithmetic, and advanced microprocessor-based design, the graduate course sequence ECE 252A/B/C was meant to provide a firm foundation in the theories and techniques of advanced digital design. During the first few offerings of ECE 252B, Professor Parhami gradually modified the content to increase both its coverage and research orientation (ECE 252A and 252C later underwent similar transformations by Professor Kwang-Ting Cheng and Professor Parhami, respectively). In 2000, based on a decade of experience in teaching this course, Professor Parhami published a graduate-level textbook, ***Computer Arithmetic: Algorithms and Hardware Designs*** (Oxford University Press), which is being used at many universities worldwide. The second edition of this textbook will appear in 2010.
Offering of ECE 252B in spring 2009 (PDF file)
Offerings of ECE 252B from 2000 to 2008 (PDF file)