## Part III <br> Mesh-Based Architectures

## Introduction to Parallel Processing

Aggorithms and Architectures


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| Part I: | Background and | 1. Introduction to Parallelism |
| :---: | :---: | :---: | 2. A Taste of Parallel Algorithms

3. Parallel Algorithm Complexity
4. Models of Parallel Processing

| $$ | Part II: <br> Extreme Models | Abstract View of <br> Shared Memory <br> Circuit Model of Parallel Systems | 5. PRAM and Basic Algorithms <br> 6. More Shared-Memory Algorithms <br> 7. Sorting and Selection Networks <br> 8. Other Circuit-Level Examples |
| :---: | :---: | :---: | :---: |
|  | Part III: <br> Mesh-Based | $\begin{aligned} & \hline \text { Data Movement on } \\ & 2 D \text { Arrays } \\ & \hline \end{aligned}$ | 9. Sorting on a 2 D Mesh or Torus <br> 10. Routing on a 2 D Mesh or Torus <br> 11. Numerical 2D Mesh Algorithms <br> 12. Other Mesh-Related Architectures |
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| Part VI: Implementation Aspects | Control-Parallel Systems | 21. Shared-Memory MIMD Machines 22. Message-Passing MIMD Machines |
| :---: | :---: | :---: |
|  | Data Parallelism and Conclusion | 23. Data-Parallel SIMD Machines <br> 24. Past, Present, and Future |



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## About This Presentation

This presentation is intended to support the use of the textbook Introduction to Parallel Processing: Algorithms and Architectures (Plenum Press, 1999, ISBN 0-306-45970-1). It was prepared by the author in connection with teaching the graduate-level course ECE 254B: Advanced Computer Architecture: Parallel Processing, at the University of California, Santa Barbara. Instructors can use these slides in classroom teaching and for other educational purposes. Any other use is strictly prohibited. © Behrooz Parhami

| Edition | Released | Revised | Revised | Revised |
| :--- | :---: | :---: | :---: | :---: |
| First | Spring 2005 | Spring 2006 | Fall 2008 | Fall 2010 |
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|  |  | Winter 2019 | Winter 2020 | Winter 2021 |

## III Mesh-Type Architectures

Study mesh, torus, and related interconnection schemes:

- Many modern parallel machines are mesh/torus-based
- Scalability and speed due to short, regular wiring
- Enhanced meshes, variants, and derivative networks


## Topics in This Part

Chapter 9 Sorting on a 2D Mesh or Torus
Chapter 10 Routing on a 2D Mesh or Torus
Chapter 11 Numerical 2D Mesh Algorithms
Chapter 12 Mesh-Related Architectures


## 9 Sorting on a 2D Mesh or Torus

Introduce the mesh model (processors, links, communication):

- Develop 2D mesh sorting algorithms
- Learn about strengths and weaknesses of 2D meshes

Topics in This Chapter<br>9.1 Mesh-Connected Computers<br>9.2 The Shearsort Algorithm<br>9.3 Variants of Simple Shearsort<br>9.4 Recursive Sorting Algorithms<br>9.5 A Nontrivial Lower Bound<br>9.6 Achieving the Lower Bound



### 9.1 Mesh-Connected Computers



2D, four-neighbor (NEWS) mesh; other types in Chapter 12

Square $p^{1 / 2} \times p^{1 / 2}$ or rectangular $r \times p / r$

MIMD, SPMD, SIMD, Weak SIMD

Single/All-port model
Diameter-based or bisection-based lower bound: $\mathrm{O}\left(p^{1 / 2}\right)$

Fig. 9.1 Two-dimensional mesh-connected computer.

## MIMD, SPMD, SIMD, or Weak SIMD Mesh


a. MIMD all-port








 0
c. SIMD single-port


b. MIMD Single-port




d. Weak SIMD

Some communication modes.

All-port: Processor can communicate with all its neighbors at once (in one cycle or time step)

Single-port: Processor can send/receive one message per time step

MIMD: Processors choose their communication directions independently

SIMD: All processors directed to do the same

Weak SIMD: Same direction for all (uniaxis)

## Torus Implementation without Long Wires



Fig. 9.2 A $5 \times 5$ torus folded along its columns. Folding this diagram along the rows will produce a layout with only short links.

## Processor Indexing in Mesh or Torus


a. Row-major

| 0 | 1 | 4 | 5 |
| ---: | ---: | ---: | ---: |
| 2 | 3 | 6 | 7 |
| 8 | 9 | 12 | 13 |
| 10 | 11 | 14 | 15 |

c. Shuffled row-major

b. Snakelike row-major

d. Proximity order

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## Register-Based Communication



Fig. 9.4 Reading data from NEWS neighbors via virtual local registers.

### 9.2 The Shearsort Algorithm

Shearsort algorihm for a 2D mesh with r rows

$$
T_{\text {shearsort }}=\left\lceil\log _{2} r\right\rceil(p / r+r)+p / r
$$ repeat $\lceil\log 2 \mathrm{r}\rceil$ times


endrepeat then
sort the
columns
(top-to-
bottom)


On a square mesh: $T_{\text {shearsort }}=p^{1 / 2}\left(\log _{2} p+1\right)$

Diameter-based LB:
$T_{\text {sort }} \geq 2 p^{1 / 2}-2$
Sort the rows


Snakelike
(depending on the desired final sorted order)


Row-Major

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Fig. 9.5 Description of the shearsort algorithm on an $r$-row 2D mesh.

## Proving Shearsort Correct

Row 2i
Row $2 \mathrm{i}+1$

Case (a): More 0s

Case (b):
More 1s


Case (c): Equal \# 0s \& 1s



Sinks down in the next column sort

Assume that in doing the column sorts, we first sort pairs of elements in the column and then sort the entire column

Fig. 9.6 A pair of dirty rows create at least one clean row in each shearsort iteration

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## Shearsort Proof (Continued)



Fig. 9.7 The number of dirty rows halves with each shearsort iteration.

After $\log _{2} r$ iterations, only one dirty row remains


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## Shearsort Example



Fig. 9.8 Example of shearsort on a $4 \times 4$ mesh.

### 9.3 Variants of Simple Shearsort

Observation: On a linear array, odd-even transposition sort needs only $k$ steps if the "dirty" (unsorted) part of the array is of length $k$

$$
\begin{array}{llllll|llllllllllllllll}
0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\
\text { Unsorted part } & & & & & & & & &
\end{array}
$$


#### Abstract

In shearsort, we do not have to sort columns completely, because only a portion of the column is unsorted (the portion shrinks in each phase)


$$
T_{\text {opt shearsort }}=\underbrace{\left.(p / r)\left(\log _{2} r\right\rceil+1\right)}_{2 r-2}+
$$

Thus, $2 r-2$ replaces $r \log _{2} r$ in simple shearsort

At most $\lceil\mathrm{X} / 2\rceil$
dirty rows
On a square mesh:

$$
\begin{aligned}
& T_{\text {opt shearsort }}= \\
& p^{1 / 2}\left(1 / 2 \log _{2} p+3\right)-2
\end{aligned}
$$

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Keys | 1 | 12 | 21 | 4 |
| :---: | :---: | :---: | :---: |
| 6 | 26 | 25 | 10 |
| 15 | 20 | 13 | 2 |
| 31 | 32 | 16 | 30 |
| 5 | 9 | 18 | 7 |
| 11 | 19 | 27 | 8 |
| 22 | 3 | 14 | 17 |
| 28 | 23 | 29 | 24 |

Two keys held by one processor

# Shearsort with Multiple Items per Processor 


#### Abstract

Perform ordinary shearsort, but replace compare-exchange with merge-split $(n / p) \log _{2}(n / p)$ steps for the initial sort; the rest multiplied by $n / p$


Fig. 9.9 Example of shearsort on a $4 \times 4$ mesh with two keys stored per processor.

The final row sort (snake-like or row-major) is not shown.

### 9.4 Recursive Sorting Algorithms



1. Sort quadrants

2. Sort columns

3. Sort rows

4. Apply $4 \sqrt{ } p$ steps of odd-even transposition along the overall snake

Snakelike sorting order on a square mesh
$T\left(p^{1 / 2}\right)=T\left(p^{1 / 2} / 2\right)+5.5 p^{1 / 2}$
Note that row sort in phase 2 needs fewer steps

$$
T_{\text {recursive } 1} \cong 11 p^{1 / 2}
$$

Fig. 9.10 Graphical depiction of the first recursive algorithm for sorting on a 2D mesh based on four-way divide and conquer.

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## Proof of the $11 p^{1 / 2}$-Time Sorting Algorithm



State of the array after Phase 3

| 0 | $x$ rows | Fig. 9.11 <br> The proof <br> of the first |
| :---: | :--- | :--- |
| $\sqrt{\sqrt{p}-x-x^{\prime}}$ |  |  |
| rows | recursive <br> sorting |  |
| 1 | $x^{\prime}$ rows | algorithm <br> for 2D <br> meshes. |

$$
x \geq b+c+\lfloor(a-b) / 2\rfloor+\lfloor(d-c) / 2\rfloor \quad \text { A similar inequality applies to } x^{\prime}
$$

$$
\begin{aligned}
x+x^{\prime} & \geq b+c+\lfloor(a-b) / 2\rfloor+\lfloor(d-c) / 2\rfloor+a^{\prime}+d^{\prime}+\left\lfloor\left(b^{\prime}-a^{\prime}\right) / 2\right\rfloor+\left\lfloor\left(c^{\prime}-d^{\prime}\right) / 2\right\rfloor \\
& \geq b+c+a^{\prime}+d^{\prime}+(a-b) / 2+(d-c) / 2+\left(b^{\prime}-a^{\prime}\right) / 2+\left(c^{\prime}-d^{\prime}\right) / 2-4 \times^{1} / 2 \\
& =\left(a+a^{\prime}\right) / 2+\left(b+b^{\prime}\right) / 2+\left(c+c^{\prime}\right) / 2+\left(d+d^{\prime}\right) / 2-2 \\
& \geq p^{1 / 2}-4
\end{aligned}
$$

## Some Programming Considerations



1. Sort quadrants

2. Sort columns


3. Sort rows

4. Apply $4 \sqrt{ } p$ steps of odd-even transposition along the overall snake

Fig. 9.10

Let $b$ (a power of 2 ) be the block length for snakelike sorting
snakelike-mesh-sort(b)
snakelike-mesh-sort(b/2)
snakelike-row-sort(b)
column-sort(b)
snake-odd-even-xpose(4b)
snakelike-row-sort(b)
for $k=0$ to $b-1 \operatorname{Proc}(i, j), j$ even, do case $i, k$ even; even: if $j \neq 0 \bmod b$ AND (R5) < (R3) then R5 $\leftrightarrow$ R3 even, odd: if $(R 2)<(R 5)$ then $R 2 \leftrightarrow R 5$

Fig. 9.4

## Another Recursive Sorting Algorithm



1. Sort quadrants

2. Sort double columns in snakelike order


Distribute
these $\sqrt{ } p / 2$ columns $\prod \|$ evenly

Fig. 9.12 Graphical depiction of the second recursive algorithm for sorting on a 2D mesh based on four-way divide and conquer.

$$
T\left(p^{1 / 2}\right)=T\left(p^{1 / 2} / 2\right)+4.5 p^{1 / 2}
$$

Note that the distribution in phase 2 needs $1 / 2 p^{1 / 2}$ steps
$T_{\text {recursive } 2} \cong 9 p^{1 / 2}$

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## Proof of the $9 p^{1 / 2}$-Time Sorting Algorithm



Fig. 9.13 The proof of the second recursive sorting algorithm for 2D meshes.

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## Our Progress in Mesh Sorting Thus Far

Lower bounds: Theoretical arguments based on bisection width, and the like

Upper bounds: Deriving/analyzing algorithms and proving them correct



### 9.5 A Nontrivial Lower Bound




Any of the values 1-63 can be forced into any desired column in sorted order by mixing 0s and 64s in the shaded area

Fig. 9.15 Illustrating the effect of fewer or more 0 s in the shaded area.

| 0 | 0 | 0 | 0 | 1 |
| :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 2 | 3 |
| 0 | 0 | 4 | 5 | 6 |
| 0 | 7 | 8 | 9 | 10 |
| 11 | 12 | 13 | 14 | 15 |


| 16 | 16 | 16 | 16 | 1 |
| :---: | :---: | :---: | :---: | :---: |
| 16 | 16 | 16 | 2 | 3 |
| 16 | 16 | 4 | 5 | 6 |
| 16 | 7 | 8 | 9 | 10 |
| 11 | 12 | 13 | 14 | 15 |

$\left.\begin{array}{|c|c|c|c|}\hline 0 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \hline & 0 \\ \hline 1 & 2 & 3 & 4\end{array}\right) 5$.

| 1 | 2 | 3 | 4 | 5 |
| :---: | :---: | :---: | :---: | :---: |
| 10 | 9 | 8 | 7 | 6 |
|  | 12 | 13 | 14 | 15 |
|  | 16 | 16 | 16 | 16 |
| 16 | 16 | 16 | 16 | 16 |

## Proving the Lower Bound

Any of the values 1-63 can be forced into any desired column in sorted order by mixing 0s and 64 s in the shaded area

Fig. 9.15 (Alternate version) Illustrating the effect of fewer or more 0s in the shaded area.

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### 9.6 Achieving the Lower Bound

Schnorr-Shamir snakelike sorting

1. Sort each block in snakelike order
2. Permute columns such that the columns of each vertical slice are evenly distributed among all slices
3. Sort each block in snakelike order
4. Sort columns from top to bottom
5. Sort Blocks $0 \& 1,2 \& 3, \ldots$ of all vertical slices together in snakelike order; i.e., sort within $2 p^{3 / 8} \times p^{3 / 8}$ submeshes
6. Sort Blocks $1 \& 2,3 \& 4, \ldots$ of all vertical slices together in snakelike order
(7.) Sort rows in snakelike order
7. Apply $2 p^{3 / 8}$ steps of odd-even transposition to the snake

Fig. 9.16 Notation for the asymptotically optimal sorting algorithm.


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## Elaboration on the $3 p^{1 / 2}$ Lower Bound

In deriving the $3 p^{1 / 2}$ lower bound for snakelike sorting on a square mesh, we implicitly assumed that each processor holds one item at all times

## Without this assumption, the following algorithm leads to a running time of about $2.5 p^{1 / 2}$

Phase 1: Move all data to the center $p^{1 / 2} / 2$ columns

Phase 2: Perform 2-2 sorting in the half-wide center mesh

Phase 3: Distribute data from center half of each row to the entire row



## 10 Routing on a 2D Mesh or Torus

Routing is nonexistent in PRAM, hardwired in circuit model:

- Study point-to-point and collective communication
- Learn how to route multiple data packets to destinations

Topics in This Chapter<br>10.1 Types of Data Routing Operations<br>10.2 Useful Elementary Operations<br>10.3 Data Routing on a 2D Array<br>10.4 Greedy Routing Algorithms<br>10.5 Other Classes of Routing Algorithms<br>10.6 Wormhole Routing



### 10.1 Types of Data Routing Operations

Point-to-point communication: one source, one destination
Collective communication
One-to-many: multicast, broadcast (one-to-all), scatter Many-to-one: combine (fan-in), global combine, gather Many-to-many: all-to-all broadcast (gossiping), scatter-gather


## Types of Data Routing Algorithms

Oblivious: A source-destination pair leads to a unique path; non-fault-tolerant

Adaptive: One of the available paths is chosen dynamically; can avoid faulty nodes/links or route around congested areas
Degree of adaptivity leads to trade-offs between decision simplicity (e.g., hard to avoid infinite loops) and routing flexibility

Optimal (shortest-path): Only shortest paths considered; can be oblivious or adaptive

Non-optimal (non-shortest-path): Selection of shortest path is not guaranteed, although most algorithms tend to choose a shortest path if possible


## Our First Encounter with Data Routing Issues

Shared memory: Processors can communicate by storing data into and reading data from the memory

Circuit model: Sending results from one part of the system to other parts is hardwired at design time


Sorting network


Graph model: We must specify the routing process explicitly

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## 1-to-1 Communication (Point-to-Point Messages)

| $a$ | $b$ |  |  |
| :--- | :--- | :--- | :--- |
|  |  | $c$ |  |
|  | $d$ | $e$ | $f$ |
| $g$ |  | $h$ |  |



Packet destinations


Message sources, destinations, and routes


Destination nodes
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## Routing Operations Specific to Meshes

Data compaction or packing
Move scattered data elements to the smallest possible submesh (e.g., for problem size reduction)


| a | b | c |  |
| :---: | :---: | :---: | :--- |
| d | e | f |  |
| g | h |  |  |
|  |  |  |  |

Fig. 10.1 Example of data compaction or packing.
Random-access write (RAW)
Emulates one write step in PRAM (EREW vs CRCW)

Routing algorithm is critical


Packet sources


Packet destinations

Random-access read (RAR)
Can be performed as two RAWs: Write source addresses to destinations; write data back to sources (emulates on PRAM memory read step)


### 10.2 Useful Elementary Operations

Row/Column rotation
All-to-all broadcasting in a row or column

Sorting in various orders
Chapter 9

## Semigroup computation

Fig. 10.2 Recursive semigroup computation in a 2D mesh.


Horizontal combining $\cong \sqrt{p} / 2$ steps



Vertical Combining


Vertical combining
$\cong \sqrt{ } \mathrm{p} / 2$ steps


Horizontal Combining (includes reversal)

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### 10.3 Data Routing on a 2D Array

Exclusive random-access write on a 2D mesh: MeshRAW

1. Sort packets in column-major order by destination column number; break ties by destination row number
2. Shift packets to the right, so that each item is in the correct column (no conflict; at most one element in a row headed for a given column)
3. Route the packets within each column


Fig. 10.5 Example of random-access write on a 2D mesh.


## Analysis of Sorting-Based Routing Algorithm




After row routing
Not a shortest-path algorithm

$$
\begin{aligned}
T= & 3 p^{1 / 2}+o\left(p^{1 / 2}\right) & & \text { \{snakelike sorting\} } \\
& +p^{1 / 2} & & \text { \{odd column reversals \}} \\
& +2 p^{1 / 2}-2 & & \text { \{row \& column routing\} } \\
= & 6 p^{1 / 2}+o\left(p^{1 / 2}\right) & & \\
= & 11 p^{1 / 2}+o\left(p^{1 / 2}\right) & & \text { with unidirectional commun. }
\end{aligned}
$$

Node buffer space requirement: 1 item at any given time

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### 10.4 Greedy Routing Algorithms

Greedy algorithm: In each step, try to make the most progress toward the solution based on current conditions or information available

This local or short-term optimization often does not lead to a globally optimal solution; but, problems with optimal greedy algorithms do exist


Fig. 10.6 Greedy row-first routing on a 2D mesh.

## Analysis of Row-First Greedy Routing

$$
T=2 p^{1 / 2}-2
$$

This optimal time achieved if we give priority to messages that need to go further along a column

Thus far, we have two mesh routing algorithms:
$6 p^{1 / 2}$-step, 1 buffer per node
$2 p^{1 / 2}$-step, time-optimal, but needs large buffers

Question: Is there a middle ground?


Fig. 10.7 Demonstrating the worst-case buffer requirement with row-first routing.

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## An Intermediate Routing Algorithm

Sort $\left(p^{1 / 2} / q\right) \times\left(p^{1 / 2} / q\right)$ submeshes in column-major order

Perform greedy routing

Let there be $r_{k}$ packets in $B_{k}$ headed for column $j$

Number of row-i packets headed for column $j$ :

$$
\begin{aligned}
& \sum_{k=0 \text { to } q-1}\left\lceil r_{k} /\left(p^{1 / 2} / q\right)\right\rceil \\
& \quad<\sum\left[1+r_{k} /\left(p^{1 / 2} / q\right)\right] \\
& \quad \leq q+\left(q / p^{1 / 2}\right) \sum r_{k} \leq 2 q
\end{aligned}
$$

Fig. 10.8 Illustrating the structure of the intermediate routing algorithm.


So, $2 q-1$ buffers suffice

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## Analysis of the Intermediate Algorithm

Buffers: $2 q-1$, Intermediate between 1 and $O\left(p^{1 / 2}\right)$

Sort time: $4 p^{1 / 2 / q}+o\left(p^{1 / 2} / q\right)$
Routing time: $2 p^{1 / 2}$
Total time: $\cong 2 p^{1 / 2}+4 p^{1 / 2 / q}$
One extreme, $q=1$ :
Degenerates into sorting-based routing

Another extreme, large $q$ : Approaches the greedy routing algorithm


Fig. 10.8 Illustrating the structure of the intermediate routing algorithm.

### 10.5 Other Classes of Routing Algorithms

Row-first greedy routing has very good average-case performance, even if the node buffer size is restricted

Idea: Convert any routing problem to two random instances by picking a random intermediate node for each message

Regardless of the routing algorithm used, concurrent writes can degrade the performance

Priority or combining scheme can be built into the routing algorithm so that congestion close to the common destination is avoided


Fig. 10.9 Combining of write requests headed for the same destination.

## Types of Routing Problems or Algorithms

Static:
Dynamic:
Off-line:
On-line:
Oblivious:
Adaptive:
Deflection:

Packets to be routed all available at $t=0$
Packets "born" in the course of computation
Routes precomputed, stored in tables
Routing decisions made on the fly
Path depends only on source and destination Path may vary by link and node conditions

Any received packet leaves immediately, even if this means misrouting (via detour path); also known as hot-potato routing


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### 10.6 Wormhole Routing

Circuit switching: A circuit is established between source and destination before message is sent (as in old telephone networks)

Advantage: Fast transmission after the initial overhead
Packet switching: Packets are sent independently over possibly different paths

Advantage: Efficient use of channels due to sharing

Wormhole switching: Combines the advantages of circuit and packet switching


Fig. 10.10 Worms and deadlock in wormhole routing.

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## Route Selection in Wormhole Switching

Routing algorithm must be simple to make the route selection quick
Example: row-first routing, with 2-byte header for row \& column offsets
But . . . care must be taken to avoid excessive blocking and deadlock

(a) Two worms en route to their respective destinations

(b) Deadlock due to circular waiting of four blocked worms

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## Dealing with Conflicts



Fig. 10.11 Various ways of dealing with conflicts in wormhole routing.

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## Deadlock in Wormhole Switching

Each worm is blocked at the point of attempted right turn


Deadlock avoidance requires a more complicated routing algorithm and/or more conservative routing decisions
... nontrivial performance penalties

## Deadlock Avoidance via Dependence Analysis



3-by-3 mesh with its links numbered


Unrestricted routing (following shortest path)


E-cube routing (row-first)

A sufficient condition for lack of deadlocks is to have a link dependence graph that is cycle-free

Less restrictive models are also possible; e.g., the turn model allows three of four possible turns for each worm

Fig. 10.12 Use of dependence graph to check for the possibility of deadlock

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## Deadlock Avoidance via Virtual Channels



Deadlock Avoidance via Routing Restrictions

Allow only three of the four possible turns



## 11 Numerical 2D Mesh Algorithms

Become more familiar with mesh/torus architectures by:

- Developing a number of useful numerical algorithms
- Studying seminumerical applications (graphs, images)

| Topics in This Chapter |  |
| :--- | :--- |
| 11.1 | Matrix Multiplication |
| 11.2 | Triangular System of Linear Equations |
| 11.3 | Tridiagonal System of Linear Equations |
| 11.4 | Arbitrary System of Linear Equations |
| 11.5 | Graph Algorithms |
| 11.6 | Image-Processing Algorithms |



### 11.1 Matrix Multiplication



Fig. 11.1 Matrix-vector multiplication on a linear array.
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## Another View of Matrix-Vector Multiplication


$m$-processor linear array for multiplying an $m$-vector by an $m \times m$ matrix.


## Mesh Matrix Multiplication

Fig. 11.2 Matrix-matrix multiplication on a 2D mesh.
$C=A B$ or
$c_{i j}=\sum_{k=0 \text { to } m-1} a_{i k} b_{k j}$
Col 0 of $B$
Row 0 of $A$

$p=m^{2}, T=3 m-2$

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## Matrix-Vector Multiplication on a Ring



Fig. 11.3 Matrix-vector multiplication on a ring.

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## Torus Matrix Multiplication

Fig. 11.4 Matrix-matrix multiplication on a 2D torus.
$C=A B$ or
$c_{i j}=\sum_{k=0 \text { to } m-1} a_{i k} b_{k j}$
$p=m^{2}, T=m=p^{1 / 2}$

For $m>p^{1 / 2}$, use block matrix multiplication

Can gain efficiency from overlapping communication with computation


### 11.2 Triangular System of Linear Equations



Fig. 11.5 Lower/upper triangular square matrix; if $a_{i i}=0$ for all $i$, then it is strictly lower/upper triangular.

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## Forward Substitution on a Linear Array



Fig. 11.6 Solving a triangular system of linear equations on a linear array.

Triangular Matrix Inversion: Algorithm


Fig. 11.7 Inverting a triangular matrix by solving triangular systems of linear equations.

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## Triangular Matrix Inversion on a Mesh



Fig. 11.8 Inverting a lower triangular matrix on a 2D mesh.

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### 11.3 Tridiagonal System of Linear Equations

$$
\begin{aligned}
& I_{0} x_{-1}+d_{0} x_{0}+u_{0} x_{1}=b_{0} \\
& I_{1} x_{0}+d_{1} x_{1}+u_{1} x_{2}=b_{1} \\
& I_{2} x_{1}+d_{2} x_{2}+u_{2} x_{3}=b_{2}
\end{aligned}
$$

Special case of a band matrix


Fig. 11.9 A tridiagonal system of linear equations.

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## Other Types of Diagonal Matrices

Tridiagonal, pentadiagonal, . . . matrices arise in the solution of differential equations using finite difference methods

Matrices with more than three diagonals can be viewed as tridiagonal blocked matrices

| $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $\mathbf{x}$ | $\mathbf{x}$ | $\mathbf{x}$ |

A pentadiagonal matrix.


## Odd-Even Reduction

$I_{0} x_{-1}+d_{0} x_{0}+u_{0} x_{1}=b_{0} \quad$ Use odd equations to find odd-indexed
$l_{1} x_{0}+d_{1} x_{1}+u_{1} x_{2}=b_{1} \quad$ variables in terms of even-indexed ones
$I_{2} x_{1}+d_{2} x_{2}+u_{2} x_{3}=b_{2}$
$l_{3} x_{2}+d_{3} x_{3}+u_{3} x_{4}=b_{3}$

$$
\begin{aligned}
& d_{1} x_{1}=b_{1}-I_{1} x_{0}-u_{1} x_{2} \\
& d_{3} x_{3}=b_{3}-I_{3} x_{2}-u_{3} x_{4}
\end{aligned}
$$

Substitute in even equations to get a tridiagonal system of half the size

$$
\begin{aligned}
& L_{0} x_{-2}+D_{0} x_{0}+U_{0} x_{2}=B_{0} \\
& L_{2} x_{0}+D_{2} x_{2}+U_{2} x_{4}=B_{2} \\
& L_{4} x_{2}+D_{4} x_{4}+U_{4} x_{6}=B_{4}
\end{aligned}
$$

Sequential solution:
$T(m)=T(m / 2)+c m=2 c m$

The six divides are replaceable with one reciprocation per equation, to find $1 / d_{j}$ for odd $j$, and six multiplies

$$
\begin{aligned}
& L_{i}=-I_{i} I_{i-1} / d_{i-1} \\
& D_{i}=d_{i}-I_{i} u_{i-1} / d_{i-1}-u_{i} I_{i+1} / d_{i+1} \\
& U_{i}=-u_{i} u_{i+1} / d_{i+1} \\
& B_{i}=b_{i}-I_{i} b_{i-1} / d_{i-1}-u_{i} b_{i+1} / d_{i+1}
\end{aligned}
$$

## Architecture for Odd-Even Reduction



Fig. 11.10 The structure of odd-even reduction for solving a tridiagonal system of equations.

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## Odd-Even Reduction on a Linear Array



Fig. 11.11 Binary X-tree (with dotted links) and multigrid architectures.

Architecture of Fig. 11.10 can be modified to binary X-tree and then simplified to 2D multigrid

Communication time on linear array:

$$
\begin{aligned}
T(m) & =2(1+2+\ldots+m / 2) \\
& =2 m-2
\end{aligned}
$$



## Odd-Even Reduction on a 2D Mesh



Communication time on 2D mesh:
$T(m) \cong 2\left[2\left(1+2+\ldots+m^{1 / 2 / 2}\right)\right]$

$$
\cong 2 m^{1 / 2}
$$



### 11.4 Arbitrary System of Linear Equations

$2 x_{0}+4 x_{1}-7 x_{2}=3$
$3 x_{0}+6 x_{1}-10 x_{2}=4$
$-x_{0}+3 x_{1}-4 x_{2}=6$

$A x=b \quad$| $2 x_{0}+4 x_{1}-7 x_{2}=7$ |  |
| ---: | :--- |
| $3 x_{0}+6 x_{1}-10 x_{2}=8$ |  |
| $-x_{0}+3 x_{1}-4 x_{2}=$ | -1 |

Extended matrix $A^{\prime}=\left[\begin{array}{rrr|rr}2 & 4 & -7 & 3 & 7 \\ 3 & 6 & -10 & 4 & 8 \\ -1 & 3 & -4 & 6 & -1\end{array}\right] \begin{aligned} & \text { Divide row 0 by 2; } \\ & \begin{array}{l}\text { subtract } 3 \text { times } \\ \text { from row } 1 \\ \text { (pivoting oper) }\end{array}\end{aligned}$
Gaussian elimination

Extended matrix $A^{\prime}=\left(\begin{array}{rrrrr}1 & 2 & -3.5 & 1.5 & 3.5 \\ 0 & 0 & 0.5 & -0.5 & -2.5 \\ 0 & 5 & -7.5 & 7.5 & 2.5\end{array}\right)$
Extended matrix $A^{\prime}=\left(\begin{array}{rrrrr}1 & 0 & 0 & -2 & 0 \\ 0 & 1 & 0 & 0 & -7 \\ 0 & 0 & 1 & -1 & -5\end{array}\right)$
Repeat until identity matrix appears in first $n$ columns; read solutions from remaining columns

## Performing One Step of Gaussian Elimination



Fig. 11.12 A linear array performing the first phase of Gaussian elimination.

## Gaussian Elimination on a 2D Mesh



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## Matrix Inversion on a 2D Mesh



Fig. 11.14 Matrix inversion by Gaussian elimination.

## Jacobi Methods

| $2 x_{0}+4 x_{1}-7 x_{2}$ | $=3$ |
| ---: | :--- |
| $3 x_{0}+6 x_{1}-10 x_{2}$ | $=4$ |
| $-x_{0}+3 x_{1}-4 x_{2}$ | $=6$ |$\quad$ Ax $=b \quad$ Solution: | $x_{0}=-2$ |
| :--- |
| $x_{1}$ |$=0$

Use each equation to find one of the variables in terms of all others
$x_{0}=-2.000 x_{1}+3.500 x_{2}+1.500$
$x_{1}=-0.500 x_{0}+1.667 x_{2}+0.667$
$x_{2}=-0.250 x_{0}+0.750 x_{1}-1.500$
Iterate: Plug in estimates for the unknowns on the right-hand side to find new estimates on the left-hand side

Example: Estimate $x_{0}=1, x_{1}=1, x_{2}=1$

$$
\begin{aligned}
& x_{0}=-2.000+3.500+1.500=3.000 \\
& x_{1}=-0.500+1.667+0.667=1.834 \\
& x_{2}=-0.250+0.750-1.500=-1.000
\end{aligned}
$$



## Jacobi Relaxation and Overrelaxation

Jacobi relaxation: Assuming $a_{i j} \neq 0$, solve the $i$ th equation for $x_{i}$, yielding $m$ equations from which new (better) approximations to the answers can be obtained.

$$
x_{i}^{(t+1)}=\left(1 / a_{i j}\right)\left[b_{i}-\sum_{j \neq i} a_{i j} x_{j}^{(t)}\right] \quad x_{i}^{(0)}=\text { initial approximation for } x_{i}
$$

On an $m$-processor linear array, each iteration takes $O(m)$ steps.
The number of iterations needed is $\mathrm{O}(\log m)$ if certain conditions are satisfied, leading to $\mathrm{O}(m \log m)$ average time.

A variant: Jacobi overrelaxation

$$
x_{i}^{(t+1)}=(1-\gamma) x_{i}^{(t)}+\left(\gamma / a_{i j}\right)\left[b_{i}-\sum_{j \neq i} a_{i j} x_{j}^{(t)}\right] \quad 0<\gamma \leq 1
$$

For $\gamma=1$, the method is the same as Jacobi relaxation For smaller $\gamma$, overrelaxation may offer better performance

### 11.5 Graph Algorithms


$A=\left(\begin{array}{llllll}0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0\end{array}\right)$

$$
W=\left(\begin{array}{ccccc}
0 & 2 & 2 & \infty & 2 \\
1 & 0 & 2 & \infty & \infty \\
\infty & \infty & 0 & -3 & \infty \\
\infty & \infty & \infty & 0 & 0 \\
1 & \infty & \infty & \infty & 0
\end{array}\right)
$$

Fig. 11.15 Matrix representation of directed graphs.

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## Transitive Closure of a Graph

$$
\begin{array}{ll}
A^{0}=I & \text { Paths of length } 0 \text { (identity matrix) } \\
A^{1}=A & \text { Paths of length } 1 \\
A^{2}=A \times A & \text { Paths of length } 2 \\
A^{3}=A^{2} \times A & \text { Paths of length } 3
\end{array} \text { etc. }
$$



Compute "powers" of $A$ via matrix multiplication, but use AND/OR in lieu of multiplication/addition

Transitive closure of $G$ has the adjacency matrix

$$
A^{*}=A^{0}+A^{1}+A^{2}+\ldots
$$

$$
A=\left(\begin{array}{llllll}
0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 1 \\
0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0
\end{array}\right)
$$

$A_{i j}^{*}=1$ iff node $j$ is reachable from node $i$
Powers need to be computed up to $A^{n-1}$ (why?)

## Graph $G$ with adjacency matrix $A$

## Transitive Closure Algorithm

Initialization: Insert the edges ( $i, i$ ), $0 \leq i \leq n-1$, into the graph
Phase 0 Insert the edge ( $i, j$ ) into the graph if $(i, 0)$ and $(0, j)$ are in the graph

Phase 1 Insert the edge $(i, j)$ into the graph if $(i, 1)$ and $(1, j)$ are in the graph

Phase $k$ Insert the edge $(i, j)$ into the graph if $(i, k)$ and $(k, j)$ are in the graph [Graph $A^{(k)}$ then has an edge $(i, j)$ iff there is a path from $i$ to $j$ that goes only through nodes $\{1,2, \ldots, k\}$ as intermediate hops]

Phase $n-1 \quad$ Graph $A^{(n-1)}$ is the answer $A^{*}$


Graph G with adjacency matrix $A$

## Transitive Closure on a 2D Mesh

The key to the algorithm is to ensure that each phase takes constant time; overall $\mathrm{O}(n)$ steps. This would be optimal on an $n \times n$ mesh because the best sequential algorithm needs $\mathrm{O}\left(n^{3}\right)$ time.


Initially



Row 2


Graph G with adjacency matrix $A$

Fig. 11.16 Transitive closure algorithm on a 2D mesh.
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## Elimination of Broadcasting via Retiming



Example of systolic retiming by delaying the inputs to $\mathrm{C}_{\mathrm{L}}$ and advancing the outputs from $\mathrm{C}_{\mathrm{L}}$ by $d$ units [Fig. 12.8 in Computer Arithmetic: Algorithms and Hardware Designs, by Parhami, Oxford, 2000]



## Systolic Retiming for Transitive Closure

Add $2 n-2=6$ units of delay to edges crossing cut 1
Move 6 units of delay from inputs to outputs of node $(0,0)$

Fig. 11.17 Systolic retiming to eliminate broadcasting.


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### 11.6 Image Processing Algorithms

Labeling connected components in a binary image (matrix of pixels)


The reason for considering diagonally adjacent pixels parts of the same component.


Worst-case component showing that a naïve "propagation" algorithm may require $\mathrm{O}(p)$ time.

## Recursive Component Labeling on a 2D Mesh

| $C_{0}$ |
| :--- |
| 1 |$|$| 1 | 0 | 1 | 1 | 0 | 1 | 1 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

Fig. 11.18 Connected components in an $8 \times 8$ binary image.

$\mathrm{C}_{3}$| $1_{0}$ | $1_{0}$ | 0 | $1_{3}$ | $1_{4}$ | 0 | $1_{4}$ | $1_{4}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | $1_{0}$ | 0 | $1_{3}$ | 0 | $1_{4}$ | 0 | $1_{4}$ |
| $1_{0}$ | 0 | 0 | 0 | $1_{4}$ | 0 | 0 | 0 |
| $1_{0}$ | 0 | $1_{26}$ | $1_{26}$ | 0 | $1_{4}$ | $1_{4}$ | $1_{4}$ |
| 0 | 0 | 0 | 0 | $1_{36}$ | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | $1_{36}$ | 0 | 0 | $1_{47}$ |
| $C_{47}$ | $0_{0}$ | $1_{49}$ | 0 | 0 | $1_{36}$ | 0 | $1_{47}$ |
| 0 | $1_{47}$ |  |  |  |  |  |  |
| $1_{49}$ | $1_{49}$ | 0 | 0 | 0 | 0 | 0 | $1_{47}$ |

Fig. 11.19 Finding the connected components via divide and conquer.

$$
T(p)=T(p / 4)+\mathrm{O}\left(p^{1 / 2}\right)=\mathrm{O}\left(p^{1 / 2}\right)
$$

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## Analysis and Proof of Levialdi's Algorithm


0 is changed to 1 if $N=W=1$
$\begin{array}{ll}0 & 1 \\ 0 & 1 \\ 0 & 1 \\ \text { if } N=W=N W & N\end{array}$
Figure 11.20
Transformation or rewriting rules for Levialdi's algorithm in the shrinkage phase (no other pixel changes).
Latency of Levialdi's algorithm
$T(n)=2 n^{1 / 2}-1\{$ shrinkage $\}+2 n^{1 / 2}-1$ \{expansion $\}$

| $x$ | 1 | $y$ | Component do not merge in shrinkage phase <br> Consider a 0 that is about to become a 1 |
| :--- | :--- | :--- | :--- |
| 1 | 0 | $y$ | If any $y$ is 1, then already connected <br> If $z$ is 1 then it will change to 0 unless |
| $y$ | $y$ | $z$ | at least one neighboring $y$ is 1 |

## 12 Mesh-Related Architectures

Study variants of simple mesh and torus architectures:

- Variants motivated by performance or cost factors
- Related architectures: pyramids and meshes of trees

```
Topics in This Chapter
12.1 Three or More Dimensions
12.2 Stronger and Weaker Connectivities
12.3 Meshes Augmented with Nonlocal Links
12.4 Meshes with Dynamic Links
    12.5 Pyramid and Multigrid Systems
    12.6 Meshes of Trees
```



### 12.1 Three or More Dimensions

$$
\begin{array}{ll}
3 \mathrm{D} \text { vs } 2 \mathrm{D} \text { mesh: } & D=3 p^{1 / 3}-3 \text { vs } 2 p^{1 / 2}-2 ; B=p^{2 / 3} \text { vs } p^{1 / 2} \\
\text { Example: } & \text { 3D } 8 \times 8 \times 8 \text { mesh } \quad p=512, D=21, B=64 \\
& 2 D 22 \times 23 \text { mesh } \quad p=506, D=43, B=23
\end{array}
$$



Fig. 12.1 3D and 2.5D physical realizations of a 3D mesh.

## More than Three Dimensions?

2.5D and 3D packaging technologies 4D, 5D, ... meshes/tori: optical links?

## PC board


(b) 3D packaging of the future
$q \mathrm{D}$ mesh with $m$ processors along each dimension: $p=m^{q}$
Node degree
$d=2 q$
Diameter
$D=q(m-1)=q\left(p^{1 / q}-1\right)$
Bisection width: $\quad B=p^{1-1 / q}$ when $m=p^{1 / q}$ is even $q \mathrm{D}$ torus with $m$ processors along each dimension $=m$-ary $q$-cube

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## Sorting on a 3D Mesh

Time for Kunde's algorithm
$=4 \times(2 \mathrm{D}$-sort time $)+2$
$\cong 16 p^{1 / 3}$ steps
Defining the zyx processor ordering


A variant of shearsort is available, but Kunde's algorithm is faster and simpler

Sorting on 3D mesh (zyx order; reverse of node index)
Phase 1: Sort elements on each zx plane into zx order Phase 2: Sort elements on each yz plane into zy order Phase 3: Sort elements on each xy layer into yx order (odd layers sorted in reverse order)
Phase 4: Apply 2 steps of odd-even transposition along z Phase 5: Sort elements on each xy layer into $y x$ order

## Routing on a 3D Mesh

Time for sort-based routing
= Sort time + Diameter
$\cong 19 p^{1 / 3}$ steps
As in 2D case, partial sorting can be used


Simple greedy algorithm does fine usually, but sorting first reduces buffer requirements

Greedy zyx (layer-first, row last) routing algorithm
Phase 1: Sort into zyx order by destination addresses
Phase 2: Route along $z$ dimension to correct $x y$ layer
Phase 3: Route along $y$ dimension to correct column
Phase 4: Route along $x$ dimension to destination

## Matrix Multiplication on a 3D Mesh

A total of $\left(m^{1 / 4}\right)^{3}$ $=m^{3 / 4}$ block multiplications are needed

Matrix blocking for multiplication on a 3D mesh


$\mathrm{m}^{9 / 4}$ processors

Assume the use of an $m^{3 / 4} \times m^{3 / 4} \times m^{3 / 4}$ mesh with $p=m^{9 / 4}$ processors
Each $m^{3 / 4} \times m^{3 / 4}$ layer of the mesh is assigned to one of the $m^{3 / 4} \times m^{3 / 4}$ matrix multiplications ( $m^{3 / 4}$ multiply-add steps)

The rest of the process can take time that is of lower order
Optimal: Matches sequential work and diameter-based lower bound

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## Low- vs High-Dimensional Meshes

There is a good match between the structure of a 3D mesh and communication requirements of physical modeling problems

| $6 \times 6$ mesh emulating $3 \times 3 \times 3$ mesh (not optimal) | Middle layer | Upper layer |
| :---: | :---: | :---: |
|  | Lower layer |  |



A low-dimensional mesh can efficiently emulate a high-dimensional one
Question: Is it more cost effective, e.g., to have 4-port processors in a 2D mesh architecture or 6-port processors in a 3D mesh architecture, given that for the 4-port processors, fewer ports and ease of layout allow us to make each channel wider?

### 12.2 Stronger and Weaker Connectivities




Node i connected to $\mathrm{i} \pm 1$, $i \pm 7$, and $i \pm 8(\bmod 19)$.

Fortified meshes and other models with stronger connectivities:

Eight-neighbor Six-neighbor

Triangular Hexagonal

Fig. 12.2 Eight-neighbor and hexagonal (hex) meshes.
As in higher-dimensional meshes, greater connectivity does not automatically translate into greater performance

Area and signal-propagation delay penalties must be factored in

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## Simplification via Link Orientation

Two in- and out-channels per node, instead of four

Some shortest paths become longer, however


With even side lengths, the diameter does not change

Can be more cost-effective than 2D mesh

Figure 12.3 A $4 \times 4$ Manhattan street network.


Figure 12.4 A pruned $4 \times 4 \times 4$ torus with nodes of degree four [Kwai97].


Honeycomb torus

Pruning a high-dimensional mesh or torus can yield an architecture with the same diameter but much lower implementation cost

## Simplification via Link Sharing



Fig. 12.5 Eight-neighbor mesh with shared links and example data paths.
Factor-of-2 reduction in ports and links, with no performance degradation for uniaxis communication (weak SIMD model)

### 12.3 Meshes Augmented with Nonlocal Links

Motivation: Reduce the wide diameter (which is a weakness of meshes)

Increases max
 node degree and hurts the wiring locality and regularity


Fig. 12.6 Three examples of bypass links along the rows of a 2 D mesh.


## Using a Single Global Bus



The single bus increases the bisection width by 1 , so it does not help much with sorting or other tasks that need extensive data movement

Fig. 12.7 Mesh with a global bus and semigroup computation on it.
Semigroup computation on 2D mesh with a global bus
Phase 1: Find partial results in $p^{1 / 3} \times p^{1 / 3}$ submeshes in $O\left(p^{1 / 3}\right)$ steps; results stored in the upper left corner of each submesh
Phase 2: Combine partial results in $O\left(p^{1 / 3}\right)$ steps, using a sequential algorithm in one node and the global bus for data transfers
Phase 3: Broadcast the result to all nodes (one step)

## Mesh with Row and Column Buses



The bisection width doubles, so row and column buses do not fundamentally change the performance of sorting or other tasks that need extensive data movement

Fig. 12.8 Mesh with row/column buses and semigroup computation on it.

## Semigroup computation on 2D mesh with row and column buses

Phase 1: Find partial results in $p^{1 / 6} \times p^{1 / 6}$ submeshes in $O\left(p^{1 / 6}\right)$ steps
Phase 2: Distribute $p^{1 / 3}$ row values left among the $p^{1 / 6}$ rows in same slice
Phase 3: Combine row values in $p^{1 / 6}$ steps using the row buses
Phase 4: Distribute column-0 values to $p^{1 / 3}$ columns using the row buses
Phase 5: Combine column values in $p^{1 / 6}$ steps using the column buses
Phase 6: Distribute $p^{1 / 3}$ values on row 0 among $p^{1 / 6}$ rows of row slice 0
Phase 7: Combine row values in $p^{1 / 6}$ steps
Phase 8: Broadcast the result to all nodes (2 steps)

### 12.4 Meshes with Dynamic Links



Fig. 12.9 Linear array with a separable bus using reconfiguration switches.
Semigroup computation in $O(\log p)$ steps; both 1D and 2D meshes

$\{\mathrm{N}\}\{\mathrm{E}\}\{\mathrm{W}\}\{\mathrm{S}\}$


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Various subsets of processors (not just rows and columns) can be configured, to communicate over shared buses

Fig. 12.10 Some processor states in a reconfigurable mesh.

## Programmable Connectivity in FPGAs



Interconnection switch with 8 ports and four connection choices for each port:
0 - No connection
1 - Straight through
2 - Right turn
3 - Left turn
8 control bits (why?)


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## An Array Reconfiguration Scheme

3-state $2 \times 2$ switch


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## Reconfiguration of Faulty Arrays



Question: How do we know which cells/nodes must be bypassed?


Must devise a scheme in which healthy nodes set the switches

### 12.5 Pyramid and Multigrid Systems

Faster than mesh for semigroup computation, but not for sorting or arbitrary routing


Fig. 12.11 Pyramid with 3 levels and $4 \times 4$ base along with its 2D layout.
Originally developed for image processing applications
Roughly $3 / 4$ of the processors belong to the base
For an $l$-level pyramid: $\quad D=2 l-2 \quad d=9 \quad B=2^{\prime}$

## Pyramid and 2D Multigrid Architectures



Fig. 12.12 The relationship between pyramid and 2D multigrid architectures.

Multigrid architecture is less costly and can emulate the pyramid architecture quite efficiently


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### 12.6 Meshes of Trees

$2 m$ trees, each with $m$ leaves, sharing leaves in the base


Row and column roots can be combined into $m$ degree- 4 nodes


Fig. 12.13 Mesh of trees architecture with 3 levels and a $4 \times 4$ base.

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## Alternate Views of a Mesh of Trees



2D layout for mesh of trees network with a $4 \times 4$ base; root nodes are in the middle row and column


Fig. 12.14 Alternate views of the mesh of trees architecture with a $4 \times 4$ base.

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## Simple Algorithms for Mesh of Trees

Semigroup computation: row/column combining


Sorting $m$ keys stored in merged roots: broadcast $x_{i}$ to row $i$ and column $i$, compare $x_{i}$ to $x_{j}$
in leaf ( $i, j$ ) to set a flag, add flags in column trees broadcast $x_{i}$ to row $i$ and column $i$, compare $x_{i}$ to $x_{j}$
in leaf $(i, j$ ) to set a flag, add flags in column trees to find the rank of $x_{i}$, route $x_{i}$ to node $\operatorname{rank}\left[x_{i}\right]$ Parallel prefix computation: similar
Routing $m^{2}$ packets, one per processor on the $m \times m$ base: requires $\Omega(m)=\Omega\left(p^{1 / 2}\right)$ steps
In the view of Fig. 12.14, with only $m$ packets to be routed from one side of the network to the other, $2 \log _{2} m$ steps are required, provided destination nodes are distinct
Sorting $m^{2}$ keys, one per processor on the $m \times m$ base: emulate any mesh sorting algorithm

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## Some Numerical Algorithms for Mesh of Trees

Matrix-vector multiplication $A x=y$ ( $A$ stored on the base and vector $x$ in the column roots, say; result vector $y$ is obtained in the row roots): broadcast $x_{j}$ in the $j$ th column tree, compute $a_{i j} x_{j}$ in base processor ( $i, j$ ), sum over row trees

Convolution of two vectors: similar


Column tree (only one shown)

Diagonal trees


Fig. 12.15 Mesh of trees variant with row, column, and diagonal trees.

## Minimal-Weight Spanning Tree Algorithm

Greedy algorithm: in each of at most $\log _{2} n$ phases, add the minimal-weight edge that connects a component to a neighbor


Supernode 1


Sequential algorithms, for an $n$-node, $e$-edge graph:

Kruskal's: $\mathrm{O}(e \log e)$
Prim's (binary heap):

$$
\mathrm{O}((e+n) \log n)
$$

Both of these algorithms are $\mathrm{O}\left(n^{2} \log n\right)$ for dense graphs, with $e=\mathrm{O}\left(n^{2}\right)$

Prim's (Fibonacci heap):
$\mathrm{O}(e+n \log n)$, or
$\mathrm{O}\left(n^{2}\right)$ for dense graphs

Fig. 12.16 Example for min-weight spanning tree algorithm.
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## MWST Algorithm on a Mesh of Trees

The key to parallel version of the algorithm is showing that each phase can be done in $\mathrm{O}\left(\log ^{2} n\right)$ steps; $\mathrm{O}\left(\log ^{3} n\right)$ overall

Row tree (one per row)

Leaf $(i, j)$ holds the weight $W(i, j)$ of edge $(i, j)$ and "knows" whether the edge is in the spanning tree, and if so, in which supernode. In each phase, we must:
a. Find the min-weight edge incident to each supernode
b. Merge supernodes for next phase

Subphase a takes $O(\log n)$ steps Subphase b takes $O\left(\log ^{2} n\right)$ steps

Fig. 12.17 Finding the new supernode ID when several supernodes merge.


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