Design Methodologies for 3D Mixed Signal Integrated Circuits: a Practical 12-bit SAR ADC Design Case

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ABSTRACT

Three-dimensional (3D) integration technology has been proposed as a promising technology to provide small footprint, reduced wirelength, and the capability of heterogeneous integration. In particular, 3D IC is a good candidate to address the design issues in conventional analog/digital mixed-signal IC designs. In this work, we focus on modeling and analyzing the impacts of through silicon vias (TSVs) on mixed-signal ICs. Based on the analysis, a set of design methodologies for 3D mixed-signal ICs are proposed. The design methodologies are verified with a case study, in which a 12-bit successive approximation register analog-to-digital converter (SAR ADC) is re-designed by partitioning it into three stacked layers for 3D integration. The experimental results show that, compared to the traditional 2D counterpart, our 3D SAR ADC with optimized TSV placement can achieve significant area and power reduction, and performance improvement. Specifically, due to the isolation of substrate noise disturbance in our 3D design, the signal-to-noise-plus-distortion ratio (SNDR) is improved from 68.74 dB to 74.12 dB.

1. INTRODUCTION

Three-dimensional (3D) ICs have been proposed as a promising technology for future IC designs. For a 3D chip, multiple dies can be stacked together with various vertical interconnect techniques, such as through-silicon-via (TSV), inductive or capacitive coupling, and wire-bonding. Consequently, 3D ICs show significant advantages over traditional two-dimensional (2D) designs, which include and are not limited to: 1) reduced wire length on global interconnects; 2) smaller footprint due to the increasing cell density; and 3) heterogeneous integration of mixed-technology dies [1].

The characteristics of 3D stacking in shortening the global interconnects, increasing the bandwidth between dies, and shrinking the footprint have been well studied in previous works [1, 2, 3], which mainly focus on digital IC design. Meanwhile, another advantage of 3D stacking, heterogeneous integration, has not been fully exploited. In particular, 3D heterogeneous die-stacking technology provides a promising solution to alleviate many issues exposed in the traditional 2D mixed-signal ICs by separating digital and analog circuits onto different dies as shown in Figure 1. The advantages of 3D stacking of mixed-signal ICs can be summarized as: 1) ideally eliminating the switching noise disturbance due to the shared substrate in the 2D case, and therefore avoiding the unnecessary guard rings or deep well process; 2) elevating the performance and reducing the power consumption of digital circuit by applying different process technologies to digital and analog designs, respectively (e.g., a 32nm digital design can be stacked with a 90nm analog design); 3) also shrinking the concerned footprint and shortening the length of global interconnects.

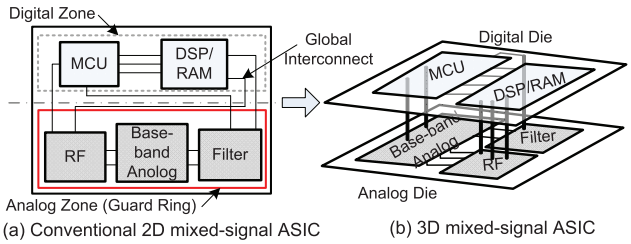

Figure 1: 2D and 3D mixed-signal ASIC architectures

Even though 3D ICs are able to provide great benefits for mixed-signal applications, there are still several challenges in this area. Specifically, in order to fully exploit the potential of 3D heterogeneous integration, the impact of vertical carriers (TSVs in this work) on the mixed-signal system should be carefully evaluated. In addition, it is unclear how to optimize the TSVs for the mixed-signal design to achieve proper trade-offs among performance, power, and area.

In this work, we focus on modeling and analyzing the impact of TSVs on mixed-signal ICs. Based on the analysis, a set of design guidelines for 3D mixed-signal ICs are proposed. The proposed design methodologies are verified with a case study, in which a 12-bit successive approximation register analog-to-digital converter (SAR ADC) is re-designed by partitioning it into three stacked layers for 3D integration. In general, the contributions of this work can be summarized as follows.

- We analyze and model three types of TSV-induced effects on mixed-signal systems, TSV-to-metal layer, TSV-to-TSV, and TSV-to-active device. The sensitivity of these three types of TSV impacts to the analog/mixed-signal modules is also analyzed in this work.
- Based on the models and analysis of TSV-induced impacts on mixed-signal ICs, we propose a few design guidelines for 3D mixed-signal IC design.
- We design a practical three-layer stacked ADC through fully exploiting the potential of 3D heterogeneous integration.

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The rest of the paper is organized as follows. Section 2 shows the related work. Section 3 presents three models for TSV's effects and analyzes the sensitivity of these effects to analog/mixed-signal modules. The design methodologies about how to optimize the TSVs in mixes-signal ICs are described in Section 4. Section 5 shows our 3D SAR ADC design and the corresponding evaluation results. Finally, the paper is concluded in Section 6.

2. RELATED WORK

Related Work on 3D IC Design. Recently, many work has been done to explore 3D IC design space and several 3D prototype chips have been unveiled as the demonstration. Most of these 3D IC designs [2, 3, 4, 5, 6, 7, 8] can be classified into two categories: 1) 3D digital IC designs [2, 3, 4, 5] by stacking memory or logic onto several layers and 2) 3D sensor node designs by stacking a sensor layer onto the processor layer [6, 7, 8]. Very littel has been done for 3D analog or mixed-signal design.

Related Work on TSV Modeling and 2D Mixed-signal IC Design. There are also several work on analyzing the TSV-induced impacts on 3D ICs. the TSV-to-TSV coupling effects in device or full-chip level have been studied [9, 10, 11]. For example, the noise coupling effect between TSVs and active circuits has been studied [12]. Those studies, however, only address an individual TSV-induced coupling effect, and only in digital circuits. Compared with digital circuit, the analog circuits behave differently with respect to various TSV-induced coupling effects. A much more comprehensive analysis, therefore, is necessary and essential for TSV-based 3D mixed-signal ICs.

In this work, an SAR ADC is re-designed as a case study for 3D mixed-signal circuitry. The SAR ADC is suitable for applications with moderate speed/resolution, flexible reconfigurability, and very low power consumption. Two designs of low-power SAR ADCs (3.8μW at 1V and 11.5μW at 1.8V) are proposed recently by Agnes et al. [13]. An ultra low power (25μW at 1V) 12-bit rate-resolution scalable SAR ADC is proposed by Verma et al. [14]. All of these designs can achieve very low power but with undesirable SNDR and effective number of bits (ENOB). In contrast, a 12-bit 0.1MS/s SAR ADC with on-chip self-calibration is proposed by Fan et al. [15], which can achieve high spurious free dynamic range (SFDR), high ENOB, and linearity, but suffers from the relatively high power consumption. In this work, we leverage the architecture proposed by Fan et al. [15] as the baseline to evaluate the performance improvement and power reduction of 3D mixed-signal IC design.

3. MODELING OF TSV-INDUCED IMPACT ON MIXED-SIGNAL IC

Compared with the conventional 2D mixed-signal ICs, the major difference of 3D stacked mixed-signal circuits is the impact of vertical interconnects (through-silicon-via or TSVs). Although prior work [9, 10, 11] has been done to model the behavior of TSVs in the digital case, the TSV-induced effects on analog/mixed-signal ICs have not been fully studied. The components in the TSV-based 3D analog/mixed-signal ICs can be classified into three categories:1) the interconnects and the passive devices designed with the metal layers, such as resistors, inductors, and capacitors; 2) the TSVs; 3) the active devices fabricated on the substrate, such as the transistors and diodes. Therefore, the TSV-induced impacts on the analog/mixed-signal ICs mainly involve the TSV-to-metal layers, the TSV-to-TSV, and the TSV-to-active devices couplings. In this section, we describe the models for the coupling effects between TSVs and other components [9, 10, 12].

3.1 TSV-to-metal layer coupling effect

In analog/mixed-signal IC design, there are great amounts of passive devices, such as resistors, capacitors, and inductors, which are usually designed with top metal layers. Simultaneously, due to the big size of TSVs, a bottom metal layer (M1) with much larger wire width than the traditional metal layer is bonded to the top of TSVs. When the passive devices located on the analog die are controlled by some digital logic on the other die through TSVs, it will introduce extra parasitic capacitance and resistance between M1 and the passive devices as shown in Figure 2. Note that compared with the parasitic capacitance between M1 and top metal layers, the direct capacitive coupling between the TSVs and the top metal layers is negligible.

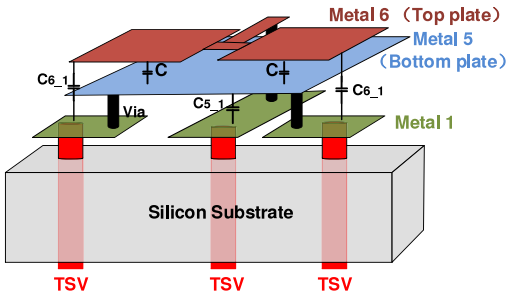

Figure 2: The coupling effect among TSVs and metal layers: as an example, a capacitor array with 2C capacitance, which is consisted of two parallel-connected unit capacitor with capacitance of C, is controlled through TSVs for charging/discharging

When two different metal layers are not via-connected and have overlap areas, there is parasitic capacitance between these two metal layers. In general, the capacitor consisted of M1 and the top metal layers is filled with multiple different dielectric materials. The parasitic capacitance (resistance) between the top metal layer and M1 can be modeled as a series-connected capacitors (metal vias) [16]. We can use the following formulas to calculate the parasitic capacitance and resistance between the top metal layers and M1:

$$\frac{1}{C_{M_i\_M_1}} = \frac{1}{C_{M_2\_M_1}} + \frac{1}{C_{M_3\_M_2}} + \cdots + \frac{1}{C_{M_i\_M_{i-1}}}, \quad (1)$$

$$C_{M_i\_M_{i-1}} = \frac{\varepsilon_{i\_i-1} \times \varepsilon_0 \times A_{overlap}}{d_{i\_i-1}}, \quad (2)$$

$$R_{M_i\_M_1} = Rvia_{M_2\_M_1} + Rvia_{M_3\_M_2} + \cdots + Rvia_{M_i\_M_{i-1}}, \quad (3)$$

where ε_{i_i-1} and d_{i_i-1} are the dielectric constant and thickness of the insulator between metal layer i and metal layer $i-1$, respectively; $Rvia_{M_i\_M_{i-1}}$ is the parasitic resistance of the via connecting metal layer i and metal layer $i-1$. $A_{overlap}$ defines the overlap area between M1 and top metal layers.

3.2 TSV-to-TSV coupling effect

In 3D ICs, the coupling effect between two adjacent TSVs could be significant because of the big size of TSVs. For digital ICs, this TSV-to-TSV coupling effect could lead to logic errors or timing violations and cause extra power consumptions [17]. For analog/mixed-signal ICs, the TSV-to-TSV coupling effect, however, has not been fully evaluated, which could cause coupling noise disturbance and degrade the performance of sensitive analog devices. Generally, the noise-sensitive devices or interconnects need to be shielded by ground in the traditional analog/mixed-signal IC designs, which easily leads to one signal TSV surrounded by several grounded TSVs as shown in Figure 3.

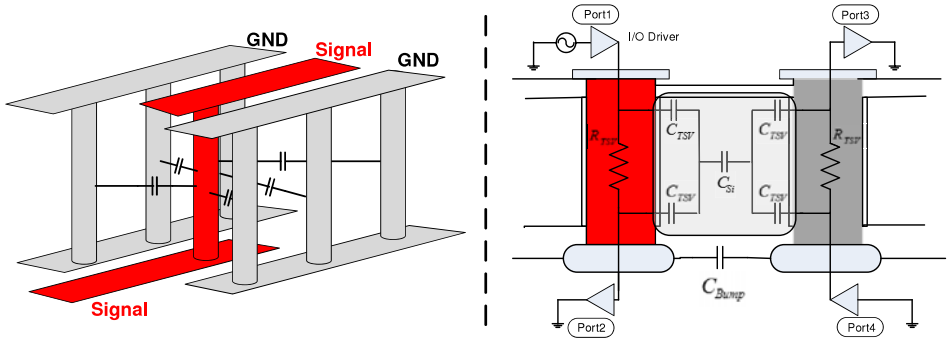

Figure 3: The Coupling effect between TSVs

In this work, we model the two coupled TSVs according to the lumped circuit model proposed earlier [9, 10]. We use the following simplified formulas to calculate the capacitances and the resistances:

$$C_{TSV} = \frac{1}{4}\frac{2\pi\varepsilon_0\varepsilon_r}{\ln(\frac{r_{TSV}+t_{OX}}{r_{TSV}})} \times l_{TSV}, \quad (4)$$

$$C_{si} = \varepsilon_0\varepsilon_{si}\frac{2(r_{TSV}+t_{OX})+\alpha}{d} \times l_{TSV}, \quad (5)$$

$$C_{Bump} = \frac{\varepsilon_0\varepsilon_r}{d-2r_{Bump}} \times \pi \times r_{Bump} \times l_{Bump}, \quad (6)$$

$$R_{TSV} = \frac{l_{TSV}}{\sigma\pi r_{TSV}^2}, \quad (7)$$

$$R_{Si} = \frac{\varepsilon_{si}}{C_{si}\sigma}, \quad (8)$$

where r_{TSV} and l_{TSV} are the TSV radius and height respectively, r_{Bump} and l_{Bump} are the radius and height of a bump, t_{OX} is the thickness of the insulator, ε_0 and ε_{si} are the dielectric constant of vacuum and silicon, α is the scaling factor, and d is the distance between two TSVs.

3.3 TSV-to-active device coupling effect

As Figure 4 shows, a SiO_2 insulation layer is formed between the TSV and the highly conductive silicon substrate [12] to isolate the DC leakage, which results in large parasitic capacitance. Therefore, there will be a transmission path for the high frequency coupling noise between the substrate and TSV, which degrades circuit performance. As illustrated in Figure 4, the TSV-to-active device coupling effect should be carefully modeled to evaluate this impact in 3D mixed-signal IC designs.

In this work, we simplify the TSV-to-active device coupling model proposed earlier [12], which mainly consists of two parts: 1) the model of an isolated TSV, and 2) the model of substrate. The parameters of an isolated TSV, C_{TSV}, R_{TSV} have been described in Section 3.2. The substrate can be divided into several cubes as proposed earlier [12]. w_{sub}, l_{sub}, and h_{sub} represent the width, length, and height of a substrate cube, respectively. In this way, the detailed parameters of the TSV-to-active device model shown in Figure 4 can be calculated according to the following equations:

$$C_{sub1} = C_{sub2} = \varepsilon_{si}\frac{h_{sub} \times l_{sub}}{w_{sub}}, \quad (9)$$

$$R_{sub1} = R_{sub2} = \frac{1}{\rho_{si}}\frac{w_{sub}}{h_{sub} \times l_{sub}}, \quad (10)$$

$$C_{sub3} = \varepsilon_{si}\frac{w_{sub} \times l_{sub}}{h_{sub}}, \quad (11)$$

$$R_{sub3} = \frac{1}{\rho_{si}}\frac{h_{sub}}{w_{sub} \times l_{sub}}. \quad (12)$$

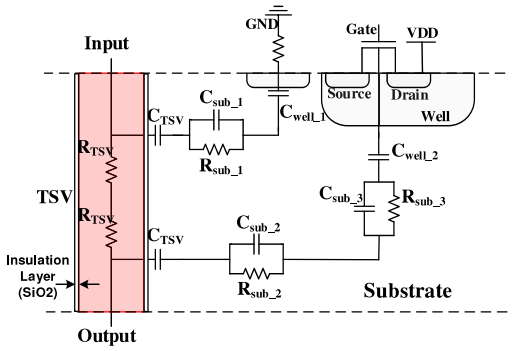

Figure 4: Modelling the coupling effect among TSVs and active devices

4. ANALYSIS OF TSV-INDUCED IMPACTS AND OPTIMIZATION OF TSV PLACEMENT

In this section, the TSV coupling models described in Section 3 are applied to design cases to explore design methodologies for 3D mixed-signal ICs.

4.1 Analysis of TSV-to-metal layer coupling effect

As illustrated in Section 3.1, the "large" bonding metal (M1) causes extra coupling effect to the passive devices or interconnects in analog/mixed-signal IC designs. In order to explore this effect, we apply the TSV-to-metal layer coupling model presented in Section 3.1 into a practical small design case: a capacitor array with 2C capacitance consisted of two parallel-connected unit capacitor with capacitance of C as shown in Figure 2. The top and bottom plates of this capacitor are designed with metal layer 6 (M6) and metal layer 5 (M5), respectively. One TSV is utilized to connect the top plate, and other two TSVs are utilized to connect the bottom plate. Assigning different signals to these TSVs can control the charging and discharging pattern of this capacitor.

Placing the TSVs far away from the passive devices can reduce the coupling effect between M1 and the top metal layers (M5, M6), which however can lead to area overhead. Figure 5 shows the calculated trade-off between the mismatch of the capacitor array and the area overhead.

Design Guideline (I): For the applications of placing TSVs under passive devices with larger area, reducing the overlap area

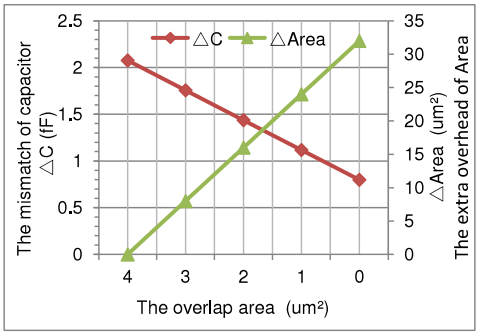

Figure 5: The trade-off between mismatch of the capacitor array and the area overhead

between M1 and passive device layers can well alleviate the mismatch issue (ΔC) for the passive devices, such as the mismatch-sensitive capacitor array in the sampling circuits. Meanwhile, the area overhead ($\Delta Area$) needs to be balanced in the area limited analog/mixed-signal IC designs.

4.2 Analysis of TSV-to-TSV coupling effect

The structure shown in Figure 3 is used as an example to analyze the coupling effect between adjacent TSVs in mixed-signal ICs. In this structure, one signal TSV is surrounded by six victim ground TSVs. In the digital case, Liu et al [17] claimed that the latency of a signal through the TSV can be reduced by 65% if the distance between two adjacent TSVs is increased from $11um$ to $100um$. For analog/mixed-signal ICs, we mainly focus on the noise induced by the TSV-to-TSV coupling effect.

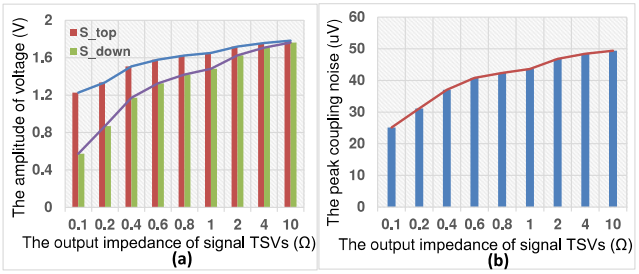

Figure 6: The impact of output impedance for one signal TSV with six coupled victim TSVs: (a) The voltage difference between the input and output of signal TSVs, S_top, S_{down}, with the variation of the output impedance of the signal TSV; (b) the peak coupling noise at the input/output port of ground TSVs with the variation of the output impedance of signal TSVs

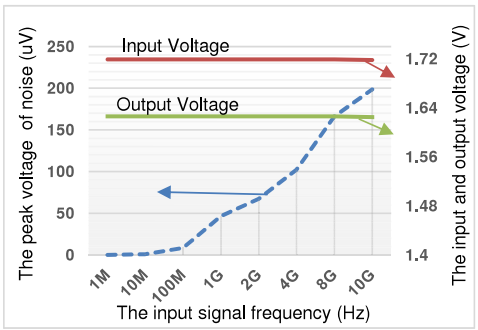

Figure 7: The impact of frequency for one signal TSV with six coupled victim TSVs

We apply a 1 GHz square wave source at the signal TSV input port as shown in Figure 3. By varying the output impedance of the signal TSV, we can find that the voltage amplitude across the TSV is inversely proportional to its output impedance, as shown in Figure 6 (a). when the output impedance of one signal TSV is 10 Ω, the voltage division due to the TSV-to-TSV coupling effect is negligible. The coupling noise in the ground TSVs, however, becomes much more severe with increasing output impedance of the signal TSV as shown in Figure 6(b), which means that the ground is not an ideal "0". In order to explore the frequency characteristic of the TSV-to-TSV coupling effect, we change the frequency of input signal from 1 Mhz to 10 Ghz while fixing the output impedance of the signal TSV at 2 Ω. The simulation result is shown in Figure 7. For the high-frequency signal, the input and output voltages of the signal TSV have little variation. However, the coupling noise in the ground TSVs is aggravated rapidly with the increase of signal frequency.

Design Guideline (II): For the applications of placing ground wires with multiple ground TSVs as the shielder, when the mixed-signal ICs are sensitive to the voltage variation, the voltage division effect induced by TSVs coupling can be alleviated by enlarging the output impedance of signal TSVs. While for the ground noise-sensitive circuits, the output impedance of signal TSVs should be downsized.

Design Guideline (III): For the high-frequency signal, when the analog/mixed-signal ICs are sensitive to the ground noise, the TSVs coupling induced ground noise should be alleviated by increasing the distance between the signal TSV and victim ground TSVs.

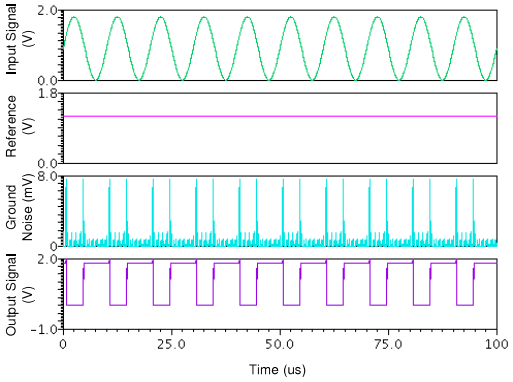

Figure 8: The coupling effect between TSVs and a comparator

4.3 Analysis of TSV-to-active device coupling effect

As stated in Section 3.3, there will be a high frequency noise transmission path between the TSVs and the grounded substrate if a signal TSV is placed close to the sensitive analog device as shown in Figure 4. The substrate therefore is no longer ideal '0' and may degrade the circuit performance. In this work, we take a comparator [15] as an example to analyze the impact of TSV-to-active device coupling effect on the analog/mixed-signal ICs. The original comparator has five input ports: the signal sampling port, the reference voltage port, the clock port CLK, the power source VDD, and the ground GND. Besides, there is also one output port that is for generating the comparing result. In this case, we supply the input signals through TSVs, and the TSV-to-active device coupling model presented in Section 3.3 is implemented. As shown in Figure 8, the peak coupling noise in the ground port of the comparator is 8 mV, which appears at the rising/falling edge of the comparator output signal.

Design Guideline (IV): For the applications of feeding signals through TSVs to the noise-sensitive active device, the coupling effect between a higher frequency signal TSV and the active device dominates the coupling noise in the ground. Therefore, the distance between the higher frequency TSVs and the noise-sensitive devices should be carefully designed to make trade-off among accuracy, area, and speed.

5. CASE STUDY

We implemented a 12-bit SAR ADC as a case study. The architecture and 3D physical implementation are shown in this section.

5.1 12-bit SAR ADC Architecture

Figure 9 shows the schematic of the 12-bit SAR ADC that consists of a binary-weighted capacitor array, a novel time-domain comparator, a digital SAR control unit, and many switches [15]. In addition, this design contains the on-chip self-calibration digital-to-analog converter (DAC) and control logic, which dominates the power consumption. In this work, in order to take advantages of 3D heterogeneous integration, we re-design the 12-bit SAR ADC by partitioning it into several stacked dies. With the proposed design methodologies described in Section 4, we expect to achieve power reduction and performance improvement as compared with the traditional 2D design case.

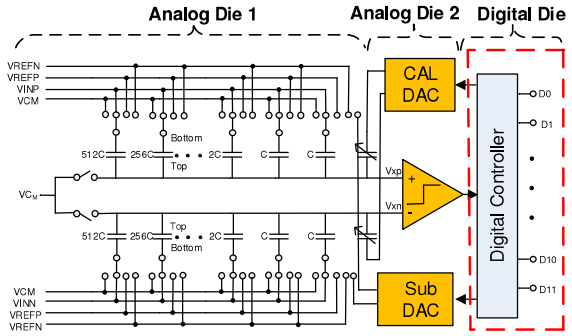

Figure 9: 12 bit SAR ADC architecture and 3D partitioning

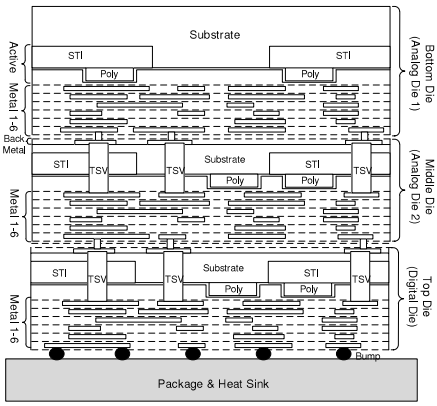

Figure 10: The three-layer F2B stacked 3D chip

5.2 3D Physical Implementation

In this work, the 3D SAR ADC is implemented with a three-layer face-to-back (F2B) stacked chip. TSVs are inserted to the top die and middle die. The top die and middle die are then thinned to tens of micrometers to expose the TSVs. In order to mitigate the coupling effects, the three-layer SAR ADC is organized such that the bottom die is for the main DAC (Analog: capacitor array), the middle die is for the sub-DAC, self-calibration DAC, and the comparator, whereas the top die is for the digital control logic and switch array. Figure 9 shows the 3D partitioning schematic and Figure 10 presents the vertical stacking schematic of our 3D chip.

The TSV technology we used in our design is from Tezzaron, with TSV size of 1.2μm × 1.2μm [4]. Dummy TSVs are inserted in order to guarantee adequate TSV density. The maximum TSV spacing is 250μm. The 3D design rule check is implemented according to HJTC 0.18μm design rules and Tezzaron 3D stacking design rules.

Figure 11 shows the layouts of the three stacked dies: two analog dies and one digital die. All of the analog and digital dies are designed with HJTC 0.18μm six-metal one polysilicon (6M1P) standard CMOS process with metal-insulator-metal (MIM) capacitors. The I/O pads are placed on the digital die.

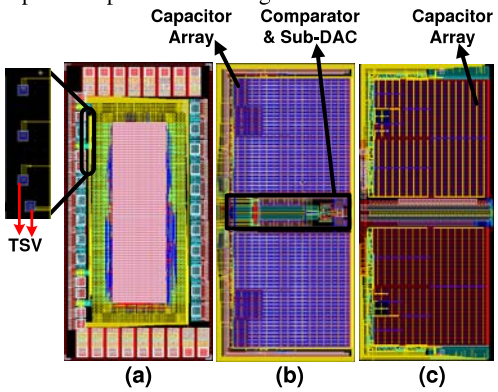

Figure 11: The layouts of the 3D 12-bit SAR ADC: (a)the top die; (b)the middle die; (c)the bottom die.

5.3 Experimental Results and Discussion

The netlist of the system is created by merging the sub-circuits of analog dies, digital die, and TSVs. With the device model libraries (HJTC 180nm digital/analog model libraries and TSV model library), the simulation is done with APS simulator which features high task parallelism to reduce the simulation time.

In order to simulate the performance of the 3D SAR ADC, the transient simulation is run for more than 1000 sampling cycles. To evaluate the efficiency of our 3D SAR ADC, we calculate the figure of merit (FOM) as below:

$$FOM = \frac{Power}{2^{ENOB} \times f_s} \tag{13}$$

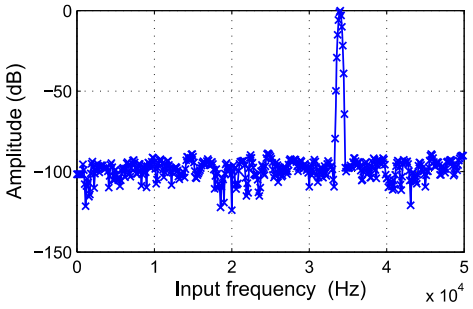

Figure 12: The dynamic performance spectrum of our designed 3D 12-bit SAR ADC

According to our proposed design guidelines for 3D mixed-signal IC design, we optimize the TSV placement to minimize the nega-

tive impacts of TSVs on the 12-bit SAR ADC. From the experimental results shown in Table 1, compared with the traditional 2D case [15], our proposed 3D 12-bit SAR ADC can achieve approximate 4.8% power reduction. Meanwhile, the SFDR is improved from 90.36 dB to 91.61 dB. Figure 12 shows the dynamic performance spectrum of our designed 3D ADC. Due to the isolation of substrate noise disturbance in our 3D design, the SNDR is improved from 68.74 dB to 74.12 dB.

In order to demonstrate the efficiency of our proposed design guidelines in system level, we implement an experiment by placing TSVs at the nearest available space, without optimizing the TSV placement according to the design guidelines. Parts of TSV locations for the TSV-optimized design and TSV-unoptimized design are shown in Figure 13. For the TSV optimized design in this figure, we place the TSVs far away from the active device areas in the available space to alleviate the TSV coupling noise disturbance. The power consumption of this unoptimized design is similar to the TSV-optimized design. However, as shown in Table 1, the unoptimized design has significant performance degradation due to the impact of the bad TSV placement. The SFDR is even worse than the traditional 2D design. Therefore, the impacts of TSVs on the mixed-signal ICs should be carefully evaluated.

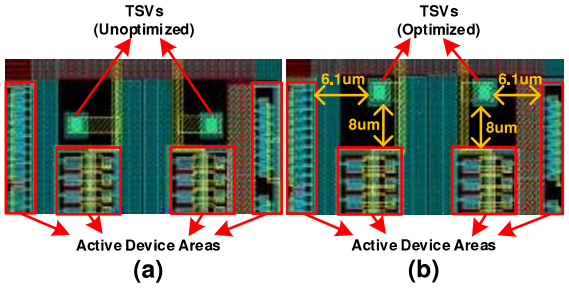

Figure 13: The TSV locations of the TSV-unoptimized design and TSV-optimized design

In addition, the power consumption of this 12-bit SAR ADC schematic is one of the most important issue [15]. To explore the reduction of power consumption for this 12-bit SAR ADC in our 3D design, we also implement an experiment by lowering the supply voltage of digital die as 1V, while the supply voltages of the other two analog dies are still 1.8V. The experimental results show that the system power consumption can be reduced to 180.53 μW. The power can be further reduced if a more advanced technology is used for the digital die.

Table 1: Comparison of the performance of several ADCs

Parameter	2D [15]	3D Optimized	3D Unoptimized
Bits	12	12	12
MS/s	0.1	0.1	0.1
Technology(um)	0.18	0.18	0.18
Supply voltage(V)	1.8	1.8	1.8
Power(uW)	579.6	552	553
SFDR(dB)	90.36	91.61	85.08
SNDR(dB)	68.74	74.12	70.15
ENOB	11.13	11.75	11.36
FOM(pJ/step)	2.59	1.60	2.10

6. CONCLUSIONS

In this work, we focus on modeling and analyzing the TSVs coupling effects in mixed-signal ICs and propose design methodologies for 3D mixed-signal ICs. A case study on a three-layer stacked 12-bit SAR ADC chip design demonstrates the advantages of 3D integration for mixed-signal IC design as compared to the counterpart implemented in traditional 2D technology.

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