TSV Power Supply Array Electromigration Lifetime Analysis in 3D ICs*

Qiaosha Zou, Tao Zhang, Cong Xu, Yuan Xie
Computer Science and Engineering
the Pennsylvania State University
University Park, PA 16802
{qszou, zhangtao, czx102, yuanxie}@cse.psu.edu

ABSTRACT

Electromigration (EM) can cause severe reliability issues in contemporary integrated circuits. For the emerging three-dimensional integrated circuits (3D ICs), the introduction of through-silicon vias (TSVs) as the vertical signal carrier complicates the electromigration analysis. In particular, an accurate EM analysis on TSV arrays that are used in the power supply network is critical since the large current going through those TSVs can accelerate their degradation. In this work, we propose a novel EM analysis framework that focuses on TSV arrays in the power supply network, under the circumstance of uneven current distribution. The impacts of various design factors on the EM lifetime are discussed in detail. Our results reveal that the predicted TSV array lifetime is largely biased without proper current distribution analysis, resulting in an unexpected early failure.

1. INTRODUCTION

Electromigration (EM), which refers to the migration of metal atoms in response to an electric field in a conductor, has been proven to be one of the major factors of interconnect failure [3]. The factors that influence EM lifetime of interconnects have been unveiled in previous studies [1, 5], emphasizing the impact of current density on conductor's EM mean-time-to-failure (MTTF).

In recent years, three-dimensional integrated circuits (3D ICs) have been proposed to overcome the increased interconnect crisis along with technology scaling. In particular, through-silicon-vias (TSVs) have been widely adopted as vertical power and signal carriers. Considering the higher current density requirement on power/ground (P/G) TSVs for the power delivery, it can induce severe EM problems on P/G TSVs [8]. Usually, multiple TSVs are applied for the power delivery due to the limited current delivering capability of a single TSV [10]. Unfortunately, prior studies on EM lifetime modeling and analysis mainly focus on individual TSVs, leaving the EM lifetime analysis on such TSV arrays unexplored. Different from previous work, we model P/G TSV arrays and perform the EM lifetime analysis.

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2. EM LIFETIME CALCULATION

In this section, the 3D power network model is introduced first. Then the framework to calculate the current density and the EM lifetime of TSV arrays is explained. In general, the EM analysis framework contains two stages. The first stage concentrates on the current distribution analysis. The calculated current densities are then used as inputs for the second stage to estimate EM lifetime of the TSV array.

2.1 Power Grid Model

The 3D power network model contains two parts: 2D planar power grids and vertical power connections. We assume two orthogonal metal layers are used for local power or ground rails, which are placed alternately. TSVs connect the global power grid between two adjacent tiers. In the design, only one TSV (*center TSV*) in the array is directly connected to one C4 bump (off-chip P/G pins) while other TSVs (*peripheral TSVs*) are connected to the center TSV with metal wires as proposed by previous study [4].

Because constant unidirectional current stress is applied, the inductance and capacitance are irrelevant to our model, leaving resistance the only parasitic parameter that should be concerned. Due to the resistance network and TSV connections, current is unevenly distributed among TSV arrays. In our framework, the value of voltage drop between two neighboring TSVs is extracted from HSPICE simulation and remains constant during the following EM analysis. TSVs and metal wires are modeled as resistors and the devices powered by the TSV array are abstracted as current sources which are predetermined or extracted from real designs.

2.2 Current Density Calculation

Due to the dependency of TSV's EM lifetime on the current density, the current analysis is performed to generate the current distribution map. In recent studies, in addition to current density, recent studies also reveal other EM driving forces including atomic concentration gradients, thermal gradients, and stress gradients [5]. The detailed EM lifetime calculation considering these factors requires significant computation overhead, which makes it infeasible to model gradual failure in a TSV array. Therefore, in this work, we focus on the impact of current distribution on the EM lifetime, and only use Black's equation [1] to estimate the MTTF.

The current density on TSV is calculated from the voltage difference between two connected nodes. Therefore, the voltage analysis is performed first when the resistance network is known. The voltage analysis contains two steps: 2D power grid voltage analysis and 3D power propagation. We modify the node-based fast algorithm [11] for 2D power grid voltage analysis and voltage propagation method [9] for 3D

TSV voltage analysis. Different from [9], we place the off-chip power supply on the bottom tier and use the distributed TSV array topology to mimic the practical design.

2.3 Array EM Lifetime Calculation

In order to explore the longest possible lifetime, we assume that **a TSV array fails if and only if when the last via in the array is worn out due to EM effect**. We apply the lognormal distribution [3, 2] for the calculation of a single TSV's EM lifetime and combine it with Monte Carlo approximation to generate the EM lifetime distribution of a TSV array.

Since the EM effect is memorizable, the stress time translation is necessary to take the stressed history into account after current redistribution. We leverage the translation rule $\left(\frac{I_{m-1}}{I_m}\right)^2 = \frac{t_m}{t_{m-1}}$ as proposed in previous work [6], where I and t denote the current density and stress time; m represents the timing sequence.

After current densities are generated for the TSV array through the voltage propagation process, one of the possible failure sequences can be determined in the following procedure. First, we select one TSV in each iteration and make it fail with weighted probabilities determined by their current densities in the program. The larger current density one TSV has, the higher probability that it will be selected. The MTTF of the selected TSV is then calculated and the EM failure time is obtained following the lognormal distribution. Then, the stressed time for the remaining TSVs are translated according to the translation rule. The current density calculation process is applied for the rest TSVs to establish the new current density map. The iteration continues until the TSV array fails due to EM degradation. To this end, one sample of array EM lifetime is successfully calculated. Monte Carlo estimation with massive samples is used to generate the MTTF and lifetime distribution for the TSV array.

3. TSV ARRAY EM LIFETIME ANALYSIS

This section shows the TSV array EM lifetime analysis results with various design parameters. For each experiment, we capture massive Monte Carlo samples to calculate the EM MTTF and generate the EM lifetime distribution. A two-tier stacking chip is used as the design target. The TSV diameter is $5\mu m$ and the height is $30\mu m$. The current load of each node in the power grid is assigned assuming an universal activity factor with fixed total current load. Experiment results are normalized to the case with one TSV under the same current load.

3.1 TSV Array EM Lifetime

In this experiment, the target P/G TSV array contains 4×4 TSVs. From the result, we can observe that the TSV array lifetime also follows the lognormal distribution. We also conduct experiments on different TSV counts with the same current load. With more TSVs, the EM lifetime is extended and the distribution variation becomes larger since the number of possible failure sequences is increased, making it harder to predict the exact EM failure time.

When an even current distribution is assumed on the TSV array, the EM lifetime would be overestimated. The results show that for four TSV array configurations (2×2, 3×3, 4×4, and 5×5), the EM MTTF in uneven current distribution is only 36.79%, 32.02%, 24.38%, and 18.89% of that in even current distribution, respectively. The percentage goes down with larger TSV array because the current distribution is more uneven.

3.2 Other Design Parameters

Filling Materials In this part, we study the impact of TSV filling materials (copper, aluminum, and tungsten [7]) on the EM lifetime. Among these three materials, copper has the smallest resistivity. The result indicates that copper TSV arrays have the longest EM lifetime, whereas aluminum and tungsten TSVs have similar EM behaviors. However, the differences of three EM lifetimes are marginal.

TSV Number and Size Normally, the overall area budget for TSVs is determined at the early design stage. With the fixed area budget, we should make the trade-off between the size and the number of TSVs to achieve the desired EM lifetime. Table 1 shows that as we increase the number of TSVs from 4 to 9, the EM lifetime is improved at first; then, it is shortened if we further increase the number of TSVs to 25.

Table 1: EM MTTF with fixed area budget

TSV count	TSV diameter (μm)	EM MTTF (a. u.)
2×2	10	221.20
3×3	6.67	374.37
4×4	5	219.93
5×5	4	146.52

4. CONCLUSION

Electromigration is an important reliability issue in nanoscale VLSI circuit designs. In this work, we propose an analysis framework for EM lifetime of P/G TSV arrays. The results show that if the current distribution is not evaluated correctly, the estimated EM lifetime is misleading. Sensitivity studies of design parameters are conducted in the paper to show their impacts on EM lifetime. For the future work, we will include the EM influence factors, such as thermal gradients and stress gradients into the EM lifetime analysis.

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