Accurate Intrinsic Gate Capacitance Model for Carbon Nanotube-Array Based FETs Considering Screening Effect

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***Abstract*—In this letter, an accurate semi-analytical model for the intrinsic gate capacitance of carbon nanotube (CN)-array based back-gated field-effect transistors (FETs) is proposed. The model accounts for electrostatic screening effect for any given number of nanotubes, their diameter, pitch, and gate-dielectric thickness. It is shown that screening effect varies significantly not only with the change in density but also with the number of nanotubes and must be considered while modeling the intrinsic gate capacitance of array-based CNFETs for both high-performance and thin-film transistor applications.**

***Index Terms*—Carbon nanotubes, CNFET, intrinsic capacitance, quantum capacitance, screening effect.**

I. Introduction

CARBON NANOTUBE (CN) arrays have been recently used in both high-performance as well as thin-film transistors to improve performance [1], [2]. Multiple nanotubes not only increase drive current of the device but also reduce the power wasted in charging unwanted parasitic capacitances, since increasing the number of nanotubes for a given device area increases the intrinsic capacitance and reduces the parasitic components. Most of these multiple CN devices, as well as the recently proposed conventional CNFET (C-CNFET) and tunneling CNFET (T-CNFET) devices, are back-gated devices [3]. Therefore, investigating electrostatic effects in back-gated nanotube-array devices is essential for optimizing the performance of these CNFETs.

Since intrinsic capacitance determines many key performance parameters such as delay and maximum operating frequency, it is important to formulate accurate models for such capacitance. The intrinsic capacitance is strongly influenced by the distribution of charges among the nanotubes that arise due to the fact that electric field lines can get screened due to the presence of other nanotubes. The screening effect in CNFETs with top, bottom, and wrapped-around gate has been studied using numerical simulations in [4]. However, such simulations provide limited physical insight into the problem.

While an analytical model has been proposed in [5], it does not account for any variation in charge density among nanotubes. The model proposed in [6] is developed for a top-gated structure, which is only valid for a limited range of the pitch. Moreover, both these models do not consider variation in screening effect with the *number* of nanotubes in the array, which is essential to fully account for any inter-tube capacitive coupling that determines charge distribution along each nanotube. Although there are accurate numerical techniques that do not assume nanotubes to be metallic conductors [7], such simulations cannot be performed efficiently when the number of CNs in the array is high. There has also been an experimental attempt to characterize and compare transport properties of dense and sparse array of nanotubes [8], but the analytical model proposed in [8] does not account for variation in screening effect. This letter introduces a new approach for accurate and fast estimation of the intrinsic gate capacitance in any array-based back-gated CNFET while considering screening effect and its variation with the number of nanotubes.

II. Nanotube-Array Gate Capacitance Calculation

The intrinsic gate capacitance (C_G) of an array based CNFET consists of electrostatic capacitance (C_E) and the quantum capacitance (C_Q) in series [9]. C_Q for an individual nanotube is given by $q^2D(E)$, where $D(E)$ is the density of states [10]. Typically, in back-gated structures, the value of C_Q for CNs is very high compared to C_E, and therefore, C_G is dominated by C_E [10]. In this section, a methodology to calculate the gate capacitance of array based device is discussed.

Consider an array of n nanotubes of radius r placed side by side with pitch $= 2s$ over a dielectric with effective thickness t and with a gate electrode beneath the dielectric [Fig. 1(a)], which is generally the case with all back-gated CNFETs. Fig. 1(b) illustrates the capacitances involved in such an array consisting of three nanotubes. Since there are multiple nanotubes, electric field lines starting from a given nanotube will not end entirely on the gate electrode as in the case of a single nanotube device due to screening by neighboring nanotubes [Fig. 1(c)]. In such cases, when a voltage is applied to the gate terminal, charges are induced over all nanotubes which are

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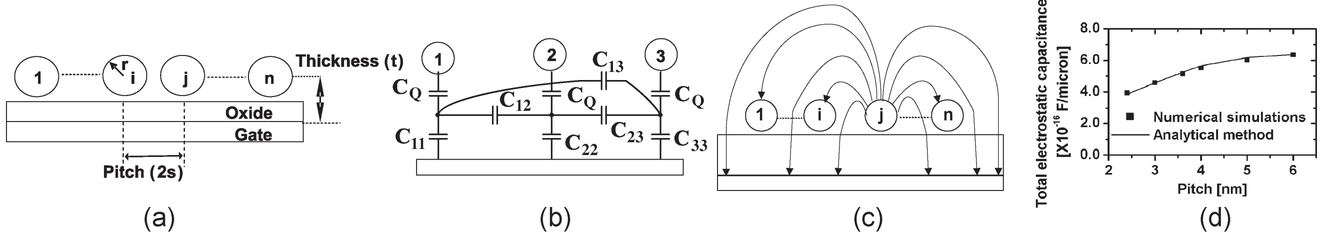

Fig. 1. (a) Cross section of a CNT-array based FET with pitch $= 2s$ $(= 2r + \text{intertube spacing})$ and effective dielectric thickness $= t$ $(= \text{physical oxide thickness} + \text{van der Waals gap} + \text{radius of nanotube})$, for the general case of n nanotubes. (b) Capacitances between the nanotubes and the gate terminal C_{ii}, quantum capacitance C_Q, and mutual capacitances C_{ij} of the nanotubes, in the case of three nanotubes. (c) Electric field lines between multiple nanotubes when j^{th} nanotube is charged with Q_j and gate is charged to $-Q_j$, illustrating screening effect. (d) Comparison of proposed method with numerical simulations for varying pitch ($r = 1$ nm, $t = 4$ nm, and $n = 12$). Both are 2-D simulations, and fringing fields at the end of the nanotubes are neglected. The deviation in proposed method is around 2%–4%. Source and drain terminals are considered to be grounded in the simulations. Note that electrostatic gate capacitance will be totally geometry dependent, independent of any terminal bias.

different for different nanotube. Hence, we need to determine the exact induced charge in the nanotubes when certain potential is applied to the gate terminal. In the proposed approach, a single nanotube is charged to Q_j, and the potential induced due to that charge on other nanotubes is examined with respect to a reference potential (in this case, the gate terminal). This process is repeated for all other nanotubes. Finally, the potentials generated on the surface of the nanotube due to charge placed on that particular nanotube as well as due to charge placed on other nanotubes are added using principle of superposition. The method is validated with 2-D numerical simulations using ANSYS and shows good agreement [Fig. 1(d)]. The method used for 2-D analysis is outlined below.

Consider the jth nanotube surrounded by $n-1$ nanotubes over the gate electrode. Such a case can be considered as a network of $n(n+1)/2$ electrostatic capacitors connected between the nanotubes (mutual capacitance) and between the nanotubes and the gate terminal. Considering CNs as solid conductors, suppose that charges Q_j and $-Q_j$ are placed on the jth conductor and the reference gate terminal, respectively, while other conductors are left floating. This arrangement will produce potential difference between each nanotube with respect to the reference gate terminal potential V_0. Let the potential developed on the ith conductor with respect to the gate terminal potential V_0 under such an arrangement be equal to $P_{\text{ij}}Q_j$, where P_{ij} is the coefficient relating the charge on the jth conductor to the potential on the ith conductor.

If this procedure is repeated for each conductor (from 1 to n), one can add all the potentials produced on the ith conductor using the superposition principle and thereby determine the total potential on the ith nanotube as $V_i = P_{i1}Q_1 + P_{i2}Q_2 + P_{i3}Q_3 + \cdots + P_{\text{in}}Q_n$ [11]. Hence, one can express the total potential for each conductor as:

$$\begin{aligned} V_1 &= P_{11}Q_1 + P_{12}Q_2 + P_{13}Q_3 \ldots P_{1n}Q_n \\ V_2 &= P_{21}Q_1 + P_{22}Q_2 + P_{23}Q_3 \ldots P_{2n}Q_n \\ V_n &= P_{n1}Q_1 + P_{n2}Q_2 + P_{n3}Q_3 \ldots P_{nn}Q_n. \end{aligned}$$

These simultaneous equations provide the value of the total potential induced on each conductor in terms of coefficients P_{ij} and charges placed on each conductor, and can be solved using the matrix method. In matrix form, one can write

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ \cdot \\ \cdot \\ \cdot \\ V_n \end{bmatrix} = \begin{bmatrix} P_{11} & P_{12} & \cdot\ \cdot\ \cdot & P_{1n} \\ P_{21} & P_{22} & \cdot\ \cdot\ \cdot & P_{2n} \\ P_{31} & P_{32} & \cdot\ \cdot\ \cdot & P_{3n} \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ P_{n1} & P_{n2} & \cdot\ \cdot\ \cdot & P_{nn} \end{bmatrix} \begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \\ \cdot \\ \cdot \\ \cdot \\ Q_n \end{bmatrix}. \quad (1)$$

The value of P_{ij} comes from the basic definition: $P_{\text{ij}} = V_i/Q_j$, when only the jth nanotube is charged and other conductors are uncharged. Using definition of potential and charge enclosed by a surface, one can express P_{ij} as

$$P_{\text{ij}} = \left.\frac{V_i}{Q_j}\right|_{Q_1=\ldots Q_{j-1}=Q_{j+1}=\ldots Q_n=0} = \frac{-\int \vec{E}_t d\vec{l}}{\varepsilon \oint\limits_s \vec{E}_t \vec{ds}} \quad (2)$$

where the denominator represents charge placed on the jth nanotube and can be determined by a closed surface integral over the surface of the jth nanotube. The numerator can be calculated by considering the potential at nanotube i in presence of the gate electrode and only the charged j^{th} nanotube, with other nanotubes being considered absent. Although this simplification introduces error in the value of mutual capacitances, the good agreement between the proposed method and numerical simulations, as shown in Fig. 1(d), indicates that this is a reasonable simplification. Using method of images, (2) can be expressed in terms of geometric parameters as [12]

$$P_{\text{ij}} = \frac{\frac{Q_j}{2\pi\varepsilon} \ln\sqrt{1+\left(\frac{t}{s_{\text{ij}}}\right)^2}}{Q_j} = \frac{\ln\sqrt{1+\left(\frac{t}{s_{\text{ij}}}\right)^2}}{2\pi\varepsilon} \quad (3)$$

where s_{ij} is half of the center-to-center distance between i^{th} and j^{th} nanotubes and t is the effective dielectric thickness. The case $i = j$ represents the diagonal elements of the matrix,

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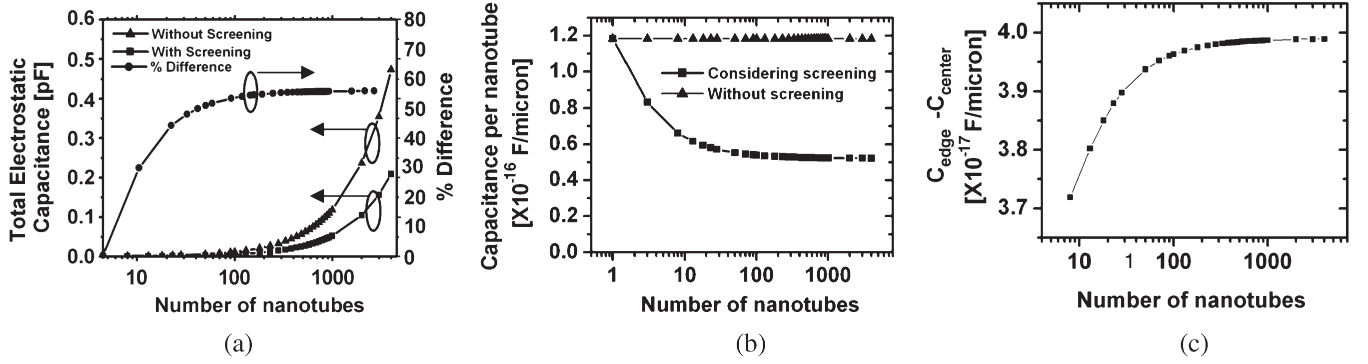

Fig. 2. (a) Total electrostatic gate capacitance in picofarads with the number of nanotubes for $r = 1$ nm, $t = 4$ nm, pitch $= 6$ nm, length $= 1$ μm, and aluminum oxide dielectric (K $\sim$ 5) [13]. Since there is a van der Waals gap between the dielectric and nanotube, analysis of effective dielectric permittivity was done as illustrated in [12]. (b) Change in electrostatic gate capacitance per nanotube. Each nanotube in the array will have different capacitance with respect to the gate terminal, but for depicting overall effect on electrostatic capacitance, average capacitance per nanotube is plotted. (c) Change in electrostatic capacitance between central and edge nanotubes with the number of nanotubes in an array.

which correspond to the potential of a nanotube with respect to the gate terminal due to its own charge. Thus,

$$P_{\rm ii} = \frac{\ln\left(\frac{t}{r_i} + \sqrt{\left(\frac{t}{r_i}\right)^2 - 1}\right)}{2\pi\varepsilon} = \frac{\cosh^{-1}\left(\frac{t}{r_i}\right)}{2\pi\varepsilon} \tag{4}$$

where r_i is the radius of $i^{\rm th}$ nanotube. Once the [P] matrix in (1) has been determined using (3) and (4), the coupling capacitance matrix can be obtained by inverting [P], which can be represented as:

$$\begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ Q_n \end{bmatrix} = \begin{bmatrix} \sum_{j=1}^{n} C_{1j} & -C_{12} & \cdot\cdot\cdot & -C_{1n} \\ -C_{21} & \sum_{j=1}^{n} C_{2j} & \cdot\cdot\cdot & -C_{2n} \\ -C_{31} & -C_{32} & \cdot\cdot\cdot & -C_{3n} \\ \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot \\ -C_{n1} & -C_{n2} & \cdot\cdot\cdot & \sum_{j=1}^{n} C_{\rm nj} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ V_n \end{bmatrix} \tag{5}$$

where $C_{\rm ii}$ and $C_{\rm ij}$ represent the capacitance components as shown in Fig. 1(b). In the matrix form, it can be represented as $[Q] = [C][V]$. From this capacitance matrix, one can accurately estimate the effective electrostatic capacitance between each nanotube and the gate terminal by adding all row elements for $V_1 = V_2 = \cdots = V_n$. As discussed earlier, neglecting the presence of surrounding nanotubes while calculating each $P_{\rm ij}$ element introduces some error in the off diagonal terms $[C]_{\rm ij}$. However, the error in overall capacitance is still small, as shown in Fig. 1(d). This is because the error in $[C]_{\rm ij}$ is significant only when $|i - j| > 2$. However, in these cases, $[C]_{\rm ij}$ is at least two orders of magnitude smaller than the diagonal terms of the capacitance matrix.

To calculate the intrinsic gate capacitance of an array based CNFET, one must also consider the quantum (C_Q) capacitance. Note that C_Q depends on the biasing condition of the transistor [7]. Hence, for a given bias, C_Q can be evaluated and included in the value of the intrinsic gate capacitance. Since the total potential on each CN is the sum of the potential drop across electrostatic and quantum capacitances, which have the same charge, the overall intrinsic capacitance matrix $[C_{G,\rm array}]$ is given by

$$\frac{1}{[C_{G,\rm array}]} = \frac{1}{[C_Q]} + \frac{1}{[C_E]}. \tag{6}$$

III. Results and Discussion

In this section, the dependence of electrostatic capacitance on factors such as the number of nanotubes in the array, spacing between nanotubes (or pitch), and diameter of nanotube is examined using the proposed model. Fig. 2(a) shows the total electrostatic gate capacitance considering and without considering the screening effect. It can be observed that there is a substantial difference in the total capacitance value and the difference increases with the number of nanotubes. Fig. 2(b) shows the variation of electrostatic gate capacitance per nanotube with change in the number of CNs in the array. Significant amount of reduction in capacitance per nanotube (up to 50%) can be observed with increase in the number of nanotubes in the array, even with constant pitch (or density), due to the increase in screening with the number of nanotubes. Fig. 2(c) shows that the difference between the edge and the center nanotube remains small compared to the reduction in overall electrostatic capacitance per nanotube [Fig. 2(b)], indicating that the effect of reduction in capacitance due to screening is approximately equally shared by all nanotubes. It also highlights the utility of the proposed method in providing physical insight into the capacitance in the array, which the other analytical methods fail to provide.

Fig. 3 shows the impact of variation of both pitch and the number of nanotubes. It can be observed that for a given density, capacitance per nanotube varies with the number of nanotubes in the array. Furthermore, it can be observed that as the pitch decreases (higher density), the screening increases, resulting in stronger dependence of capacitance on the number of nanotubes, which will be the case in dense array-based deeply scaled CNFETs. Inset of Fig. 3 shows that the model can further be employed to study the variation in capacitance with diameter of nanotubes in the array.

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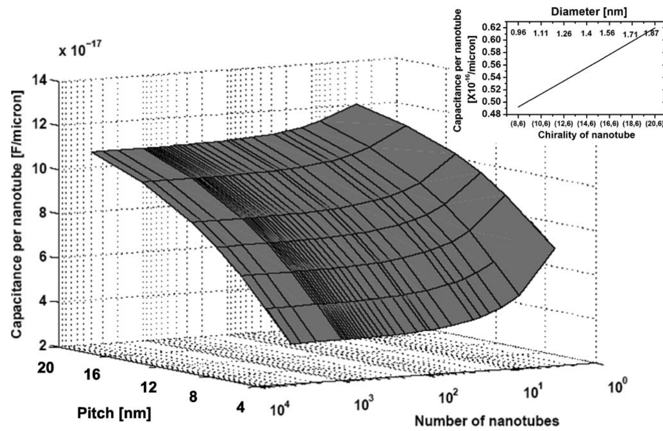

Fig. 3. Variation of average electrostatic gate capacitance per nanotube with pitch and the number of nanotubes ($r = 1$ nm and $t = 4$ nm). Inset shows variation of capacitance with change in diameter (chiral vector) of the nanotube (for $n = 10$, $s = 3$ nm, and $t = 4$ nm).

IV. Conclusion

An accurate semi-analytical model for intrinsic gate capacitance of array based back-gated CNFETs has been presented. The model accounts for screening effect as well as dependence on the nanotube diameter, pitch, and underlying dielectric thickness. In contrast with all previous modeling efforts, it is shown that screening effect, which can lower average nanotube capacitance by up to 50%, varies significantly with the number of nanotubes. Moreover, the variation becomes stronger at higher nanotube densities, emphasizing the need to accurately account for screening effect in the modeling of intrinsic gate capacitance of deeply scaled array-based CNFETs.

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