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Design tools eye nanoscale realm

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San Jose, Calif. — As the CAD community grapples with emerging technologies like silicon nanowires, biofluidic microchips and DNA self-assembly, one major question emerges: How are we going to design this stuff? That challenge was brought before researchers last week at the International Conference on Computer-Aided Design (ICCAD) here.

When noted researchers in nanotechnology and bioelectronics described design challenges and requirements for design tools, the CAD community listened. "There is a certain maturity in traditional CAD, and we're looking for a way to extend our focus," said Soha Hassoun, ICCAD program chair and associate professor of electrical engineering and computer science at Tufts University. "There are a lot of exciting challenges in nanotechnology that we need to look at."

Andr?DeHon, associate professor of computer science at the California Institute of Technology, said, "If I'm looking at what I'll be designing 10 years from now, there will be changes in methodologies and in what I need from CAD."

One big issue for DeHon and other researchers is defect tolerance: As devices become very small, they are going to have relatively high defect rates.

Another message from ICCAD is that CMOS scaling is heading toward the end of the road. "The lithography approach will fail very soon," said Konstantin Likharev, professor of electrical engineering at Stony Brook University. Because the usual lithographic patterning is just too expensive below 20 nanometers, he said, it's time to look at "bottom-up" approaches using objects at the molecular level.

An example is the molecular single-electron transistor, which traps a molecule between the source and the drain. A change in the number of electrons in the molecule causes switching to occur. While such devices are promising, yields are presently very low, Likharev said.

The real opportunity, he said, is for "hybrid CMOS/nanocircuits." These could combine the functionality, reliability, and fab and EDA infrastructure of CMOS with the very high density achievable with nanotechnology. To this end, several research groups have developed nanowire crossbar architectures with two-terminal programmable diodes at every crossbar point.

Stony Brook's so-called CMOL architecture uses two-terminal, single-electron latching switches at each point of a metallic crossbar. To allow access to individual nanodevices, it's tilted relative to the CMOS circuitry. CMOL has been applied to memories and FPGA fabrics. Using "rudimentary CAD tools," Likharev said, researchers managed to create an FPGA fabric with a hundredfold area advantage.

Design challenges for this type of architecture include individual addressing of nanodevices, defect analysis and defect tolerance. "We need better CAD tools," Likharev said. "There is a good opportunity for this [design automation] community to do some important work while the technology is still in its infancy."

DeHon, who co-authored a paper with Likharev, described research with silicon nanowires that can be 3 nm in diameter and several microns long. The electrical properties can be controlled through selective doping. The nanowires are "grown" and aligned on liquid film, and are then transferred to a substrate.

When nanowires are assembled with unique codes, they can form an address decoder. If individual nanowires are kept relatively short, this technology can be used to construct memories or logic. DeHon showed an example of a nanowire-based

PLA that offered density improvements ranging from 32 to 1,000 times in benchmark circuits.

A key EDA requirement for this type of architecture, DeHon said, is statistical analysis, prediction and optimization. Other necessary capabilities are defect calculation, location and mapping, allowing designs to be customized around defects. Finally, "lightweight" online error detection will be required to catch defects and transient errors that occur during operation. "I see an increasing role for CAD, especially dealing with post-fab issues," DeHon said.

Navin Srivastava, PhD candidate at the University of California at Santa Barbara, presented research on "realistic" RLC (resistance, inductance, capacitance) modeling of carbon nanotubes. Realizing these models is a first step toward building CAD tools for such devices, he said.

Previous modeling efforts, Srivastava said, did not provide realistic RLC calculations for bundled carbon-nanotube interconnects, did not allow for imperfect contacts, and used unrealistic drivers and loads. A "fair comparison" to copper, he said, shows that carbon-nanotube bundled interconnects don't provide much performance improvement at the local level, but do show a significant improvement for long, global interconnects.

Since nanofabrication is a very tough challenge, self-assembly — the spontaneous organization of matter under controlled conditions — is an attractive alternative. Paul Rothemund, a senior research fellow at the California Institute of Technology, showed how DNA self-assembly can generate arbitrary patterns and shapes at resolutions down to 6 nm.

Rothemund's "scaffolded origami" involves folding long, single strands of DNA into arbitrary two-dimensional shapes using a raster fill technique. DNA "helper" strands fold the scaffold into the proper formation. Design and synthesis are so simple that even a high school student could do it, he said, but that doesn't mean some automated CAD tools aren't needed.

"In making these shapes, I did a lot of things manually," Rothemund said. "I used the computer as glorified graph paper and determined the architecture of the design by hand." There's a lot of room for optimization in the design of DNA sequences, he noted.

The potential benefits of DNA self-assembly were further demonstrated in a paper presented by Chris Dwyer, assistant professor of electrical and computer engineering at Duke University. His work involves shaping DNA strands into self-assembled grids that could potentially produce patterns relevant to logic circuitry.

Dwyer's price is hard to beat. His paper said he was able to generate 10^{12} to 10^{14} structures for a materials cost of \$40, with approximately 60 percent yield. This can be done in a 60-microliter reaction volume. "The technology is here, and it's time to start thinking about architectures and systems," Dwyer said.

His research group currently has tools for cluster-based sequence optimization, layout and assembly. Dwyer's "wish list" includes yield-aware design optimization, refined device models and better, automated full-custom layout.

CAD for lab-on-a-chip

One of the most futuristic nanodevices is the biofluidic microchip, which includes lab-on-a-chip devices that can take a fluid sample and run a biochemical analysis. Portable analysis is the driving need, said Tamal Mukherjee, professor of electrical and computer engineering at Carnegie Mellon University.

"We eventually want to get to something like Mr. Spock and his tricorder," he said. With a lab-on-chip, Mukherjee noted, a user might be able to identify the virus that's making a child sick, transmit the DNA sequence to a pharmacy and get the correct treatment right away.

Some lab-on-chip devices transfer droplets using electrical fields. Others use pressure or voltage to move fluids through channels. Subsystems handle functions such as injection, mixing, separation and reaction. But it's a lot like system-on-chip design, Mukherjee said, in that it involves a limited set of library elements that are replicated many times.

Lab-on-chip designers must size microfluidic channels and determine electrokinetic drive voltages. The designers perform simulation, optimization, placement and routing. Mukherjee described a hierarchical decomposition approach that uses "Spice-like" code to assemble the design. It uses a library of parameterized models for wells, mixers, reactors, injectors, separators and splitters.

In addition to simulation and optimization, these models can be used to perform physical synthesis. Properties and constraints are used to floor-plan subsystems, determine placement of components such as wells and route subsystems to wells.

"We're focused at the circuit level," Mukherjee said. "We still haven't addressed architecture or protocol optimization."

Small world after all

From a CAD perspective, said Seth Goldstein, associate professor of electrical and computer engineering at Carnegie Mellon University, it's not so much the technology that's important — it's the revolution in system design made possible by the availability of massive numbers of nanoscale devices.

Because we'll have so many devices, Goldstein said, it's inevitable that reconfigurable computing will be needed to speed time-to-market and reduce manufacturing costs. Asynchronous architectures will reduce power, solve timing problems and aid defect tolerance. Spatial computing, which optimizes for wires at the expense of using more computational nodes, will reduce power and wire delay.

This scenario calls for significant new EDA developments, including very high-level synthesis and tools that can handle asynchronous design. "There's no reason at all that humans should be involved in the verification process from models on down," Goldstein said.

Such statements make it clear that the real design challenge for nanotechnology is not RLC modeling for carbon nanotubes, but figuring out how to take billions of devices and build something useful quickly.

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