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For Immediate Release

Tipsheet For
2005 IEEE International Electron Devices Meeting (IEDM)

The annual IEDM presents the best applied research in electronics from labs around the world. This Tipsheet is a sneak peek at some of the most interesting papers to be given at the 51st annual meeting, December 5 - 7 at the Washington, D.C. Hilton. The meeting will be preceded by a day of Short Courses on Sunday, Dec. 4. Please contact us to schedule interviews with IEDM spokespeople or with researchers, and for more information or graphics. Note that additional photos and other material may be put on the web site on an ongoing basis.[1]

Here are the topics in this Tipsheet:

1. Progress And Problems With Chips
2. Almost Here: 65-nm Technology
3. A Step Beyond: 45-nm Technology
4. Advanced Structures & Devices
5. Building New Memories
6. Big Developments At The Nano Level
7. Plastic, Flexible and Stretchable Electronics
8. A Technological Potpourri

1. Progress And Problems With Chips

Modern electronics is based on the transistor, a tiny electrical switch with no moving parts made from silicon or other semiconductors that allow electricity to pass through or not as desired. Transistors can be ganged together by the millions and programmed to sense inputs, to process information and to deliver outputs. They make electronics as we know it possible.

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[1] *While we may make available to journalists abstracts of many of the IEDM papers prior to the conference, they are given out on the understanding you will draw excerpts from them to flesh out conference-preview news or feature articles. We cannot make abstracts available to anyone who would print substantially all of the information contained in an abstract prior to the conference, or who would show it directly or indirectly to a competitor of the presenting company, or to a consultant/analyst.*

But "electronics as we know it" is changing, a victim of its own success. Integrated circuits, or chips, are fingernail-sized slabs of semiconducting material on which devices like transistors and their interconnections have been built. Progress comes from more integration -- putting more elements on chips to add more functions at less cost. To do this, everything must be shrunk, or in industry terminology "scaled."

But as these elements scale from microns to nanometers, formerly small problems loom large. Current leakage and other undesirable phenomena are becoming major stumbling blocks. It isn’t clear how all of these problems will be solved, but we know simply continuing to make devices smaller won’t always work -- in fact it will add new problems. But technologists continue to produce useful insights and each year the IEDM helps bring them forward.

Each new technology generation, or node, is designated by half the size i.e. -- half the pitch -- of the distance between adjacent printed lines. The pitch is measured in nanometers (nm, billionths of a meter). Most major semiconductor companies have introduced 90-nm chips. Many leading companies will have 65-nm chips in volume production beginning in 2006. The generation to follow -- 45 nm technology -- is expected to be in pre-production in 2008.

Most transistors are made from silicon using a manufacturing process called CMOS (complementary metal oxide semiconductor). These field-effect transistors are generically called MOSFETs, and a great many papers will address the challenges of making them and their interconnects smaller, faster, more reliable and less power-hungry.

Much work deals with the transistor gate, which controls the device. The gate's insulator, or dielectric, is important because if current leaks through the device won't work properly. Gates typically are polysilicon, with a silicon dioxide dielectric. Silicon oxide mates with polysilicon perfectly but in future chips -- maybe even the 45-nm node -- it will need to be a few atoms thick and it won't have the necessary insulating qualities at those dimensions. Other good dielectric materials exist but they aren't compatible with polysilicon gates. They would complement metal gates, but those pose challenges of their own. (In industry terminology the need is to find a good high-k dielectric. The higher the numerical value of "k", the better the insulator.)

Another key issue is the wiring or interconnect which connects devices on a chip. The tiny widths and close proximity of adjacent copper lines introduce resistance and capacitance delays that impose a virtual "speed limit" on the speed at which an advanced chip can operate. Here a low-k dielectric is needed, but these tend to be fragile if not porous materials which pose many processing and reliability challenges.

On other fronts, standard “bulk” silicon isn’t the only useful semiconductor. Faster transistors compatible with standard CMOS fabrication processes can be made from strained silicon. Also, speedy chips made with alloys of silicon and germanium (SiGe) are the focus of much research, as is the use of germanium combined with new dielectric materials. Completely different semiconductors also may yield ultra-fast transistors for high-performance systems.

Finally, the IEDM will address issues at the frontiers of electronics, among them such thought-provoking topics as flexible and stretchable electronic circuits, nanoelectromechanical switches for ultra-dense memory chips, self-assembled 3-D chips and many others.

2. Almost Here: 65-nm Technology

- **65-nm SOI Strained Four Ways:** Researchers from the IBM/Sony/Toshiba/AMD alliance will discuss an integrated 65-nm SOI technology that delivers exceptional performance, adds few additional process steps and offers yields and reliability comparable to baseline 65-nm technology. All known methods of straining silicon are used: 1) a dual stress liner using compressive stressed nitride on NMOS transistors and tensile stressed nitride on PMOS devices to give each the optimum strain; 2) embedded SiGe puts compressive strain in the source/drain regions of PMOS devices; and 3) a novel stress-memorization technique strains NMOS devices. With the latter, a nitride layer is placed on the gate before annealing the source/drain regions. These regions recrystallize during the anneal, introducing strain. When the nitride layer is removed following anneal, the strain remains. Impressive on-off performance was achieved: drive currents of 735µA/µm and 1259µA/µm for p-FETS and n-FETs, respectively, and off current of 200 nA/µm.

  The technology also uses an advanced low-k SiCOH-based interconnect dielectric (k=2.75) in some of 10 wiring levels, leading to a 6% reduction in interconnect delay. The researchers built a 0.65µm^2 SRAM cell to test for reliability and yield. **(Paper #3.3, *"High Performance 65 nm Technology with Enhanced Transistor Strain and Advanced Low-k BEOL,"* W-H. Lee et al)**

- **New Facet of p-FET Performance:** Silicon, like diamond, is crystalline with different “faces” or surface orientations. Complementary CMOS circuits feature two different transistor architectures that must work in tandem, p-FETs and n-FETs. N-FET devices are faster and prefer a (100) surface. If p-FET performance could be ratcheted up without degrading the n-FETs, overall faster circuits would result. P-FETs prefer a (110) surface.

  IBM researchers will describe how they built mixed-orientation silicon substrates in 65-nm technology using a novel direct-silicon bonding process and with solid-phase epitaxy. Mixed-orientation substrates have been demonstrated previously in silicon-on-insulator technology, but never in standard bulk silicon. The result was an increase in p-FET performance of 35% with no degradation of the n-FETs. When a simple benchmarking circuit called a ring oscillator was built with this technology, gate delays were reduced by 20%. **(Paper #10.3, *"High Performance CMOS Bulk Technology using Direct Silicon Bond (DSB) Mixed Crystal Orientation Substrates,"* C.Y. Sung et al, IBM)**

3. A Step Beyond: 45-nm Technology

- **Record Drive Currents, On/Off:** Intel researchers will report state-of-the-art 35-nm transistors with record drive currents (1.75mA/µm for NMOS devices, 1.06mA/µm for PMOS) and on-off characteristics (low standby current of 100nA/µm in each case). These are the first to combine highly strained silicon channels with fully silicided metal gates, and with an ultra-thin 1.2-nm SiON gate oxide.

  Strained silicon allows a transistor to operate more quickly than standard bulk silicon, or to operate at the same speed but more efficiently. Here, Intel built a highly strained transistor channel and combined it for the first time with fully silicided metal gates. These gates began as polysilicon but the FUSI process converted them into metal by diffusing nickel through them. Building a metal gate this way can be done at low processing temperatures and avoids gate-depletion effects. The process also prevents metal from compromising the gate dielectric. **(Paper #10.1, *"High Performance 35nm L_{gate} CMOS Transistors Featuring NiSi Metal Gate (FUSI), Uniaxial Strained Silicon Channels and 1.2nm Gate Oxide,"* P. Ranade et al, Intel)**

- **Half the Power:** There are many reasons why simply scaling things down in size may not bring about the speed, power and cost advantages the industry always has enjoyed. Two are that in ultra-small devices, junction-leakage currents are too high and drive currents are not high enough. Fujitsu will describe an integrated approach to overcome these issues and scale to the 45-nm node.

  First, they used an improved shallow trench isolation to build devices with reduced leakage currents. These also featured strained silicon in the channel and SiON gate dielectrics. They were used to build a conventional 6T SRAM memory cell, which was half the size (0.246 μm^2) of a similar cell built with 65-nm process technology. Then, to reduce capacitance among the wires which interconnect these tiny devices, they used a nano-clustering silica low-k dielectric (k=2.25). The net effect of all these improvements was a 50% reduction in required power, compared to 65-nm technology. **(Paper #3.2, *"45-nm Node CMOS Integration with a Novel STI Structure and Full-NCS Interlayers for Low-Operation-Power (LOP) Applications,"* M. Okuno et al, Fujitsu)**

- **Strained Silicon at 45 nm:** Toshiba will argue strained silicon can be fully integrated into a 45-nm process, and maybe beyond. Researchers will assert that strain generated by stress liners and by an embedded SiGe layer in the substrate, combined with a SiOn gate dielectric and the tuning of other elements for optimum performance, is both manufacturable and scalable. **(Paper #10.4, *"High Performance CMOSFET Technology for 45nm Generation and Scalability of Stress-Induced Mobility Enhancement Technique,"* A. Oishi et al, Toshiba)**

- **High Humidity**: With regard to interconnect, there are many challenges to the adoption of ultra-low-k dielectrics and their integration with 45-nm technology. One key issue is unwanted moisture uptake by these porous, sponge-like materials. A Toshiba paper will discuss moisture-induced failure in 75-nm-wide vias, in chips with porous low-k films where k=2.3. (Vias are holes filled with copper. They physically and electrically connect copper wires among a chip's different levels.) The researchers found failure of the vias has to do with specific interconnect layouts that provide poor "ventilation" of the moisture in the low-k material. They assert such moisture-induced via failure can be suppressed completely in 45-nm technology with proper layout design. **(Paper #8.2, *"Mechanism of Moisture Uptake Induced Via Failure and Its Impact on 45nm Node Interconnect Design,"* T. Fujimaki et al, Toshiba)**

4. Advanced Structures & Devices

- **Selectively Relaxed Strain:** As transistors grow smaller they become harder to turn off reliably. To overcome this, researchers are looking into devices having multiple gates, such as the FinFET (so-called because its channel resembles the dorsal fin of a shark) and other multiple-gate geometries. However, while it is routine to apply uniaxially strained silicon in the channel regions of flat, or planar, devices for better performance, it has never been done for transistors with complex channel geometries that aren't flat. Until now, anyway.

  A MIRAI-ASET team from Japan will describe how they did it for the first time and achieved superb device performance as a result. They established a global bi-axial strain throughout the entire channel region of SGOI (silicon-germanium-on-insulator) FinFETs, and then relaxed it selectively. These FinFETs were 55-nm wide and 90-nm tall. The resulting uniaxial strain in targeted channel regions, combined with other improvements, led to superb on-off performance ($>10^8$). **(Paper #30.1, *"High Performance Multi-Gate pMOSFETs using Uniaxially Strained SGOI Channels,"* T. Irisawa et al, MIRAI-ASET)**

- **Ultra-Thin Insulator:** For the 32-nm and 16-nm technology nodes, researchers are puzzling over how to build a gate dielectric just a few atoms thick that will prevent sky-high gate leakage current. Toshiba will describe a novel ultra-thin lanthanum aluminate dielectric with excellent electrical characteristics. They achieved only 0.1A/cm^2 gate leakage even though the dielectric is equivalent to only three angstroms of SiO_2. It was built on a silicon substrate using a novel high-temperature deposition process. **(Paper #17.6, *"Ultra Thin (EOT=3Å) and Low Leakage Dielectrics of La-Aluminate Directly on Si Substrate Fabricated by High Temperature Deposition,"* M. Suzuki et al, Toshiba)**

- **Record GaN Power Output:** Many advanced military and commercial electronic systems require components offering high bandwidth at RF or microwave frequencies, or ultra-fast switching speeds. While silicon yields slower devices than some other semiconductors, it can be alloyed with certain of them to build blazingly fast devices. A team from Nitronex Corp. will describe a gallium nitride-on-silicon technology that resulted in a FET with the highest output power ever achieved for gallium nitride: a pulsed power output of 368 W at 2.14 GHz, with 70% drain efficiency and 17.5 dB of small-signal gain. **(Paper #23.1, *"A 36mm GaN-on-Si HFET Producing 368W with 70% Drain Efficiency,"* R. Therrien et al, Nitronex Corp.)**

- **InSb -- The Fastest Semiconductor:** As the end of scaling looms and the need to identify new device technology becomes pressing, attention will turn to III-V compound semiconductors, so called because of the columns in the periodic table of elements in which they appear. III-V semiconductors, though expensive and difficult to work with, are suitable for very high speed and low power logic applications. In particular, indium antimonide (InSb) offers the highest electron mobilities and saturation velocity of any known semiconductor, and is a promising channel material. Researchers from Intel and QinetiQ Corp. will describe 85-nm InSb HFETs that offer a 50% higher intrinsic switching frequency and a six-to-10% reduction in DC power dissipation, compared to advanced silicon MOSFETs. **(Paper #32.1, *"85nm Gate Length Enhancement and Depletion Mode InSb Quantum Well Transistors for Ultra High Speed and Very Low Power Digital Logic Applications,"* S. Datta et al, Intel/QinetiQ)**

5. Building New Memories

Research into memory devices is a major part of the IEDM. Papers will be presented on all of the main memory types -- DRAM, SRAM and flash -- as well as on new types currently under development, and on totally new future concepts. Regardless of the type, all memory devices have in common the ability to store and recognize something representing the values “0” and “1.” Manipulation of these values is the basis of computing. Here are some noteworthy memory papers (see the "Nanostructures" section for an additional one, #11.4):

- **Spin-RAM, A Universal Memory?** Designers want to use more and denser solid-state memory in electronic devices to eliminate hard drives and to increase storage, making new products and form-factors possible. Today's workhorse memory is the DRAM. It can be accessed at high speed but loses its data when the power is turned off. Other memory types are non-volatile but are either slower, less dense (e.g. they don't hold as much data) and/or power-hungry. The Holy Grail of memory developers is one universal type that blends the best of all these traits, and which can be scaled to smaller sizes as CMOS technology advances. Existing non-volatile magnetic memories (MRAMs) are the focus of much research, but they may be unable to scale small enough, and they consume too much power.

  However, Sony researchers built an MRAM based on different physical principles. Dubbed the Spin-RAM because it operates according to the spin-torque of electrons, it has fast 2-ns switching speeds, the ability to switch at 300 µA (1/20th the power needed for a conventional MRAM), and outstanding scalability and long-term reliability. The memory cell consists of a magnetic tunnel junction (two ferromagnetic layers separated by a spacer) and a transistor. The spin-torque of electrons flowing through the junction can be controlled and can increase or decrease the resistance of one of the ferromagnetic layers. This has important implications: Since spin-torque is used to "program" the cell, no external magnetic field is required and lower currents may be used. This makes this memory technology more scalable than conventional MRAM. The use of spin-torque to program the cell causes a change in the cell resistance. This resistance can be read as "0" or a "1." The team built a 100x150-nm 4kbit memory cell with a standard 180-nm CMOS process. They say cell size can be reduced to a $6F^2$ minimum. **(Paper #19.1, *"A Novel Nonvolatile Memory with Spin Torque Transfer Magnetization Switching: Spin-RAM,"* M. Hosomi et al, Sony)**

- **Long-Term Nanocrystal Memory:** Some non-volatile memory cells make use of a floating gate: an area where charge is stored to represent a "1", separated by an oxide layer from the rest of the cell. The oxide barrier prevents charge from leaking out but it usually contains weak spots that allow the charge to leak out over time.

  Toshiba researchers will describe a planar 35-nm gate-length MOSFET SiN trap memory that uses a layer of 1.5-nm silicon nanocrystals as the barrier, separating double tunnel junctions. It can retain a four-decade-wide memory window for 10 years, with outstanding read/write reliability and low operating voltages. Inherent dangling bond traps in the nanocrystal layer are what suppress charge leakage. The research suggests both charge-retention and scaling can be improved by reducing the size of the nanocrystals. **(Paper # 35.2, *"35 nm Floating Gate Planar MOSFET Memory using Double Junction Tunneling,"* R. Ohba et al, Toshiba)**

- **Protein Templates For Nanocrystal Memory Arrays:** The difficulty with nanocrystals is that layers of them are not uniform. University of Texas-Austin researchers will describe a self-assembling, ultra-small protein lattice that can be used as a template to assemble uniform nanocrystal arrays for flash memories. The idea is that an ordered array of tiny proteins known as chaperonins is formed on a 3.5-nm tunnel oxide layer on a Si wafer. This is done by bathing the layer in a chaperonin protein solution. Each protein has a chemical environment that can trap a nanocrystal within it. When the proteins are removed by 200°C annealing in oxygen, a very dense and uniform nanocrystal distribution results.

  The team used lead selenide crystals and achieved densities of $9.5\times10^{11}/cm^2$, though they say their method also would work with any other existing type of nanocrystal. Endurance of the array was greater than 10^5 cycles, retention time was greater than 10^4 seconds, and there was a voltage shift of just 0.5V under 8V operation. **(Paper #7.6, *"Nanocrystal Flash Memory Fabricated with Protein-Mediated Assembly,"* S. Tang et al, University of Texas-Austin.)**

- **Non-Volatile Electrolytic Memory:** Electrolytes normally are thought of as molten or liquid substances that conduct electricity. Solid electrolytes exist, however, and they have a key property: their conducting and non-conducting states are non-volatile. Thus, one could build a non-volatile memory if one had the ability to create or dissolve conduction paths in a solid electrolyte that bridged a memory cell's source and drain electrodes. The problem is, if the controlling gate lies in the conduction path, high operating voltages and currents are needed.

  NEC researchers got around this by creating a novel three-terminal device at nanometer dimensions. The solid electrolyte is a 40-nm spin-coated layer of Cu_2S; the source and gate electrodes are copper; and the drain electrode is made from platinum. When a positive voltage is applied to the gate, both the gate and the source electrode inject positive copper ions into the electrolyte. When that happens, a copper bridge grows within the electrolyte and electrically connects the source and drain. The bridge disappears when a negative voltage is applied. More work needs to be done to improve cycling endurance and to reduce switching speeds at lower voltages, but the work is a promising first step. **(Paper #19.5, *"Three Terminal Solid-Electrolyte Nanometer Switch,"* T. Sakamoto et al, NEC)**

6. Big Developments At The Nano Level

Some of the most interesting work in the physical and life sciences is being done on the scale of nanometers, the Lilliputian world where microscopic mechanical structures, molecules, living cells, and atoms and atomic particles like electrons intersect. The IEDM has always been at the forefront of nanotechnology as applied to electronics.

- **Nanoelectromechanical Switches for DRAM:** Can one make an ultra-small DRAM memory cell from tiny carbon nanotubes, nanoscale cylindrical structures that conduct electricity? Cambridge University researchers will describe a nanoelectromechanical DRAM memory cell built from two adjacent nanotubes grown upward from a substrate. The nanotubes are connected to a capacitor and either attract or repulse each other depending on whether the capacitor injects a charge into them with opposite or the same polarity. The switching action breaks or makes a circuit and corresponds to a memory value of either "0" or "1," which is read by sensing the charge on the capacitor. The researchers built arrays of these nanotubes. Their small size, plus the cell's vertical structure, give it very compact dimensions, meaning that if this idea could be made practical, it would be a way to dramatically increase the density of DRAM and other memory types. **(Paper #11.4, *"Nanoelectromechanical DRAM for ultra-large-scale integration (ULSI),"* J.E. Jang et al, University of Cambridge)**

- **Twin Nanowires :** Various new transistor concepts have been reported as potential solutions to the scaling problem. Samsung researchers will report on MOSFETs consisting of two 10-nm-diameter silicon nanowires with a wrap-around gate. They exhibited outstanding off-state performance and were made on a bulk silicon wafer with existing lithography equipment, using a self-aligned dual-damascene approach. Drive currents were 2.64 mA/µm (n-channel) and 1.11 mA/µm (p-channel), and the on/off ratio was as high as 10^8. **(Paper #30.3, *"High Performance 5nm Radius Twin Silicon Nanowire MOSFET [TSNWFET]:Fabrication on Bulk Si Wafer, Characteristics and Reliability,"* S. Dae Suk et al, Samsung)**

- **A Forest of Nanowires as the Channel:** Researchers from Sweden's Lund University built a MOSFET using an air-bridge design with a 10x10 vertical array of InAs nanowires as the channel. Electrons flow through InAs extremely fast, and so this structure promises excellent performance. Electron mobilities through the array may be as high as 10000 cm^2/Vs, and drive current of 100µA and transconductance of 2 mS were measured at zero gate voltage.

  The nanowires were 1 µm apart, grown by chemical beam epitaxy on lithographically defined gold disks on a substrate, which acted as catalysts for their growth. The disks were patterned using electron-beam lithography. All other patterning was accomplished with conventional optical lithography and standard III-V processing techniques. A wrap-gate dielectric and the gold disks were formed from low-temperature CVD-deposited SiN and sputtered Ti/Au, respectively. **(Paper #11.5, *"Wrap-Gated InAs Nanowire Field Effect Transistor,"* L-E Wernersson et al, University of Lund)**

7. Plastic, Flexible and Stretchable Electronics

The IEDM Emerging Technologies Session is a special session of invited papers focusing on new areas of interest with strong future potential. This year's ET session, on Tuesday afternoon, Dec. 6, is comprised of five papers describing recent findings in the areas of polymer and flexible electronics. Polymer electronics, based on organic semiconductors, have a wide range of applications in electronic systems, displays and sensors. Organic devices and circuits also can be built on flexible substrates and at low cost, which makes them suitable for large-area applications. Recent improvements in organic electronics on several fronts have positioned organic-based electronics at the forefront of several emerging areas:

- **Electronics Everywhere:** A Penn State University paper will present characteristics of organic thin-film electronics well-suited to "electronics-everywhere" applications because of the diversity and flexibility of the devices, their functions and their fabrication processes. In bringing an electronic solution to a problem, the size, form-factor, materials and function of the devices all matter, and organic-based electronics can provide unique capabilities for each of these. **(Paper #18.1, *"Organic Thin-Film Electronics-- Electronics Anywhere,"* Tom Jackson, Penn State University)**

- **Organic Solutions:**

-- A University of Tokyo paper[1] will present the latest findings on **the use of organic materials in MEMS and photonic applications**.
-- A Max Planck Institute paper[2] will discuss **circuit applications of organic devices.** Challenges for future development of large-scale organic circuits include supply voltage and power consumption, stability, modeling, complementary logic, and how to balance performance with and the cost of manufacturing. The paper will discuss how self-assembled monolayer gate dielectrics may be useful for a variety of low-voltage, low-power applications. It will present solutions in several of these areas and compare their performance.
-- A University of Texas paper[3] will present **the advantages of organic materials in sensing, selectivity and resolution**.

[1] **Paper #18.2, *"Flexible, Large-Area Sensors and Actuators with Organic Transistor Integrated Circuits,"* T. Someya et al, University of Tokyo**
[2] **Paper #18.3, *"Organic Circuits on Flexible Substrates,"* Hagen Klauck, Max Planck Institute**
[3] **Paper #18.4, *"Organic and Hybrid Organic/Inorganic Transistors for Chemical and Bio Sensing,"* A. Dodabalapur et al, University of Texas-Austin**

- **Inorganic Solutions:** The last talk of the session will present alternate approaches for obtaining flexible electronics not based on organic semiconductors. A University of Illinois researcher will describe the operational aspects of high-performance flexible transistors and circuits that use printable semiconductors based on single-crystal inorganic materials and carbon nanotubes. Low-cost, soft lithographic techniques based on printing and modeling can be used to fabricate these circuits. **(Paper #18.5, *"Materials and Patterning Techniques for Macroelectronics,"* J. Rogers, University of Illinois)**

Not all of the noteworthy papers on these topics are in the ET session. Here are others:

- **A Display for the Blind:** When we think of computer assistance for the blind, we may think of functions like synthesized speech and voice recognition. But a University of Tokyo group has developed a plastic sheet that "displays" Braille lettering by creating arrays of bumps on its rubber-like surface. They are driven by Braille input, such as from an e-book. The sheet can be rolled up and carried in a pocket. Researchers first built an underlying array of organic pentacene thin-film transistors (TFTs) with top-contact geometry, on PEN or polyimide plastic substrates. (They had 20-µm channel lengths and mobilities of 1 cm^2/Vs.)

Then, actuators were fabricated from conductive polymer. When the transistor beneath an actuator feeds voltage to it, the actuator moves upward. Each actuator has a tiny bubble, or semisphere, attached to it, which in turn pushes up against and deforms a spot on the surface film, a 10-µm thick PDMS film. These actuators are in 2x3 arrays that can form every Braille letter. The entire 4x4 cm^2 display can create a total of 24 Braille letters. This is the first reported integration of active-matrix organic TFT arrays with plastic actuators, and it opens up great possibilities for new types of large-area and flexible electronic displays. **(Paper #5.1, *"A Flexible, Lightweight Braille Sheet Display with Plastic Actuators Driven by an Organic Field-Effect Transistor Matrix,"* Y. Kato et al, University of Tokyo.)**

- **Stretchable Circuits:** Think of the potential uses for elastic, stretchable circuitry -- prosthetic skin, wearable electronic systems, sensor arrays that could be stretched over arbitrary surfaces, and others. Stretchable systems would be possible if arrays of thin-film transistors could be fabricated directly on elastomeric or stretchable substrates. Princeton University researchers made a key advance in this area by fabricating integrated circuits on a soft, elastic silicone substrate (PDMS). Using an all-dry fabrication process, they built a matrix of rigid, mechanically distinct subcircuit islands containing amorphous thin-film silicon transistors. The islands were interconnected with gold conductors laid out in a serpentine fashion. When the substrate is stretched, the rigid device islands protect the transistors from excessive mechanical strain, while the silicone substrate and the interconnect network accommodate most of the strain. **(Paper #5.2, *"Thin Film Transistor Circuits Integrated Onto Elastomeric Substrates for Elastically Stretchable Electronics,"* S. Lacour et al, Princeton University)**

8. A Technological Potpourri

- **MEMS-Based Position-Sensing Cochlear Implant:** Some 100,000 profoundly deaf people worldwide have received cochlear implants. With these, a wire bundle of up to 22 electrodes is inserted into the ear's cochlea to stimulate auditory nerve receptors electrically, bypassing defective hair cells and restoring hearing. Ideally, the implant should avoid damaging any surviving hair cells during insertion, and should hug the interior ear wall to minimize distance to the receptors. If the wire bundle of electrodes could be replaced with a conformal thin-film electrode array of greater density, not only could the user enjoy better sound discrimination but a position-sensing function could be built into the device to allow it to be placed in the ear with high accuracy and with no need for X-ray guidance.

  University of Michigan researchers built such an electrode array using MEMS techniques (microelectromechanical systems). It integrates eight segmented piezoresistive position sensors with an electronic signal-processing chip. An eight-line polymeric cable routes power, control inputs and outputs between the electrode array and an electronics processing unit that incorporates a microprocessor, A/D converter and inductively coupled wireless interface. **(Paper #5.7, *"An Integrated Position-Sensing System for a MEMS-Based Cochlear Implant,"* J. Wang et al, University of Michigan)**

- **MEMS-Based Gas Analyzer:** Chromatography is a process used to detect and analyze various gases. If a wristwatch-sized gas chromatograph could be built it would be useful for security and other applications. A key challenge is to build columns (to separate the gas into fractions) having high sensitivity, high speed, good thermal response and low power usage. University of Michigan researchers used MEMS techniques to build 25-cm-long coils of ultra-low-mass gas columns on a 6mm^2 die that met all of these criteria. They used stress-free PECVD-oxynitride films and a CMOS-compatible process. The columns demonstrated high-performance separation of n-alkane gas mixtures, are capable of multi-second analysis, and have power consumption of <10mW at 100°C in vacuum. The work opens the door to a high-performance and potentially very inexpensive instrument. **(Paper #12.8, *"PECVD-Oxynitride Gas Chromatographic Columns,"* M. Agah et al, University of Michigan)**

- **Self-Assembled 3-D Chips:** 3-D, or multi-level, chips would offer increased performance and packing density plus lower power consumption. But it's hard to make them because of yield and alignment problems. Chips are produced en masse on a wafer. After wafer-processing is completed, the wafer is sawed into individual chips. The good ones are kept while defective ones are discarded. The more good chips on a wafer, the higher its yield. But few if any wafers containing complex chips have a 100% yield. So one or more chips in a multi-level device could be defective, and anyway achieving precise alignment of a stack of them across the entire surface of a wafer would be next to impossible. But researchers from the University of Tohoku in Japan have developed a novel self-assembly technique that may solve these problems.

  In industry parlance, a chip is also called a die. Known good die are temporarily glued to a transfer or "handle" wafer. Other known good die, thinned to just a few microns and with through-wafer copper vias already created, are then stacked onto the original die on the handle wafer using a novel self-assembly technique. The new chips are interconnected with flip-chip processes and this sequence is repeated for as many die as are needed. The researchers say they can stack various chip types of different sizes and thicknesses, such as MEMS devices, sensors, and RF, MMIC, power, analog and logic ICs. As a demonstration, they built a multi-level SRAM test chip with 10 individual memory layers atop one another, aligned within 1µm. **(Paper #14.4, *"New Three-Dimensional Integration Technology Using Self-Assembly Technique,"* T. Fukushima et al, University of Tohoku)**

- **Cool Chips:** Cooling is one way to boost chip performance, but is there an optimum temperature beyond which further cooling yields diminishing returns? What is the best balance between IC cooling and power consumption? University of California-Santa Barbara researchers will present a comprehensive analysis for various nanometer-scale bulk CMOS and SOI technologies. Some conclusions: SOI-based devices are more responsive to cooling; the benefits of cooling increase as technology scales; localized rather than global cooling is more effective for hot-spot management; and the power needed for cooling may be regained from the lower leakage of the cooled devices. **(Paper #41.1, *"Analysis and Implications of IC Cooling for Deep Nanometer Scale CMOS Technologies,"* S-C. Lin et al, UC-Santa Barbara)**

- **28 Megapixel Color Photos?** Researchers from DALSA in the Netherlands have developed a large-area 28 megapixel color CCD image sensor for high-end digital still cameras. The 44mm x 33mm CCD is made possible with a novel on-chip charge-binning concept that until now was reserved for monochrome CCDs. The technology is applicable for cameras designed to be used where high sensitivity, high signal-to-noise and high frame rates are needed, such as for sport photography (motion), digital still images and low-light situations. **(Paper #33.5, *"A 28 Mega Pixel Large Area Full Frame CCD with 2x2 On-Chip RGB Charge-Binning for Professional Digital Still Imaging,"* C. Draijer et all, DALSA Professional Imaging)**

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