

On the Applicability of Single-Walled Carbon Nanotubes as VLSI Interconnects

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Abstract—This paper presents a comprehensive study of the applicability of single-walled carbon nanotubes (SWCNTs) as interconnects in nanoscale integrated circuits. A detailed analysis of SWCNT interconnect resistance (considering its dependence on all physical parameters, as well as factors affecting the contact resistance), the first full 3-D capacitance simulations of SWCNT bundles for realistic very large scale integration (VLSI) interconnect dimensions, and a quantitative evaluation of the importance of inductive effects in SWCNT interconnects are presented. The applicability of carbon nanotube (CNT) based vias (vertical interconnects)—the most realizable CNT interconnects in the current state of the art—is addressed for the first time. It is shown that CNT interconnects can provide 30%–40% improvement in the delay of millimeter-long global interconnects. The applicability of CNT monolayers as local interconnects is found to be much more limited than that reported in the prior literature. Dense CNT bundle global interconnects are shown to offer a 4× reduction in power dissipation while achieving the same delay as optimally buffered Cu interconnects at the 22 nm node. This power saving increases to 8× at the 14 nm node. Furthermore, 3-D finite-element electrothermal simulations show that CNT bundles used as vias in between Cu metal layers can provide large improvement in metal interconnect lifetime by lowering the temperature of the hottest interconnects.

Index Terms—Carbon nanotube (CNT), performance, power, reliability, thermal management, very large scale integration (VLSI) interconnect.

I. INTRODUCTION

SINCE their accidental discovery in 1991 [1], carbon nanotubes (CNTs) have aroused a lot of interest as building blocks for future integrated circuits (ICs) due to their outstanding electrical properties [2], high thermal and mechanical stability, high thermal conductivity, and large current-carrying capacity [3]–[6]. Alongside research efforts into developing *semiconducting* CNT-based transistors [7], *metallic* CNTs (mCNT) have also been suggested as an interconnect material [8], [9]. Several

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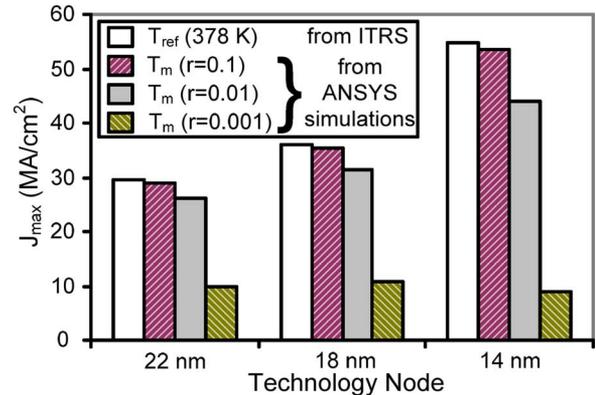


Fig. 1. Maximum allowed rms current density (unipolar ac current stress) for Cu local vias at different metal temperatures. The International Technology Roadmap for Semiconductors (ITRS) provides J_{max} values at 378 K (T_{ref}). J_{max} values at actual metal temperature (T_m) are calculated for the same electromigration lifetime as with ITRS current densities. T_m is obtained from 3-D electrothermal simulations using a commercial finite-element solver Ansys. The current stress for Ansys simulations are obtained using ITRS-specified J_{max} values with different duty ratios (r) as shown.

groups have reported progress on the fabrication of CNT-based interconnects [8], [10], [11], which can alleviate the significant performance and electromigration (EM) reliability concerns in future generations of Cu interconnects [12], [13]. The widening gap between ITRS current-density requirements [14] and the current-carrying capacity of Cu vias—primarily due to the steep rise in parasitic resistance of aggressively scaled Cu interconnects [14]–[16] and rising on-chip metal temperatures—is shown in Fig. 1, indicating the need for identifying alternate interconnect materials for very large scale integration (VLSI).

In this paper, we present a comprehensive study of the applicability of single-walled CNTs (SWCNTs) as VLSI interconnects. The paper is organized as follows. Section II provides a brief introduction to CNT interconnect technology. Section III starts with a review of existing works analyzing the performance of CNT interconnects and presents an equivalent circuit model, based on the Luttinger liquid theory, to calculate the propagation delay of a CNT bundle interconnect. The properties of the equivalent circuit model are discussed, highlighting all underlying assumptions. Salient features of Section III include the impact of all physical parameters on CNT resistance, the first 3-D capacitance simulation results for CNT bundles of realistic VLSI interconnect dimension, and a quantitative analysis of the importance of inductance in calculating CNT interconnect propagation delay.

Based on the equivalent circuit model, the performance of CNT bundles is evaluated in Section IV, and the advantages

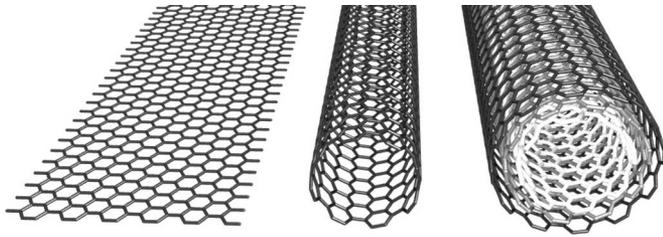


Fig. 2. Structure of a single layer of graphite (graphene) (left), single-walled carbon nanotube (SWCNT) as a rolled-up graphene sheet (middle) and a multiwalled nanotube with three concentric shells (right).

they can offer at different domains of on-chip interconnects are shown. This performance analysis provides a clear insight into the applicability of CNT interconnects in the form of dense or sparse bundles as well as monolayers. Section IV also addresses the impact of CNT bundle interconnects on global interconnect power dissipation—a critical concern for future technology generations and various interconnect-centric microarchitectures. Noting recent progress in the fabrication of CNT vias, Section V addresses the concept of *hybrid CNT/Cu* interconnects [9]—employing CNT vias in tandem with Cu metal layers—and its remarkable advantages from a reliability/thermal-management perspective. This paper is unique in its key findings with regard to interconnect power dissipation and thermal analysis of the back-end interconnect stack. Section VI concludes with a summary of our findings and lays out the process technology requirements that must be met in order to make SWCNT interconnects a reality.

II. CNT INTERCONNECTS

The basic structure of a CNT—as a rolled-up graphene sheet to form a SWCNT, or several concentric tubes to form a multiwalled CNT (MWCNT)—is shown in Fig. 2. Changing the direction of roll-up leads to different “chiralities,” which are identified by the chiral indexes (m, n) [17], [18] (when either m or n is zero it is called *zigzag* chirality, $m = n$ is called *armchair*, while all other nanotubes are called *chiral*). SWCNTs are metallic when the difference between the chiral indexes is an integer multiple of 3 ($m - n = 3i$), and are semiconducting otherwise. Hence, armchair SWCNTs are always metallic. Metallic CNTs have aroused a lot of interest as VLSI interconnects of the future [8]–[11], [19]–[22], because of their extremely desirable electrical and thermal properties. CNTs have shown current-carrying capacity in excess of 10^{10} A/cm² without any signs of damage even at an elevated temperature of 250 °C [3], [23], thereby eliminating the EM reliability concerns that plague nanoscale Cu interconnects.

Although the current-carrying capacity of an isolated CNT is much greater than that of Cu, it has a high resistance (theoretical minimum of 6.45 k Ω [24], [25]). In practice, the observed resistance of an individual CNT can be much higher [25], [26], due to the presence of imperfect metal–nanotube contacts. The high resistance of an individual CNT necessitates the use of a *bundle* (rope) of CNTs conducting current in parallel to form a low-resistance interconnect [8], [10], [11].

The work by Kreupl and coworkers [8], [19] proposed a method for growing MWCNT bundles by chemical vapor depo-

sition (CVD) from the bottom of vias and contact holes using an iron-based catalyst. In an alternative bottom-up process [11], MWCNTs are first grown (using HF-CVD) at prespecified locations, then gap-filled with oxide, and finally planarized. The high temperature (700 °C) during CNT growth [8] has been lowered to 510 °C in [19], and more recently to a low of 365 °C in [27]. Advances have also been reported on the reduction of metal–nanotube bundle contact resistance [22], integration with ultra-low K dielectrics [27], CNT through-silicon-vias [28], and densification techniques for SWCNT [29] and MWCNT [30] bundles.

While MWCNT bundles are easier to fabricate, dense metallic SWCNT bundles have greater advantages in terms of interconnect performance [31] and reliability [32]. SWCNT bundle fabrication has been difficult due to the low fertility of catalyst particles for SWCNT growth. It has recently been shown that the fertility of the growth catalyst can be increased by addition of water [33] or oxygen [34]. Thus, homogeneous SWCNT films have been developed by assembling SWCNTs into a dense “carbon nanotube wafer,” enabling integration of nanodevice systems by lithography [35]. Nevertheless, the fabrication of on-chip SWCNT interconnects still poses several challenges because of the need for low-thermal-budget dense metallic nanotube bundles.

III. MODELING AND ANALYSIS OF SWCNT INTERCONNECTS

As the interest in CNT-based interconnects gains momentum, this paper addresses the need to identify the domains of on-chip interconnections (local, intermediate, and global interconnects and vias), where this technology has the potential to replace Cu. It is shown that the requirements from SWCNT process technology vary significantly with the interconnect application that is targeted. This paper analyzes the performance, power, and reliability of SWCNT bundle interconnects in comparison with Cu, taking into account their advantages as well as practical limitations, and lays out the process requirements to make it a viable interconnect technology.

A. Previous Work

The imminent thermal/reliability issues of Cu vias and contacts and the advantages of CNT bundle vias have been reported in [12].

The analysis in [36] considers a flat array of CNTs [Fig. 3(b)], and reports that CNT interconnects have much larger delay than Cu. A similar analysis in [37] arrives at the same conclusions. However, the comments by Li *et al.* [38] show that the analysis presented in [36] and [37] has several drawbacks. Many other works in the published literature have shown that CNT-based interconnects compare favorably with Cu. Their contributions and limitations are discussed in the following paragraphs.

The superior performance of CNT bundle interconnects as compared with Cu has been shown in [39] and [40]. However, these works neglect practical limitations such as the low density of metallic nanotubes and the presence of imperfect metal–nanotube contacts. Moreover, it is assumed that CNT bundles always have the same capacitance as Cu wires. The work in [41]

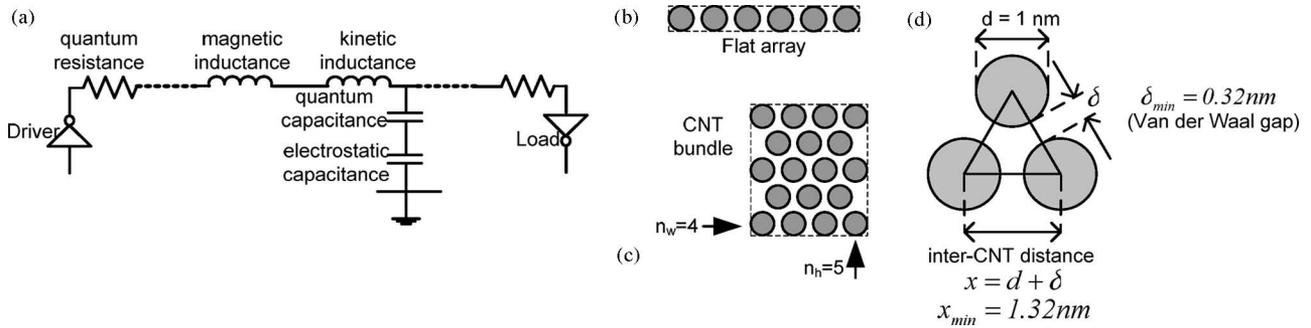


Fig. 3. (a) Equivalent circuit model for an isolated SWCNT [51], for length less than the mean free path of electrons. (b) CNT arrays and (c) CNT bundles increase the number of nanotubes to reduce effective resistance (n_w and n_h denote number of columns and rows in the bundle, respectively). (d) Dense triangular packing of CNTs with minimum separation δ_{\min} (Van der Waal's gap) [54]. Varying density of metallic CNTs is modeled using $x > x_{\min}$, where x is the center-to-center distance between adjacent CNTs.

provides a more comprehensive analysis of the performance of CNT interconnects taking into account these limitations, but uses an empirical model to calculate the CNT bundle capacitance. More realistic capacitance calculations have recently been shown for a 10-nm-wide CNT bundle [42], [43]. However, the effect of bundle geometry or aspect ratio for more realistic VLSI interconnect dimensions is not known.

The resistance calculations in [43] and [44] assume that the saturation current in a CNT is independent of its length. However, this assumption is not supported by measurements (see Section III-B1a). This paper relies on published experimental data to show that the low-voltage bias resistance is valid for most CNT bundle interconnects. This, however, may not be valid for CNT monolayer interconnects that have been proposed as efficient local interconnects up to 20 μm lengths [42], [43], [45]. The analysis in this paper shows that the high resistance of SWCNT monolayers limits their applicability to the shortest local interconnects, which are driven by minimum-sized drivers (less than 1- μm -long interconnects at advanced technology nodes). While the diameter dependence of SWCNT resistance has been discussed in [46], this paper discusses the impact of other important physical parameters such as temperature, contact geometry, and properties of the contact metal.

The importance of considering inductance in CNT interconnect delay calculation has been addressed qualitatively in [47] and quantitatively in [43]. However, the impact of drivers that are critical for such an evaluation has been neglected. We present a realistic quantitative evaluation of the importance of inductance in CNT interconnect delay computation, taking into account the driver impedance, line impedance, and the characteristic wave impedance. The mutual inductance between nanotubes of a bundle has been considered in [48] by assuming each nanotube as a solid metallic conductor. However, this model does not correctly capture the high-frequency current distribution inside a CNT bundle [49]. In this paper, we neglect the mutual inductance between nanotubes of a bundle. However, as discussed in Section III-C, neglecting this mutual inductance will not have an adverse impact on the results shown here.

While most prior works address only the performance of CNT interconnects, the work in [50] highlights their advantages in terms of reliability and back-end thermal management as well.

This paper provides a complete analysis of the applicability of SWCNT bundles at different domains (local, intermediate, and global) of VLSI interconnects. Some of the main contributions in this paper are CNT interconnect resistance modeling considering its dependence on all physical parameters, detailed discussion of factors affecting contact resistance of SWCNT interconnects, full 3-D capacitance simulation of CNT bundles for realistic VLSI interconnect dimensions, a quantitative discussion of the importance of inductive effects, analysis of the repeater power dissipation in buffered global interconnects, and an evaluation of CNT vias, which are already being fabricated by several research groups.

B. Equivalent Circuit Parameters for SWCNT Bundle Interconnects

The equivalent circuit model parameters for an isolated SWCNT of length smaller than the mean free path of electrons [51] are shown schematically in Fig. 3(a). This model is based on the Luttinger liquid theory [52], which describes interacting electrons in a 1-D conductor (since the commonly used Fermi liquid theory breaks down in 1-D systems [53]). Besides, the well-known magnetic inductance and electrostatic capacitance, the quantum resistance, quantum capacitance, and kinetic inductance are important considerations for low-dimensional systems such as CNTs.

As mentioned in Section II, the high resistance of an isolated CNT necessitates the use of a bundle of CNTs [Fig. 3(c)] to form a low-resistance interconnect. The minimum intertube spacing observed in SWCNT bundles is 0.32 nm, characteristic of Van der Waals intertube binding [54]. This close-packed structure, shown schematically in Fig. 3(d), is the configuration considered in the analysis of CNT interconnects in this paper. In practical reality, not all CNTs of such a bundle are metallic. Moreover, other fabrication techniques do not yield such densely packed CNT bundles. Sparsely populated bundles and the presence of nonmetallic CNTs (which do not contribute to current conduction) are accounted for by taking a larger center-to-center distance between adjacent mCNTs (x): $x > x_{\min}$ [Fig. 3(d)]. The electrical properties and equivalent circuit parameters for such a bundle need careful analysis in order to ascertain the applicability of CNTs as VLSI interconnects of the future. This

requires detailed modeling of the bundle resistance, capacitance, and inductance while incorporating fundamental physics of low-dimensional conductors. The models and their components are explained in detail in the following subsections.

1) SWCNT Interconnect Resistance Modeling:

a) *Resistance of an isolated CNT*: From the Landauer approach, the conductance of an isolated CNT can be modeled by $G = 2(e^2/h)MT$ [24], where e is electronic charge, h is Planck's constant, M is the number of allowed channels for transport, and T is the transmission probability. The factor of 2 accounts for spin degeneracy (spin up and spin down). An SWCNT has two conducting channels ($M = 2$). Hence, the lowest possible resistance of an isolated SWCNT, assuming perfect metal–CNT contacts ($T = 1$), is given by [24]

$$R_Q = \frac{h}{4e^2} = 6.45 \text{ k}\Omega. \quad (1)$$

This is the fundamental quantum of resistance associated with an SWCNT of length less than the mean free path of electrons [55] ($l < \lambda_{\text{CNT}}$), which is typically $1 \mu\text{m}$ [8], [56], [57]. For such lengths, electron transport within the nanotube is essentially ballistic and resistance is independent of length. R_Q for a CNT is equally divided between the two metal–nanotube contacts (assuming identical contacts) on either side. However, for lengths $l > \lambda_{\text{CNT}}$, scattering leads to an additional resistance of $(h/4e^2)l/\lambda_{\text{CNT}}$ [58], which yields a distributed resistance per unit length (also confirmed by experimental observations [57], [59])

$$R_S(\text{p.u.l.}) = \frac{h}{4e^2} \left(\frac{1}{\lambda_{\text{CNT}}} \right). \quad (2)$$

i) *Voltage bias dependence of SWCNT resistance*: The resistance of a nanotube is known to be a function of the voltage bias across it. At high voltages, resistance increases due to enhanced phonon scattering of high-energy electrons [57]. The inset in Fig. 4 shows the monotonic increase in CNT resistance (R_{CNT}) as the voltage bias (V_{bias}) increases, following the relation [60]

$$R_{\text{CNT}} = R_{\text{low-bias}} + \frac{V_{\text{bias}}}{I_0} \quad (3)$$

where $R_{\text{low-bias}}$ is the CNT resistance at low bias (around 0 V) and I_0 is the saturation current (current does not increase beyond I_0 even if V_{bias} is increased). For a $1\text{-}\mu\text{m}$ -long CNT, I_0 is found to be around $25 \mu\text{A}$ [57], [60]. This is also the theoretically calculated value of I_0 [60]. However, the data in [57], [61] show that I_0 varies with CNT length.

In interconnect applications, the bias dependence of R_{CNT} can lead to an (instantaneous) increase in resistance. In order to quantify this effect, we first calculate $V_{\text{Limit}10\%}$ —the largest value of V_{bias} for which the increase in R_{CNT} is less than 10% of $R_{\text{low-bias}}$ —using

$$\begin{aligned} V_{\text{Limit}10\%} &= I_0(1.10R_{\text{low-bias}} - R_{\text{low-bias}}) \\ &= 0.1I_0R_{\text{low-bias}}. \end{aligned} \quad (4)$$

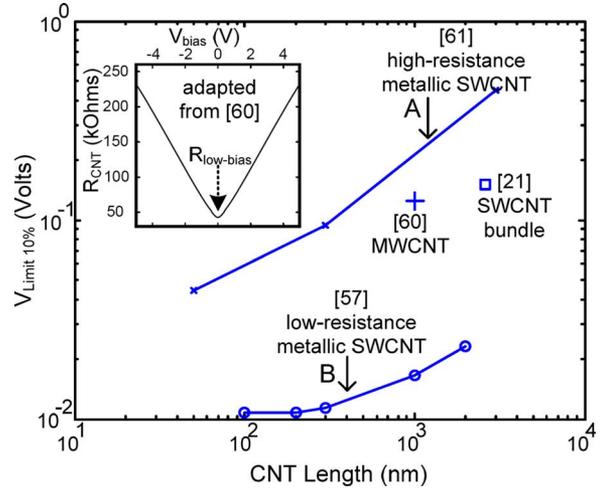


Fig. 4. (Inset) Bias dependence of CNT resistance. At very small values of V_{bias} , around 0 V, $R_{\text{CNT}} = R_{\text{low-bias}}$ is nearly constant. For larger values of V_{bias} , R_{CNT} increases monotonically. (Main figure) $V_{\text{Limit}10\%}$, calculated using (4), is based on published experimental data for I_0 and $R_{\text{low-bias}}$ from multiple sources. Curve B [57] is for very-low-contact-resistance ($< 1 \text{ k}\Omega$) SWCNTs. For high-contact-resistance ($\sim 15 \text{ k}\Omega$) CNTs, V_{Limit} is higher (curve A). In curve B, pessimistic lower limit of $I_0 = 15 \mu\text{A}$ is used. I_0 can be much higher for short CNTs [57]. Hence this curve represents a lower bound on $V_{\text{Limit}10\%}$.

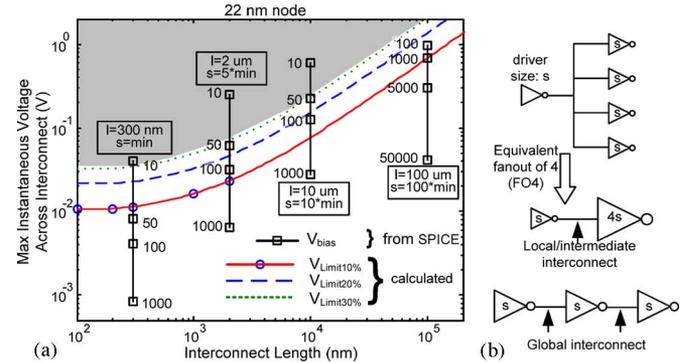


Fig. 5. (a) Maximum instantaneous voltage drop V_{bias} (solid vertical lines and square symbols) across a switching CNT bundle interconnect for different lengths (l) and driver sizes (s), from SPICE simulation at 22 nm node ($V_{\text{dd}} = 1\text{V}$). Numbers adjacent to squares are the number of metallic CNTs in the bundle. Curves show V_{Limit} for 10% (solid), 20% (dashed), and 30% (dotted) increase in R_{CNT} . Circles correspond to data points on Curve B in Fig. 4. Curves are produced using linear extrapolation since data beyond few μm lengths are not available. (b) Circuit schematic for SPICE simulation.

Based on published experimental data from various sources, Fig. 4 plots the calculated values of $V_{\text{Limit}10\%}$. The use of experimental data allow us to account for the length dependence of I_0 . It can be observed that the value of $V_{\text{Limit}10\%}$ increases as CNT length increases. This is because longer CNTs have higher $R_{\text{low-bias}}$.

Fig. 5 compares the *actual* instantaneous voltage drop across a CNT bundle interconnect, V_{bias} , to the limiting values of voltage bias calculated for 10%–30% increase in CNT resistance ($V_{\text{Limit}10\%} - V_{\text{Limit}30\%}$). V_{bias} for CNT interconnects of different lengths and driver sizes (for local, intermediate, and global levels), with varying number of CNTs per bundle, are

obtained from SPICE simulations for the configurations shown in Fig. 5(b). $V_{\text{Limit}10\%} - V_{\text{Limit}30\%}$ are obtained from (4), corresponding to the data for curve B in Fig. 4. As an example, if V_{bias} lies in the shaded region above the curve $V_{\text{Limit}30\%}$, the instantaneous increase in its resistance will be greater than 30%.

It is found that for very short interconnects ($l = 300$ nm, driven by minimum-sized drivers), as few as 50 CNTs in a bundle lead to a voltage drop less than $V_{\text{Limit}10\%}$. In other words, these interconnects will have less than 10% instantaneous increase in resistance. This is because most of the voltage drop occurs across the large driver resistance. For longer interconnects, with driver size five or ten times the minimum size, a few 100 CNTs in a bundle are needed to ensure that the instantaneous increase in resistance is less than 10%. For wide global interconnects, which can easily accommodate several thousands of CNTs, the worst-case effect of V_{bias} on resistance is negligible.

Hence, for all practical purposes, the resistance of CNT bundle interconnects is independent of voltage. However, this may not be true for CNT monolayer interconnects [42], [43], [45], which can accommodate fewer than 20 CNTs. It is important to note that the voltage drop across an interconnect is transient, and the instantaneous increase in resistance discussed here does not translate into a commensurate increase in interconnect delay.

ii) Imperfect metal–nanotube contact resistance (R_C): The observed dc resistance of a CNT (at low bias) is much higher than the resistance R_Q or R_S shown in the previous sections, due to the presence of imperfect metal–nanotube contacts. Experimental reports on the nature of contacts to CNTs have shown varied results, with Schottky contacts reported for Ti [62] and ohmic contacts reported for Au [63] and Pd [61], [64]. Experimental evidence shows that the nature of contacts also depends on nanotube diameter [65]. A rational function fit for the data in [65], with nanotube diameter as a parameter, is shown in [46]. However, the metal–CNT contact properties depend on several other physical parameters, such as contact geometry (planar versus embedded contacts shown in Fig. 6), contact metal work function, and temperature.

A theoretical analysis of contacts between metals and semi-conducting nanotubes is presented in [66], showing the effect of weak band realignment due to charge transfer at the contacts. A transition in the nature of the contact from a Schottky barrier to an ohmic contact is shown as the diameter increases. The diameter at which this transition occurs, or the crossover diameter (d_{S-O}), is given by [66] the following equation:

$$d_{S-O} = d_0 \left(1 + \alpha \sqrt{\frac{k_B T}{\phi_m - \phi_{\text{CNT}}}} \right) = d_0 \left(1 + \frac{\delta d}{d_0} \right) \quad (5)$$

where d_0 is the crossover diameter if no charge transfer were considered, k_B is Boltzmann's constant, T is temperature, and $\phi_m - \phi_{\text{CNT}}$ is the difference in work function between metal contact and the CNT. α is a parameter that depends on the

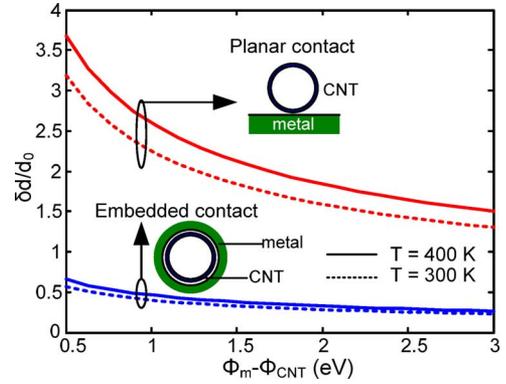


Fig. 6. Increase in crossover diameter, δd , (expressed as a fraction of d_0) at which Schottky–ohmic transition occurs, as a function of the difference between metal–CNT work functions ($\Phi_m - \Phi_{\text{CNT}}$), for different contact geometries and temperatures.

contact geometry ($\alpha \approx 14$ for planar contacts, $\alpha \approx 2.5$ for embedded contacts [67]).

In order to provide good ohmic contacts to a wide range of nanotube diameters, d_{S-O} (and hence δd) must be small. Fig. 6 shows the effect of contact geometry, temperature, and metal work functions on the ratio $\delta d/d_0$. Evidently, it is desirable to have embedded contacts with a large difference in metal–CNT work functions.

For small-diameter metallic SWCNTs, the metal–nanotube chemical bonding significantly perturbs the CNT due to high curvature and chemical reactivity of these tubes, leading to a large tunneling barrier at the contacts [66], which makes the contact resistance of metallic SWCNTs also diameter dependent. Both experimental [65] and theoretical [66] analyses have shown that it is very difficult to obtain good ohmic contacts for metallic SWCNTs with small diameter around 1 nm. Hence, even though small contact resistances have been achieved in some laboratory experiments [56], [68], it is important to consider the possibility of large (imperfect) metal–nanotube contact resistance in the practical application of CNT interconnects.

The contact resistance R_C is divided equally between the two contacts and is in series with the quantum resistance R_Q . The total resistance of an isolated SWCNT is given by the following:

$$R_{\text{CNT}} = \left\{ \begin{array}{ll} R_C + R_Q, & \text{if } l \ll \lambda_{\text{CNT}} \\ R_C + R_Q + lR_S, & \text{if } l > \lambda_{\text{CNT}} \end{array} \right\}. \quad (6)$$

Evidently, the resistance associated with a single CNT is too high for realizing an interconnection. Hence, it is necessary to have a bundle of CNTs to lower the effective resistance.

b) Resistance of an SWCNT Bundle Interconnect: The effective resistance of a CNT-bundle with n_{CNT} mCNTs is given by

$$R_{\text{bundle}} = \frac{R_{\text{CNT}}}{n_{\text{CNT}}}. \quad (7)$$

It is assumed here that the interaction between adjacent CNTs of a bundle is weak. Experiments on CNT bundles have shown a large temperature-independent coupling resistance (\sim several

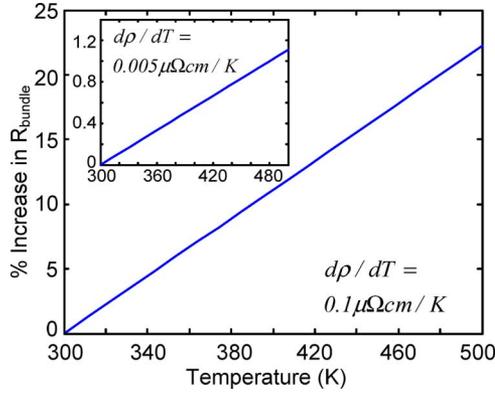


Fig. 7. Increase in SWCNT bundle resistance (as a% of resistance at 300 K) with temperature, calculated using actual measured rate of increase [72] for SWCNT bundle with $\sim 40\%$ metallic CNTs (main figure) and theoretically predicted rate of increase for densely packed metallic SWCNT bundle (inset).

M Ω [59] for defect-free nanotubes), characteristic of direct tunneling between the nanotubes. Hence, the CNTs of a bundle are only weakly coupled and can be safely assumed to carry currents independent of each other.

i) Temperature dependence of CNT bundle resistance: The resistance of a 3- μm -long isolated metallic SWCNT has been shown to increase superlinearly with temperature from about 50 to 290 K [69]. This nonlinearity has been attributed to optical phonon absorption in a temperature-dependent model in [70] with very large increase in resistance predicted for longer CNTs in the range of 400 K (typical on-chip temperatures), although this is not supported by data. On the other hand, measurements on SWCNT *bundles* have consistently shown linear increase in resistance with temperature [71], [72] for temperatures as high as 580 K over a wide range of CNT bundle lengths.

The calculated rate of change of resistivity with temperature for a densely packed SWCNT bundle [72] is $d\rho/dT = 0.005 \mu\Omega\text{-cm/K}$, while experimental measurements have shown $d\rho/dT \sim 0.1 \mu\Omega\text{-cm/K}$ [72]. The discrepancy apparently arises from the presence of semiconducting CNTs as well as from inter-CNT interactions. Fig. 7 shows that, for these values of $d\rho/dT$, SWCNT bundle resistance increases by about 10% from room temperature to 400 K (Cu resistance increases by about 40% in the same temperature range).

ii) Diameter dependence of CNT bundle resistance: Semiconducting CNTs have a large chirality-induced primary bandgap, which is inversely proportional to nanotube diameter d , as well as a curvature-induced secondary bandgap, which scales as $1/d^2$ [73]. Semimetallic nanotubes have a very small curvature induced bandgap, which scales as $1/d^2$. Armchair nanotubes (chiral indexes $m = n$), however, are truly metallic as they have zero bandgap, independent of diameter [74].

The small diameter of SWCNTs, and the absence of a controlling gate bias in interconnect applications, means that only the metallic nanotubes in an SWCNT bundle interconnect contribute to conduction. Hence, the variation in bandgap with nanotube diameter will not affect the performance of SWCNT bundle interconnects.

The electron mean free path of a CNT, which has a large impact on CNT resistance, increases linearly with nanotube

diameter [75]. In the scope of this study, we assume that all single-walled nanotubes have 1 nm diameter and a mean free path, $\lambda_{\text{CNT}} = 1 \mu\text{m}$, the typical value reported in the literature.

Fig. 8(a) shows that at the local level, for mCNT density as low as 30%, CNT bundle resistance can be lower than that of Cu interconnects when R_C is low. With high R_C , higher mCNT densities are needed. Moreover, as long as the CNT bundle resistance is less than that of Cu, the resistance can also be considered independent of the bias voltage (falling outside the shaded regions). With technology scaling, fewer nanotubes can be accommodated in the smaller cross sections, thereby increasing the bundle resistance, but the Cu interconnect resistance also increases proportionately. Hence, the same trends in comparison with Cu are seen for 22 nm node and 14 nm node (inset). However, as the shaded region of the plot expands at advanced technology nodes, higher mCNT densities will be necessary as technology scales in order to keep bundle resistance independent of voltage bias conditions.

Fig. 8(b) shows that for densely packed bundles at the global interconnect level, the bundle resistance is less than that of Cu for a wide range of interconnect lengths, even for low mCNT density (45%). R_C as large as 10 k Ω does not have a large impact on the overall bundle resistance, while the relative impact of $R_C = 100 \text{ k}\Omega$ also becomes small for long interconnects. This is because R_C is independent of length whereas the scattering resistance component (lR_S) increases linearly with length, as shown in (6). The resistance of maximum width global interconnects (width $\sim 1 \mu\text{m}$) with dense CNT bundles stays in the range of 40%–50% of Cu global interconnects and does not change appreciably over length or with technology [Fig. 8(c)]. Even with imperfect metal–CNT contacts, CNT bundle resistance $\sim 50\%$ of Cu wire resistance is easily achieved for long, wide global interconnects.

2) SWCNT Interconnect Capacitance Modeling: An external voltage applied to a 1-D conductor affects its electrochemical potential energy in two ways. The change in electrostatic potential energy when a charge δQ is added to the conductor is given by $(\delta Q)^2/(2C_E)$, where C_E is its *electrostatic capacitance*. Due to the low density of states at the Fermi energy level, the charge δQ has to occupy available quantum energy states above the Fermi energy level. The additional quantum energy required to add charge δQ to these higher energy states can be modeled as $(\delta Q)^2/(2C_Q)$, where C_Q is its *quantum capacitance* [17]. Hence, the net change in electrochemical potential energy is given by $\delta E = (\delta Q)^2/(2C_E) + (\delta Q)^2/(2C_Q)$, which indicates that the effective capacitance of a 1-D conductor is given by a series combination of C_E and C_Q [Fig. 9(a)].

The quantum capacitance depends on the density of states at the Fermi energy level $D(\mu)$. For a 1-D conductor, $D(\mu) = 1/(\pi\hbar v_F)$, where only one spin direction for electrons has been taken into account. Here, v_F is the Fermi velocity ($v_F \approx 8 \times 10^5 \text{ m/s}$) and $2\pi\hbar = h$, the Planck's constant. Hence, C_Q is given by [17] and [51]:

$$C_Q(\text{p.u.l.}) = e^2 D(\mu) = \frac{e^2}{\pi\hbar v_F} = \frac{2e^2}{\hbar v_F}. \quad (8)$$

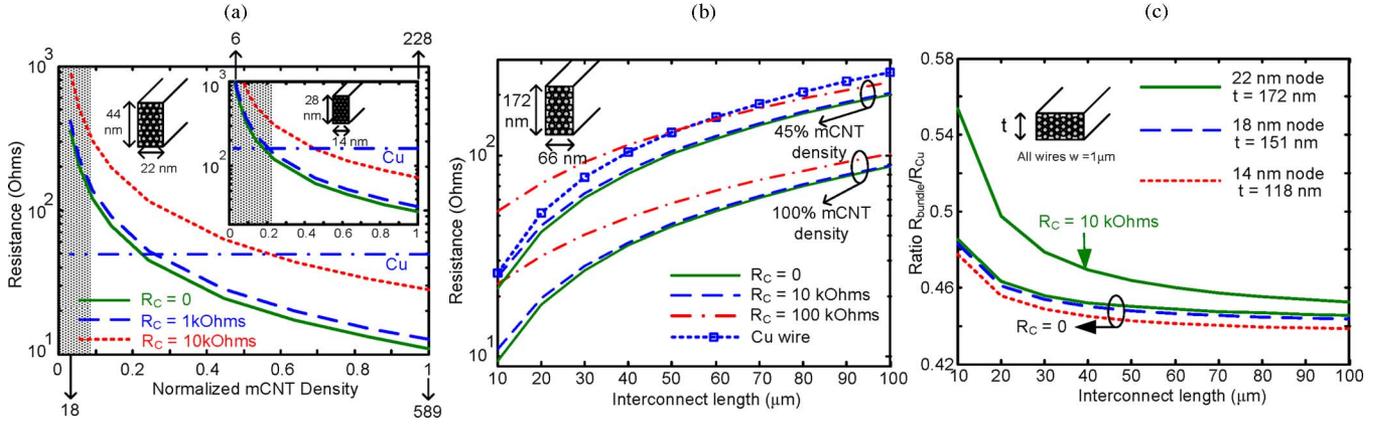


Fig. 8. (a) CNT bundle local interconnect resistance (length = $1 \mu\text{m}$) as a function of metallic CNT (mCNT) density (normalized to maximum density), at 22 nm node (main figure) and 14 nm node (inset). Length = $1 \mu\text{m}$, hence CNTs are assumed to be ballistic. Bundle dimensions and Cu wire resistance for identical dimensions are shown. Temperature = 300 K. In shaded regions, resistance may become dependent on voltage bias (see Fig. 5). Number of CNTs in bundle is shown with arrows. (b) Resistance of dense CNT bundle minimum-width global interconnect as a function of length at 22 nm node, for different values of R_C and m-CNT density. (c) Ratio of densely packed CNT bundle resistance to Cu wire resistance for maximum-width global wire ($w \sim 1 \mu\text{m}$), as a function of interconnect length and technology node. Temperature = 300 K for all figures.

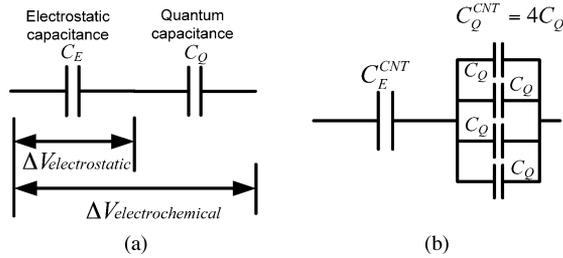


Fig. 9. Effective capacitance model of (a) general 1-D conductor and (b) an isolated SWCNT with four parallel conducting channels.

Note that for conventional 3-D conductors, the density of states $D(\mu)$ is large; hence, C_Q is large and its effect on overall capacitance is negligible.

Since an SWCNT has two conducting subbands at the Fermi energy with two electronic spin directions, each SWCNT has four 1-D conducting channels [47]. The net quantum capacitance of a CNT is given by a parallel combination of four C_Q elements, thus

$$C_Q^{\text{CNT}} (\text{p.u.l.}) = 4C_Q (\text{p.u.l.}) \approx 400 \text{ aF}/\mu\text{m}. \quad (9)$$

In order to calculate the equivalent capacitance of an SWCNT bundle, we assume that the n_{CNT} nanotubes in the bundle are noninteracting and carry equal currents independent of each other [59]. Under this assumption, the SWCNT bundle is composed of $4n_{\text{CNT}}$ 1-D conductors (each nanotube contributes four 1-D channels). For an SWCNT bundle, the effective quantum capacitance is given by

$$C_Q^{\text{bundle}} = 4n_{\text{CNT}} C_Q. \quad (10)$$

The electrostatic capacitance of a CNT, C_E^{CNT} , can be found by considering it as a thin cylindrical wire and is dependent on its surrounding environment. For the configuration shown in

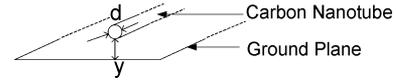


Fig. 10. Isolated conductor, diameter “ d ,” over a ground plane at a distance “ y ” below it ($y \gg d$).

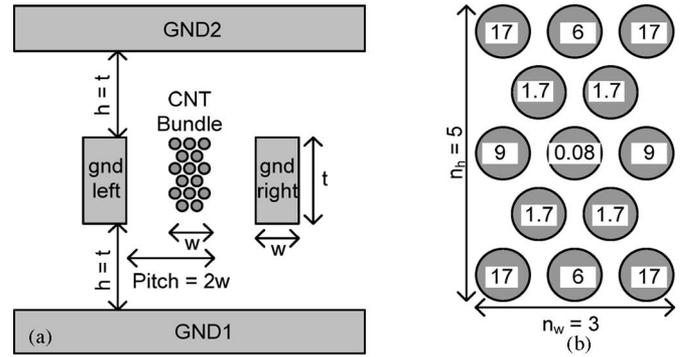


Fig. 11. (a) Cross-sectional schematic of interconnect structure. The values of the geometrical parameters are obtained from ITRS [14]. (b) Electrostatic capacitance in $\text{aF}/\mu\text{m}$ for each nanotube in a bundle with respect to the surrounding ground conductors. Thirteen CNTs densely packed: $n_w = 3$, $n_h = 5$, bundle width = 4 nm, and CNT diameter = 1 nm. Adjacent conductors are assumed to be Cu.

Fig. 10, the expression for C_E (per unit length) is given by [51]

$$C_E^{\text{CNT}} (\text{p.u.l.}) = \frac{2\pi\epsilon}{\cos h^{-1}(y/d)}. \quad (11)$$

For $d = 1 \text{ nm}$, $y = 1 \mu\text{m}$, $C_E^{\text{CNT}} \approx 30 \text{ aF}/\mu\text{m}$.

a) *Electrostatic Capacitance of an SWCNT Bundle:* Fig. 11(a) shows a cross section of the interconnect structure considered for electrostatic analysis of mCNT bundle interconnects. Two immediately adjacent wires (left and right, held at ground potential) parallel to the CNT bundle are considered. Top and bottom ground planes represent the orthogonal metal layers, although electrostatic coupling to adjacent (left/right) interconnects is dominant for wires with aspect ratio $t/w > 1$. For

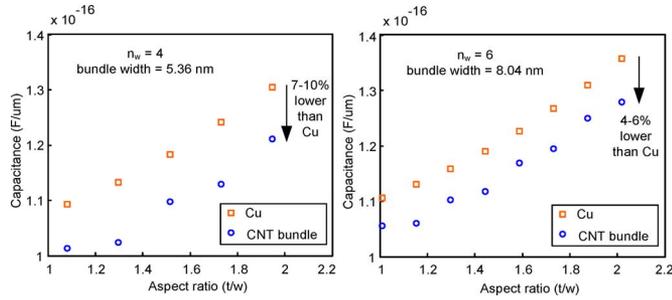


Fig. 12. Total electrostatic capacitance of densely packed SWCNT bundles with respect to neighboring ground conductors as a function of aspect ratio [see Fig. 11(a)], for two different bundle widths. Capacitance of Cu wires of equivalent dimensions as the CNT bundles is shown for comparison.

the electrostatic analysis, each CNT is treated as a metal with equal potential over the tube, similar to the approach in [76]. For the sake of simplicity, it is assumed that all CNTs are held at the same potential. Contrary to the claim in [43], this assumption is valid only when the contacts to all nanotubes within a bundle are identical and each CNT has the same mean free path. Under this assumption, the coupling capacitance between adjacent CNTs in the same bundle does not come into play.

Fig. 11(b) shows the total electrostatic capacitance with respect to left/right neighbors and top/bottom ground planes for each CNT in the bundle. These numbers are obtained from 3-D simulations on square-cross-section wires of dimensions equivalent to the 1 nm nanotubes using FastCap [77]. The numbers clearly show that inner nanotubes in the bundle are electrostatically shielded from the adjacent ground conductors. The edge nanotubes are the dominant contributors to the effective electrostatic capacitance of the CNT bundle. Hence, in order to facilitate extensive simulation of large CNT bundles, the shielded inner nanotubes can be ignored.

It must be noted that *semiconducting* nanotubes will always be present in a CNT bundle. Since no gate-bias voltage is applied to an interconnect, we can assume that the semiconducting CNTs are insulating. Hence, capacitance between metallic and semiconducting CNTs within a bundle will not be important. In this scenario, the semiconducting CNTs can still act as additional dielectric boundaries modifying the inter-mCNT capacitance of the bundle. However, this capacitance between mCNTs of the same bundle is also not important since they are assumed to be equipotential. The amount of charge injected into the semiconducting CNTs at low bias and the equipotential assumption for mCNTs in the bundle are all dependent on the quality, material, and uniformity of the metal–nanotube contacts. Although these may be important considerations for high accuracy, we ignore these modifications for the sake of simplicity.

Fig. 12 compares the net electrostatic capacitance of densely packed CNT bundles with that of equivalent-dimension Cu wires with respect to neighboring ground conductors. The dimensions of interconnects are kept small due to simulator time and memory limitations (other geometrical parameters shown in Fig. 11(a) are proportionately scaled). The results show that the capacitance of dense CNT bundles is lower (but within 10%) than that of Cu wires, for different values of aspect ratio.

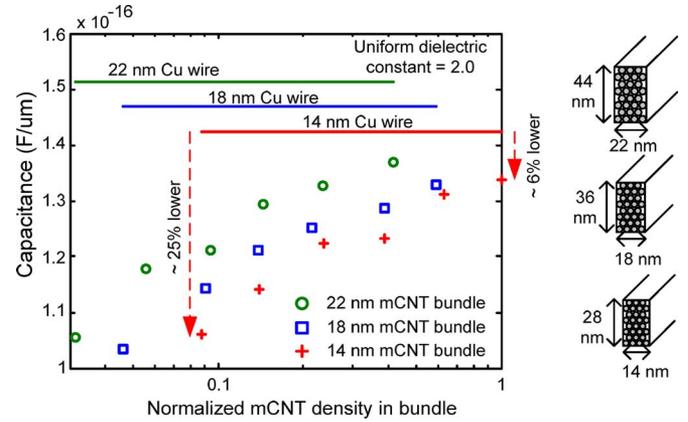


Fig. 13. Total electrostatic capacitance of realistic dimension SWCNT bundles at different technology nodes as a function of bundle density (normalized with respect to maximum density). The dimensions “ w ” and “ t ” are shown alongside; interconnect geometry is shown in Fig. 11(a).

Fig. 13 shows the comparison between CNT bundles and Cu wires of realistic dimensions below the 22 nm technology node. In the case of maximally dense bundles, the CNT bundle electrostatic capacitance is still found to be within 10% lower than that of Cu. However, as the mCNT density is reduced (assuming uniform distribution of mCNTs in the bundle), the capacitance becomes significantly lower than that of Cu interconnects.

It is important to note that the use of accurate field solvers for calculating capacitance is limited to configurations with relatively small number of conductors due to memory and time limitations (e.g., in Fig. 13, we could not obtain results for a completely dense bundle at 22 and 18 nm nodes due to the large number of CNTs in the bundle). This limitation becomes worse for wide global wires, which can accommodate thousands of CNTs. Hence, in the delay analysis of wide global interconnects in Section IV, we will use the earlier deduction that Cu wire capacitance provides an upper-bound (within 10%) for the capacitance of a *dense* CNT bundle. This deduction is supported by the results in Fig. 12 as well.

The *effective capacitance* of an SWCNT bundle interconnect (C_{bundle}) is given by the series combination of its electrostatic capacitance and quantum capacitance. As shown in Fig. 14, the effective SWCNT bundle capacitance is nearly equal to its electrostatic capacitance and the effect of the quantum capacitance is small.

3) SWCNT Interconnect Inductance Modeling:

a) *Inductance of an isolated SWCNT*: The inductance of a conductor models the energy associated with the motion of electrons carrying current (I) through it. The energy stored in the magnetic field generated by the current is given by $(1/2)L_M I^2$, where L_M is its *magnetic inductance*. For a net current to flow through a conductor, there has to be an excess of electrons moving in the direction opposite to current flow. In a 1-D conductor that has low density of states at the Fermi energy level (E_F), these excess electrons can only be added at available quantum energy states above E_F , and thus have a higher kinetic energy. This additional kinetic energy, stored in the moving electrons responsible for current flow in a 1-D conductor, is modeled

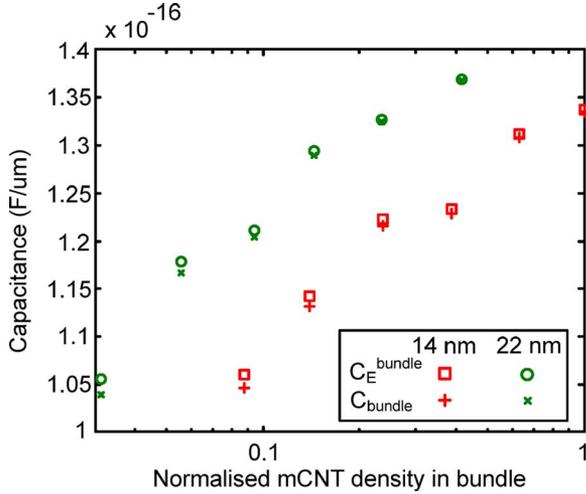


Fig. 14. CNT bundle electrostatic capacitance C_E^{bundle} in comparison with effective capacitance C_{bundle} as a function of metallic CNT (mCNT) density at two different technology nodes. Interconnect geometry is shown in Fig. 11(a).

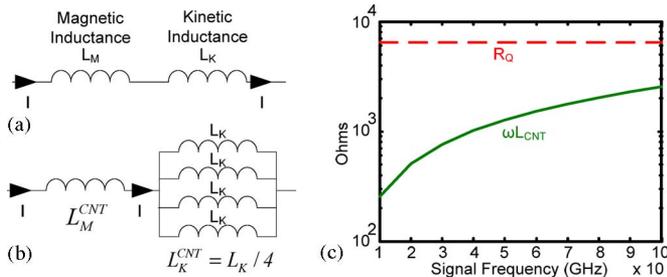


Fig. 15. Effective inductance model of (a) general 1-D conductor and (b) an isolated SWCNT with four parallel conducting channels. (c) Magnitude of inductive impedance (ΩL) of a $1\text{-}\mu\text{m}$ -long isolated ballistic SWCNT in comparison with intrinsic CNT resistance. As length increases beyond CNT mean free path, the kinetic inductance term (which dominates overall inductance) will become smaller and scattering resistance will become more significant. Hence, $R \gg \omega L$, always.

as $(1/2)L_K I^2$, where L_K is its *kinetic inductance* [47], [78]. The net change in energy due to current flow in the conductor is given by $\delta E = (1/2)L_K I^2 + (1/2)L_M I^2$. Hence, the effective inductance of a 1-D conductor is a series combination of L_M and L_K , as shown in Fig. 15(a).

For a 1-D conductor, assuming ballistic conduction, the kinetic inductance is given by [17], [78]

$$L_K (\text{p.u.l.}) = \frac{h}{2e^2 v_F}. \quad (12)$$

For lengths much larger than the mean free path, or at high bias voltages, scattering leads to a decrease in the kinetic energy and hence L_K is much smaller [17]. Since each CNT has four noninteracting parallel conducting channels, the effective kinetic inductance of a CNT is as follows:

$$L_K^{\text{CNT}} = \frac{L_K}{4} = 4\text{nH}/\mu\text{m}. \quad (13)$$

This theoretical value of kinetic inductance is in agreement with experimental observations in [79].

The magnetic inductance associated with an isolated SWCNT can be calculated from the magnetic field of a current-carrying wire, diameter “ d ,” lying a distance “ y ” away from a ground plane, as depicted in Fig. 10. Thus,

$$L_M^{\text{CNT}} (\text{p.u.l.}) = \frac{\mu}{2\pi} \cos h^{-1} \left(\frac{y}{d} \right). \quad (14)$$

For $d = 1\text{ nm}$ and $y = 1\text{ }\mu\text{m}$, L_M^{CNT} (per unit length) $\approx 1.5\text{ pH}/\mu\text{m}$. Clearly, kinetic inductance dominates the magnetic inductance for an SWCNT.

The equivalent inductance of a CNT is given by a series combination of its magnetic and kinetic inductances, as shown in Fig. 15(b). In familiar 3-D conductors with number of conducting modes $n \gg 1$, the kinetic inductance L_K/n becomes small compared to the magnetic inductance, hence its effect becomes less evident [47].

While considering the importance of CNT inductance, it must be noted that the high intrinsic resistance of a CNT ($6.45\text{ k}\Omega/\mu\text{m}$, considering perfect contacts) makes the inductive impedance appear small in comparison [Fig. 15(c)].

b) Inductance of an SWCNT Bundle Interconnect: In this paper, we have assumed noninteracting nanotubes since very little is known about the nature of the electromagnetic interactions in dense CNT bundles. Although SWCNTs in a bundle may not be isolated from each other, the consequences of this for the density of states, conductivity, and magnetically induced currents are not known yet. While the high-frequency properties of individual nanotubes as well as capacitive interactions between adjacent nanotubes in a flat array have been studied [76], [80], to the best of our knowledge, there is no experimental work or theoretical analysis yet about the nature of electromagnetic interactions between nanotubes or the penetration of electromagnetic waves inside a nanotube. Hence, the mutual inductance between SWCNTs in a bundle merits rigorous investigation before these effects can be included in the inductance model. The only work in the existing literature that attempts to calculate the mutual inductance between the nanotubes of a CNT bundle interconnect [48] assumes a nanotube as a solid metallic conductor with an equivalent conductivity. Since there is no physical justification for the validity of this approach, we refrain from using this model. In the following section, we show that CNT bundle inductance does not have a significant impact on the performance of CNT-based interconnects. Hence, neglecting the mutual inductance between CNTs in a bundle will not have a large impact on the performance analysis shown here.

Under the assumption that the nanotubes of a bundle are magnetically isolated (no mutual inductance effects), the effective inductance can be treated as the parallel combination of the inductance corresponding to each SWCNT. The inductance of the CNT bundle interconnect is then given by

$$L_{\text{bundle}} (\text{p.u.l.}) = \frac{L_K^{\text{CNT}} (\text{p.u.l.}) + L_M^{\text{CNT}} (\text{p.u.l.})}{n_{\text{CNT}}}. \quad (15)$$

The scaling of bundle inductance with number of CNTs is also supported by experimental observations [79].

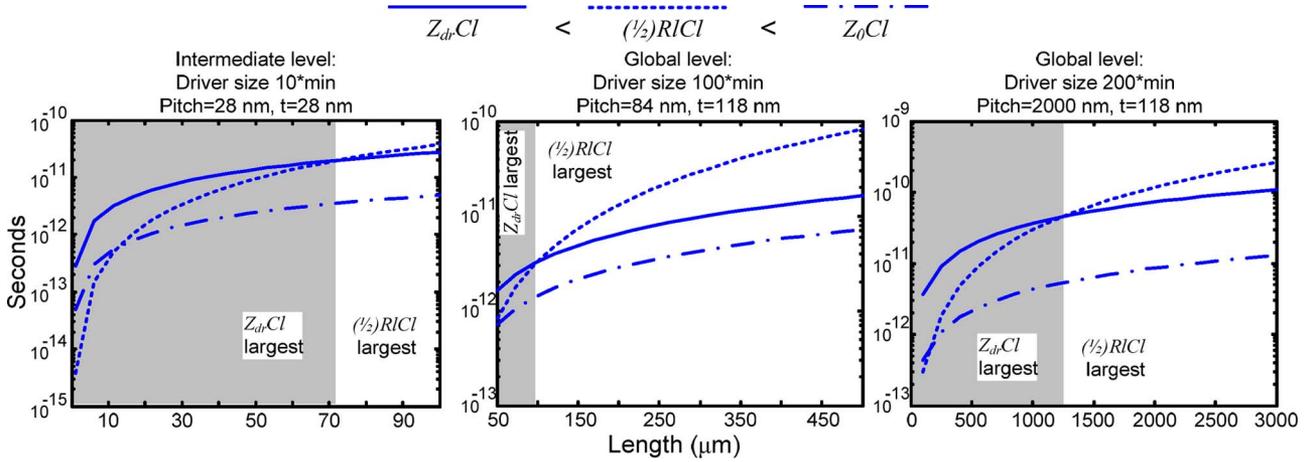


Fig. 16. Comparison of measures of propagation delay: $Z_{dr}Cl$, $(\frac{1}{2})RlCl$, and Z_0Cl , as a function of interconnect length for (a) intermediate, (b) minimum-width global and (c) maximum-width global SWCNT bundle interconnects, at 14 nm technology node. Wire width = $\frac{1}{2}$ pitch; wire thickness (t) is shown. $\lambda_{CNT} = 1\mu\text{m}$, $T = 300\text{ K}$.

C. Importance of SWCNT Bundle Inductance for Interconnect Delay

The importance of considering CNT bundle inductance in interconnect delay models can be analyzed following the methodology in [81], which presents a detailed analysis of resistance–inductance–capacitance (R – L – C) representation of interconnects. An R – C -only model for interconnect delay becomes inaccurate (and inclusion of inductance in the delay model becomes necessary) when

$$Z_{dr}Cl < \frac{1}{2}RlCl < Z_0Cl. \quad (16)$$

Here, Z_{dr} is the driver impedance; R , C , and L are the per unit length interconnect resistance, capacitance, and inductance, respectively; l is the interconnect length; and $Z_0 = \sqrt{L/C}$ is its characteristic impedance. The first inequality in (16) suggests that the gate (driver) delay should be less than the interconnect delay (approximated by $(1/2)RlCl$) as well as wave propagation delay (Z_0Cl). The second inequality suggests low resistive losses ($Rl < 2Z_0$) to ensure low-loss transmission line behavior. If these conditions are satisfied, the interconnect will behave as a transmission line, with delay determined by the wave propagation speed $1/\sqrt{LC}$, and its inductance will be important for accurate delay estimation.

Fig. 16 plots the three terms in (16) for different CNT bundle interconnect geometries. It is observed that for all different interconnect lengths and dimensions, as well as driver sizes (chosen based on intermediate or global interconnect levels), either the driver impedance (Z_{dr}) or the line impedance (Rl) dominates. This remains true for minimum-width wires as well as for the widest global interconnects. Since the inequality (16) is never satisfied, it is reasonable to assume that simple RC circuits (ignoring line inductance) will suffice to model CNT bundle interconnect delay.

It must be noted that the mutual inductance between nanotubes within a CNT bundle has not been taken into account here. However, we overestimate the magnetic inductance of each

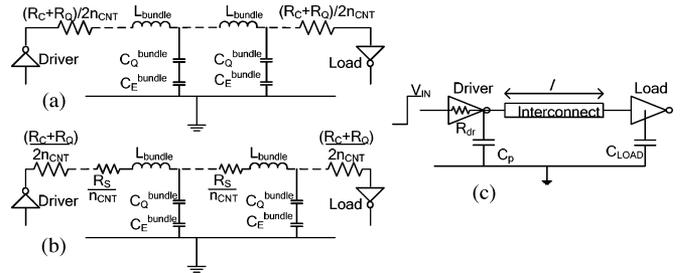


Fig. 17. Equivalent circuit diagram for a CNT bundle interconnect for (a) length less than the CNT mean free path (no scattering resistance) and (b) length greater than the CNT mean free path. (c) Equivalent circuit representation for driver and load at the ends of the interconnect.

CNT (by considering the substrate as the nearest current-return path) as well as kinetic inductance. Hence, a more accurate calculation of CNT bundle inductance will not alter the conclusions shown here.

D. Equivalent Circuit Model for SWCNT Bundle Interconnect Delay

The equivalent circuit model for an SWCNT bundle interconnect is shown in Fig. 17. The driver is represented by its equivalent resistance R_{dr} , input capacitance C_{Input} , and output parasitic capacitance C_p , while C_{LOAD} represents the input capacitance of the driven gate. Two types of interconnects are analyzed here: 1) local interconnects with driver size one to five times the minimum-sized inverter and a load fan-out of four identical gates and 2) global interconnects where the interconnect is part of a long buffered interconnect, with identical (large) inverters at driver and load ends. As shown in the previous subsection, CNT bundle inductance has little impact on the interconnect delay, hence a distributed RC model is used to represent the interconnect.

As an illustration, the commonly used Elmore delay [82] expression for a Cu interconnect is given by

$$t_{50\%}^{\text{Cu}} = 0.69R_{\text{dr}}(C_{\text{LOAD}} + C_p) + 0.69R_{\text{dr}}Cl + 0.38RCl^2 + 0.69RlC_{\text{LOAD}}. \quad (17)$$

where R and C are the interconnect resistance and capacitance per unit length, respectively, and l is the interconnect length. For local interconnects, the drivers and load are nearly minimum-sized gates, hence driver resistance R_{dr} is large, while load capacitance C_{LOAD} is small. On the other hand, the buffers/repeaters needed to send signals across large distances are sized up significantly (often more than 100 times minimum-sized gates). Hence, for global interconnects, R_{dr} is small while C_{LOAD} is large. Similar Elmore delay expressions can be obtained for the CNT bundle interconnect, e.g., the delay expression for the equivalent circuit shown in Fig. 17(b) is as follows:

$$\begin{aligned} t_{50\%}^{\text{CNT}} &= 0.69R_{\text{dr}}(C_{\text{LOAD}} + C_p) \\ &+ 0.69\left(R_{\text{dr}} + \frac{R_C + R_Q}{2n_{\text{CNT}}}\right)\left(\frac{C_Q^{\text{bundle}}C_E^{\text{bundle}}}{C_Q^{\text{bundle}} + C_E^{\text{bundle}}}\right)l \\ &+ 0.38\frac{R_S}{n_{\text{CNT}}}\left(\frac{C_Q^{\text{bundle}}C_E^{\text{bundle}}}{C_Q^{\text{bundle}} + C_E^{\text{bundle}}}\right)l^2 \\ &+ 0.69\left(\frac{R_S}{n_{\text{CNT}}}l + \frac{R_C + R_Q}{n_{\text{CNT}}}\right)C_{\text{LOAD}}. \end{aligned} \quad (18)$$

IV. INTERCONNECT PERFORMANCE ANALYSIS WITH SWCNT BUNDLES

A. Local Interconnects

Local interconnect lengths are typically a few hundred nanometers and no more than a few microns. Hence, for this analysis, it is assumed that local interconnect lengths are less than the mean free path, λ_{CNT} . Fig. 18 shows the propagation delay of short local interconnects that are driven by minimum-sized drivers. As explained in Section III-B2, since full 3-D capacitance simulations are used to accurately compute the SWCNT bundle electrostatic capacitance, the delay at 22 and 18 nm nodes is calculated only for sparse bundles (mCNT density <100%) with fewer SWCNTs. It is found that the propagation delay of short local CNT interconnects is nearly the same as that of Cu wires (delay ratio $t_{\text{CNT}}/t_{\text{Cu}} \approx 1$) over a wide range of mCNT densities and for all technology nodes considered. This is despite the fact that sparse bundles have higher resistance than Cu wires, since the driver resistance ($\sim k\Omega$) is much larger than the resistance of short local interconnects. In fact, as shown in Fig. 18(d), even with imperfect contacts ($R_C = 10 k\Omega$) that increase the CNT bundle resistance further, delay remains competitive with that of Cu wires.

As noted before, due to lack of control on chirality, it is difficult to achieve high density of metallic SWCNTs in a bundle. It is shown here that even with the low densities that may be readily achievable ($\sim 40\%$ mCNTs are routinely fabricated), SWCNT bundles can compete with the performance of Cu for short local interconnects.

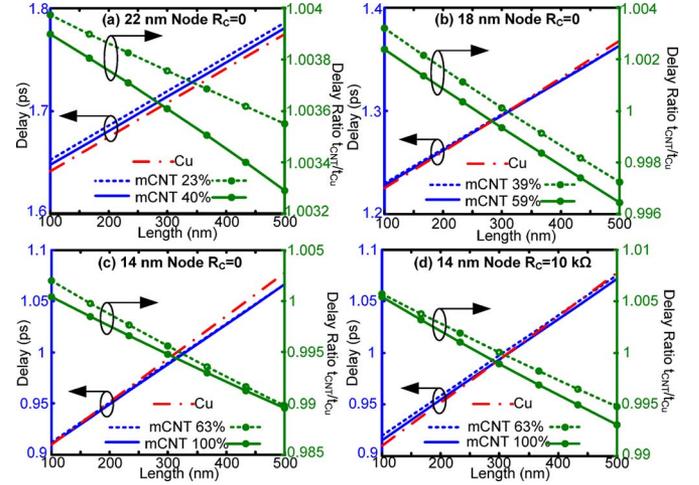


Fig. 18. Local interconnect delay (50% delay) with CNT bundles at (a) 22 nm, (b) 18 nm, (c) 14 nm technology nodes, assuming perfect metal nanotube contacts ($R_C = 0$), and (d) 14 nm node with $R_C = 10 k\Omega$. Left-hand y -axes: value of delay; right-hand y -axes: ratio of delay with CNT to that with Cu. Percentage values in legends show metallic CNT (mCNT) density, as a% of the maximum density possible. Capacitance values have been calculated using 3-D electromagnetic simulations. $\lambda_{\text{CNT}} = 1 \mu\text{m}$.

TABLE I
DRIVER RESISTANCE FOR DIFFERENT DRIVER SIZES AND INTERCONNECT RESISTANCE FOR DIFFERENT LENGTH INTERCONNECTS WITH CU AND CNT MONOLAYERS AT 22 nm NODE

R_{dr} (Ohms) (driver size)	16810 (minimum size)		1681 (10*minimum size)		
Length (μm)	2	8	12	16	20
Cu Resistance (Ohms)	124.2	496.8	745.2	993.6	1242
CNT monolayer Resistance (Ohms) 10 mCNTs, $\lambda_{\text{CNT}} = 1 \mu\text{m}$	1290	5160	7740	10320	12900

Driver resistance is calculated from ITRS. Cu resistance takes into account the increasing resistivity due to size effects.

In the case of very short interconnects ($< 1 \mu\text{m}$ length), where R_{dr} is much greater than interconnect resistance, it is beneficial to make the SWCNT bundles sparse, which reduces interconnect capacitance (see Fig. 13). CNT monolayer interconnects proposed in [45], which consist of a single flat array of SWCNTs [Fig. 3(b)], are an extreme example of this effect. The resistance of a monolayer is high because it can accommodate only a small number of SWCNTs, but its capacitance is nearly half that of a Cu wire of equal width. It has been previously reported that CNT monolayers are suitable for local interconnects up to $20 \mu\text{m}$ lengths [43]. We show here that the realistic range of lengths where CNT monolayers may be useful is significantly smaller and depends on the driver size.

1) *CNT Monolayer Interconnects*: Table I shows the driver resistance for two different driver sizes and interconnect resistances considering Cu as well as SWCNT monolayer interconnects at the 22 nm node. In this case, $R_C = 0$, assuming high-quality embedded contacts as done in [43]. It is important to note that ensuring embedded contacts (shown schematically in Fig. 6) for each SWCNT makes it difficult to pack SWCNTs with maximum density since the embedded contact material will occupy some inter-CNT space. We have optimistically assumed that ten metallic SWCNTs (diameter 1 nm each) can be

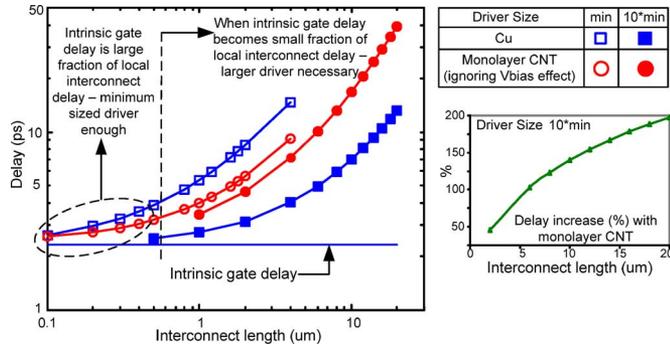


Fig. 19. Local interconnect delay (including driver and load) with CNT monolayers and Cu wires at 22 nm node, as a function of interconnect length, with minimum-sized drivers (hollow symbols) and drivers of size = 10^* minimum (solid symbols). Dotted lines identify roughly the regions where minimum-sized drivers and larger (size = 10^* minimum) drivers should be used. Percent increase in delay with CNT monolayers for driver size = 10^* minimum and interconnect lengths 2–20 μm is shown alongside.

accommodated in a 22-nm-wide monolayer interconnect. It is evident from Table I that few-micrometer-long Cu interconnects have a small resistance compared to the driver. However, this is not true for CNT monolayer interconnects *unless* the driver is minimum-sized.

Fig. 19 shows a comparison between Cu and CNT monolayer local interconnect delays for two different driver sizes (with a fan-out of four identical gates). For minimum-sized drivers (hollow symbols), CNT monolayers have lower delay than Cu because of the significantly lower capacitance. However, minimum-sized drivers can be used only when interconnect delay is dominated by the intrinsic gate delay. It is observed that at about 1 μm length, the local interconnect delay becomes much larger than intrinsic gate delay. Beyond this length, it is necessary to use larger drivers. There is a clear reduction in delay with driver size ten times the minimum (solid symbols). However, in this case, the large resistance of CNT monolayers increases delay by 100%–200% as compared to Cu, in spite of the $2\times$ lower capacitance.

Hence, CNT monolayers can provide only some delay advantage over Cu interconnects for very short, a few hundred nanometers long, local interconnects that are driven by minimum-sized drivers. For this small subset of interconnects, delay is dominated by the intrinsic gate delay. The advantage for CNT monolayers is the reduced power dissipation resulting from $2\times$ lower capacitance [42], [43], [45]. However, it must also be noted that the resistive power dissipation along these interconnects will be higher than that across Cu interconnects.

B. Global Interconnects

Fig. 20 shows that dense SWCNT bundle interconnects can easily outperform Cu at the global level (ratio of delay $t_{\text{CNT}}/t_{\text{Cu}} < 1$). The improvement in global interconnect performance with CNT bundles arises mainly from the large mean free path of electrons, which results in much lower interconnect resistance [see Fig. 8(b) and (c)]. In the case of minimum-width global interconnects, dense CNT bundles can reduce the delay by more than 55% for a 500- μm -long interconnect. In the case

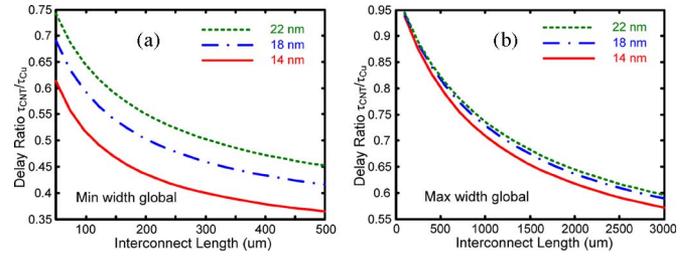


Fig. 20. Ratio of global interconnect delay with maximum-density CNT bundles to that with Cu wires, as a function of length, at different technology nodes for (a) minimum-width and (b) maximum-width global wires ($w \sim 1 \mu\text{m}$). Interconnect dimensions as per ITRS. Driver size = 100^* minimum. CNT bundle capacitance assumed equal to Cu wire capacitance.

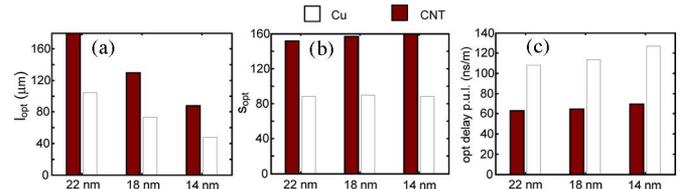


Fig. 21. Results of optimizing delay per unit length for minimum-width global interconnect [14] inserted with repeaters of optimal size “ s_{opt} ” separated by optimal distance “ l_{opt} ” showing values of (a) l_{opt} , (b) s_{opt} , and (c) optimal delay per unit length, for maximum-density CNT bundles and Cu.

of maximum-width global interconnects whose width is $\sim 1 \mu\text{m}$ at all technology nodes, dense SWCNT bundle interconnects can reduce global interconnect delay by 30% for a 1-mm-long and 40% for a 3-mm-long interconnect. The larger improvement in case of minimum-width wires is because of higher Cu resistance for these dimensions. The benefit of using SWCNT global interconnects increases with scaling and with the interconnect length. As mentioned in Section III-B2, SWCNT bundle electrostatic capacitance at the global level is assumed to be equal to Cu wire capacitance as it provides a close upper bound to the CNT bundle capacitance.

Global interconnects are often designed by inserting buffers (repeaters) at regular intervals to minimize delay per unit length (τ/l) [82]. Fig. 21 shows the optimal buffer insertion parameters: 1) l_{opt} , the optimal distance between repeaters and 2) s_{opt} , the optimal size of repeaters as a multiple of a minimum-sized inverter. Fig. 21(c) shows that the optimal delay per unit length $(\tau/l)_{\text{opt}}$, with buffered SWCNT bundles as minimum-width global interconnects, is significantly lower than that with Cu. While technology scaling alone shows a small increase in minimum-width Cu global interconnect delay, the move from Cu to CNT-based interconnect reduces delay by nearly $2\times$.

Fig. 22 shows the power dissipation of a 1-mm-long buffered global interconnect as a multiple of the power dissipation of a minimum-sized inverter (the ratio of the total width of buffers driving the interconnect to the width of a minimum-sized inverter, which is shown in the figure, is commensurate to the ratio of their power dissipations). It is found that the power dissipation of a minimum-width optimally buffered global interconnect is the same with SWCNT bundle as that with Cu at all technology nodes [Fig. 22(a)]. Note that in this optimal-delay case, SWCNT interconnects have nearly $2\times$ lower delay

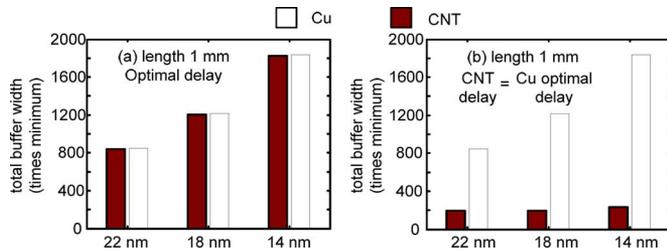


Fig. 22. Total buffer width on a 1-mm-long minimum-width global interconnect: “number of buffers” multiplied by “size of each buffer” (a) to achieve optimal delay with both Cu and CNT bundle interconnects, respectively, and (b) to achieve delay equal to Cu optimal delay with both CNT bundles and Cu. Total buffer width gives a measure of the repeater power dissipation (as a multiple of the power dissipation for a minimum-sized inverter).

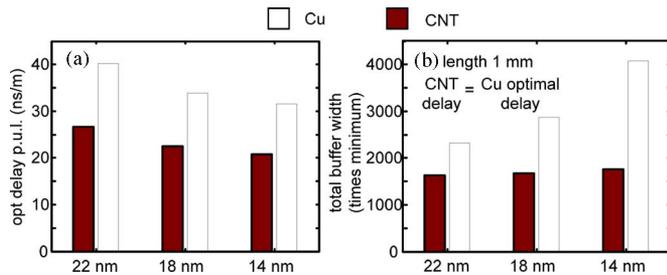


Fig. 23. (a) Optimal delay per unit length for a maximum-width global interconnect (width $\sim 1 \mu\text{m}$) inserted with repeaters, for maximum-density CNT bundles and Cu. (b) Total buffer width on a 1-mm-long interconnect to achieve delay equal to Cu optimal delay, for maximum-density CNT bundles and Cu.

than Cu. Fig. 22(b) shows the power dissipation when the delay with SWCNT bundles is suboptimal but equal to the optimal delay with buffered Cu interconnects. In this case, the power dissipation with SWCNT bundle is $4\times$ lower at the 22 nm node and nearly $8\times$ lower at the 14 nm node. This result will have significant implications for future technology generations where power dissipation (active as well as leakage) is a critical concern.

In order to reduce delay, timing-critical global wires are conventionally kept wide ($\sim 1 \mu\text{m}$) and not scaled aggressively [14]. Fig. 23(a) shows that for such large wire widths, the optimal delay is much lower than that for minimum-width wires [shown in Fig. 21(c)], while the delay with SWCNT bundles is again significantly lower than that with Cu. However, Fig. 23(b) shows that the reduction in delay by using wide wires comes with an increase in power dissipation [in comparison with Fig. 22(a)]. Fig. 23(b) also shows that for $1\text{-}\mu\text{m}$ -wide global interconnects, SWCNT bundles can achieve the same delay as optimally buffered Cu interconnect with significantly lower power dissipation. Hence, SWCNT bundles can be used to improve the performance as well as to reduce the power consumption of global level VLSI interconnects.

V. INTERCONNECT RELIABILITY ANALYSIS WITH SWCNT BUNDLES

Due to strong sp^2 bonding (like graphite), CNTs are much less susceptible to electromigration (EM) problems than Cu interconnects. Metallic SWCNT bundles can carry current densities of the order of 10^9 A/cm^2 [23]. The maximum current density in Cu interconnects, on the other hand, is limited to

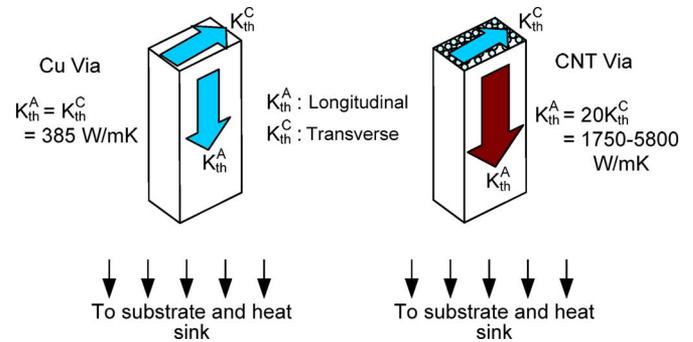


Fig. 24. Schematic showing heat conduction paths and thermal conductivity values in Cu and CNT bundle vias. CNT bundle thermal conductivity is anisotropic: in the longitudinal direction $K_{th}^A > 1750 \text{ W/mK}$ [85]; in the transverse direction, K_{th}^C is about 20 times lower [86].

$\sim 10^6 \text{ A/cm}^2$ due to EM [83]. A Cu interconnect with $100 \text{ nm} \times 50 \text{ nm}$ cross section can carry current up to $50 \mu\text{A}$, whereas a 1-nm-diameter CNT can carry up to $20\text{--}25 \mu\text{A}$ [57]. Hence, from a reliability perspective, a few CNTs are enough to match the current-carrying capacity of a typical Cu interconnect. It is only the need to reduce CNT interconnect resistance (and make its delay competitive with Cu) that necessitates bundles of a large number of CNTs. Fabrication efforts for CNT-based interconnects have thus far focused on vias, or vertical interconnects, which are most prone to failure because of their small dimensions [8], [19]–[22]. Here, we point to another property of CNTs that makes them attractive candidates for future vias.

At nanometer dimensions, interconnect metal layers in the back end see very significant temperature rise above the chip’s junction temperature as a combined result of increasing Cu interconnect resistivity and higher current density (J) demands [15]. This adversely affects interconnect reliability, since EM lifetime of Cu depends quadratically on J and exponentially on metal temperature (T_m) [83]. The primary mode of heat removal from the interconnect stack (10–14 metal layers) is by conduction toward the heat sink attached to the chip substrate [15]. Due to low thermal conductivity (K_{th}) of interlayer dielectric (ILD) ($K_{th,ILD} < 0.4 \text{ W/mK}$, and decreases further with technology), the Cu vias (with $K_{th,Cu} = 385 \text{ W/mK}$) between successive metal layers form the primary heat conduits.

Molecular dynamics simulations of CNTs predict that $K_{th} \sim 6600 \text{ W/mK}$ [5], an order of magnitude higher than that of Cu. The thermal conductivity of individual MWCNTs, found experimentally, exceeds 3000 W/mK [84]. The thermal conductivity of CNT bundles, however, can be much lower due to the presence of numerous highly resistive thermal junctions between adjacent nanotubes [84]. Based on measurements, K_{th} for an SWCNT bundle is predicted in the range $1750\text{--}5800 \text{ W/mK}$ [85] (along the CNT length) at room temperature. Hence, vias composed of CNT bundles can serve as much more effective heat conduits than Cu vias and reduce the temperature gradient in the back-end.

For SWCNT bundles, the high value of K_{th}^A is only in the longitudinal direction (see Fig. 24). In the transverse direction, K_{th}^C is about 20 times lower [86]. The K_{th}^A of $1\text{-}\mu\text{m}$ -long CNT bundles was measured in [85]. Few experimental data and thermal models are available for $l < 1 \mu\text{m}$, which will be the desired

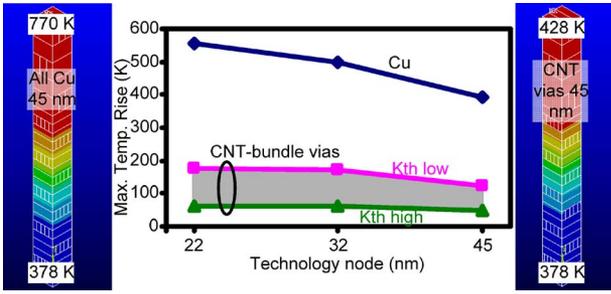


Fig. 25. Maximum temperature rise (ΔT) on interconnects using CNT bundle vias and Cu vias at different technology nodes, as obtained from 3-D finite-element electrothermal simulations. Reference (junction) temperature = 378 K. For CNT bundle, $K_{th_low} = 1750$ W/mK and $K_{th_high} = 5800$ W/mK.

height of vias in most nanoelectronic circuits. The work in [70] suggests temperature and length-dependent models for K_{th} of isolated metallic SWCNTs, but the same models may not be applicable to CNT bundles.

The results shown here are based on the assumption that the high thermal conductivities mentioned above can be achieved with CNT bundle vias, although the presence of large thermal contact resistance between CNT bundles and surrounding materials make it challenging. It is also assumed that the CNT bundles have high density and low electrical contact resistance, so as to have resistance similar to Cu vias (this requirement is further examined in the following subsection). For low via resistance values, self-heating in individual vias has a small impact on the overall temperature of the interconnect stack [15]. It has been shown in [32] that CNT vias are both electrically and thermally ballistic and heating is primarily due to the contacts. Note that we do not consider severe Joule heating effects at high bias [87] as the voltage bias across interconnects is very low. The impact of thermal contact resistance to SWCNTs [32], [88] has not been considered in this analysis. Hence, the vias are treated essentially as heat conduits raising the effective thermal conductivity between successive metal layers.

A. Hybrid CNT–Cu Interconnects

Full 3-D electrothermal simulations are performed on a complete 10–14 metal layer interconnect stack at different technology nodes, considering CNT-based vias forming vertical interconnections between Cu metal layers. This configuration is termed hybrid CNT–Cu interconnects. Fig. 25 shows that with these hybrid interconnects, the maximum temperature rise on the interconnect stack can be almost ten times smaller than that with traditional Cu interconnects.

Fig. 26(a) compares the resistance of local vias composed of CNT bundles to those made of Cu as a function of mCNT density at the 22 nm node. It is found that the resistance of CNT bundle vias can be five to ten times that of Cu vias even for very-high-density metallic-CNT bundles. Large imperfect metal–nanotube contact resistance (R_C) will have an adverse effect on the resistance of these vias. Hence, it is very important to achieve near-perfect contacts to keep CNT bundle via resistance low. Fig. 26(b) shows the delay penalty incurred by

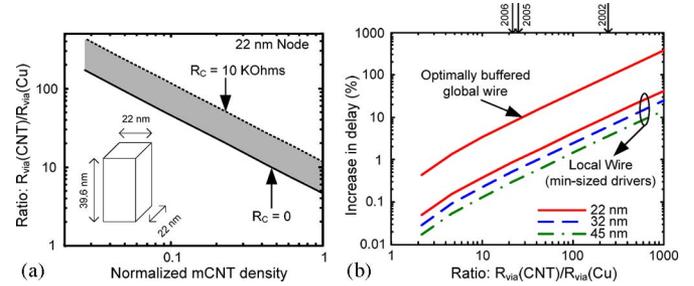


Fig. 26. (a) Ratio of CNT bundle via resistance to Cu via resistance as a function of metallic CNT (mCNT) density in bundle, at 22 nm node. Shaded region: imperfect metal–nanotube contact resistance $0 < R_C < 10$ k Ω . (b) Percent increase in delay for arbitrary increase in CNT via resistance (as a multiple of Cu via resistance) for different technology nodes, at local and global interconnect levels. Arrows along top border show the CNT via resistances (as a multiple of Cu via resistance) that have already been achieved [8], [20], [21].

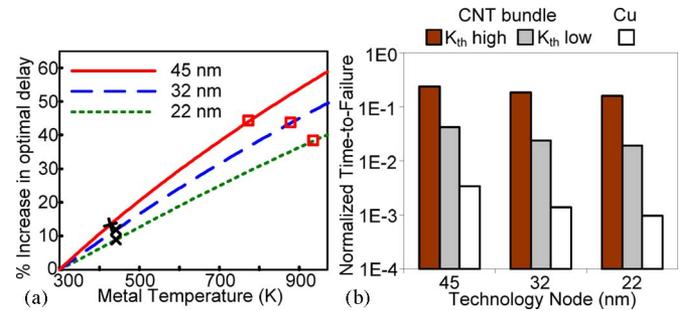


Fig. 27. (a) Increase in delay p.u.l. (τ/l) for Cu global interconnects calculated at different metal temperatures as a % of optimal τ/l at room temperature. Symbols show actual maximum interconnect temperature when the vias are made of Cu (squares) or CNTs with K_{th_low} (crosses). (b) Mean Time to Failure for Cu interconnects at maximum on-chip interconnect temperature, normalized to that at reference temperature (105 °C), with Cu vias and CNT bundle vias.

using vias with high resistance. For very short local interconnects with minimum-sized drivers, the delay penalty is less than 1% if the via resistance is less than 20 times Cu via resistance. As indicated in the figure, resistance in this range has already been achieved for MWCNT vias [8], [20], [21]. However, at the global level (where driver resistances are significantly smaller), resistance must be within four times that of Cu vias in order to limit delay penalty within 1%. This analysis assumes that SWCNT-based vias are used between all metal layers, and does not use multiple parallel vias to reduce the resistance.

B. Impact on Cu Interconnect Performance and Reliability

Fig. 27 shows the performance and reliability impact of using hybrid CNT–Cu interconnects. Since Cu resistivity increases with temperature, delay per unit length (τ/l) for Cu global interconnects at maximum temperature is about 40% higher than optimal τ/l calculated at room temperature if Cu vias are used. This number is only about 10% higher if CNT bundle vias are used [Fig. 27(a)]. Fig. 27(b) shows that the lower interconnect temperatures with CNT bundle vias can lead to two orders of magnitude improvement (for $K_{th} = 5800$ W/mK) in the EM

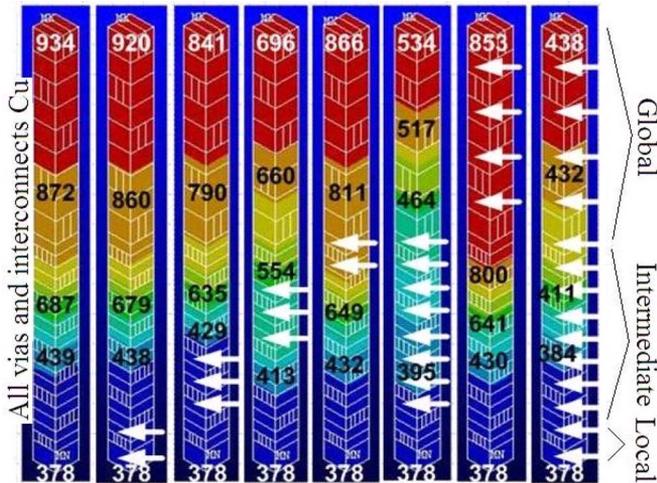


Fig. 28. Interconnect temperature (K) at different layers from 3-D finite-element electrothermal simulations (22 nm node). Leftmost: all interconnects and vias are Cu; rightmost: all vias are CNT bundles. White arrows point to the interconnect layers where the vias are composed of CNT bundles. All other vias and all metal layers are Cu.

mean-time-to-failure of Cu global interconnects and one order of magnitude improvement with $K_{th} = 1750$ W/mK.

Fig. 28 summarizes a thermal management strategy based on the use of CNT bundles to replace Cu at different locations in the interconnect stack. Full 3-D finite-element electrothermal simulation results are shown for the back-end thermal profile employing hybrid CNT–Cu interconnects. The variation in this profile and the maximum interconnect temperature is shown as the location of CNT bundles is changed from local to intermediate to global level vias. It is found that CNT bundle vias at the intermediate level yield the largest benefit in reducing the interconnect temperatures with least disruption in the Cu interconnect stack. This is because the intermediate level has the maximum number of metal layers, leading to the largest reduction in overall thermal resistance between the global metal layers and the heat sink. Thus, vias composed of CNT bundles can very effectively be used as *thermal vias* to reduce interconnect temperatures at advanced technology nodes, as well as in 3-D ICs where thermal management is a critical concern [89], [90].

VI. CONCLUSION

In conclusion, a comprehensive and realistic evaluation of SWCNT bundle interconnects has shown significant advantages over Cu in terms of performance, power dissipation, as well as thermal management/reliability. The equivalent circuit parameters needed for analyzing SWCNT interconnect delay have been studied in detail, highlighting the underlying assumptions. The correct length-dependent behavior of the voltage bias-dependent SWCNT interconnect resistance and the factors influencing CNT interconnect contact resistance have been presented. The first full 3-D capacitance simulations for SWCNT bundles of realistic VLSI interconnect dimensions, and a quantitative analysis of the importance of CNT interconnect inductance in computing interconnect delay, are shown. In light of

Table II
SUMMARY OF THE PERFORMANCE AND RELIABILITY OF CNT BUNDLES AS COMPARED WITH CU IN THE DIFFERENT DOMAINS OF ON-CHIP INTERCONNECTS ALONG WITH THEIR PROCESS REQUIREMENTS

	Local	Intermediate	Global	Via/Contact
Performance	Same as Cu	~ 50% lower delay	30-40% lower delay	< 1% delay penalty
Reliability	Exceeds Cu	Exceeds Cu	Exceeds Cu	Exceeds Cu
Process Requirements	Dense bundle; Low contact resistance	Dense bundle	Dense bundle	Dense bundle; Low contact resistance

the significant progress in state-of-the-art on-chip integration of CNT vias (vertical interconnects), this study provides a unique insight into the advantages and limitations of SWCNT bundle vias. The most important conclusions from this study are summarized below.

It is found that SWCNT bundles can provide a 4× reduction (at 22 nm node) in power dissipation of long global interconnects while offering the same performance as optimally buffered Cu interconnects. This power saving increases with technology scaling to 8× at the 14 nm node. This is a promising result as the rising power dissipation in aggressively buffered Cu global interconnects threatens to become a tremendous challenge for future technology generations. On the other hand, for performance-critical applications, SWCNT interconnects offer 30%–40% improvement in the delay of millimeter-long global interconnects as compared to Cu. The factor limiting SWCNT bundle performance in this domain is the density of mCNTs, not imperfect contact resistances. In the case of short local interconnects that have lengths less than the mean free path of electrons in a nanotube, SWCNT bundle performance again exceeds that of Cu. In this domain, the limiting factors are mCNT density as well as imperfect metal–nanotube contact resistance. In the case of vias, reliability is a far greater concern than performance. Hence, even with little or no improvement in signal propagation delay, SWCNT bundles can provide a valuable alternative to Cu due to better reliability. Most importantly, it is shown that SWCNT bundle vias can greatly reduce interconnect temperature rise and, thus, when integrated with Cu metal layers, improve Cu interconnect performance (about 30%) and lifetime (by orders of magnitude). The advantage of SWCNT bundle vias in controlling the back-end temperature, as shown in this paper, will also have significant implications for emerging technologies such as 3-D ICs where thermal management is a primary concern.

All these advantages, and the corresponding requirements from a process technology perspective that will be needed to make SWCNT bundles a viable interconnect material, are summarized in Table II.

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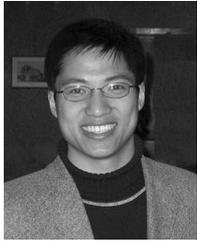
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