

Small Optical Sources with Improved Speed/Power Dissipation

HP Photonic Interconnect Forum

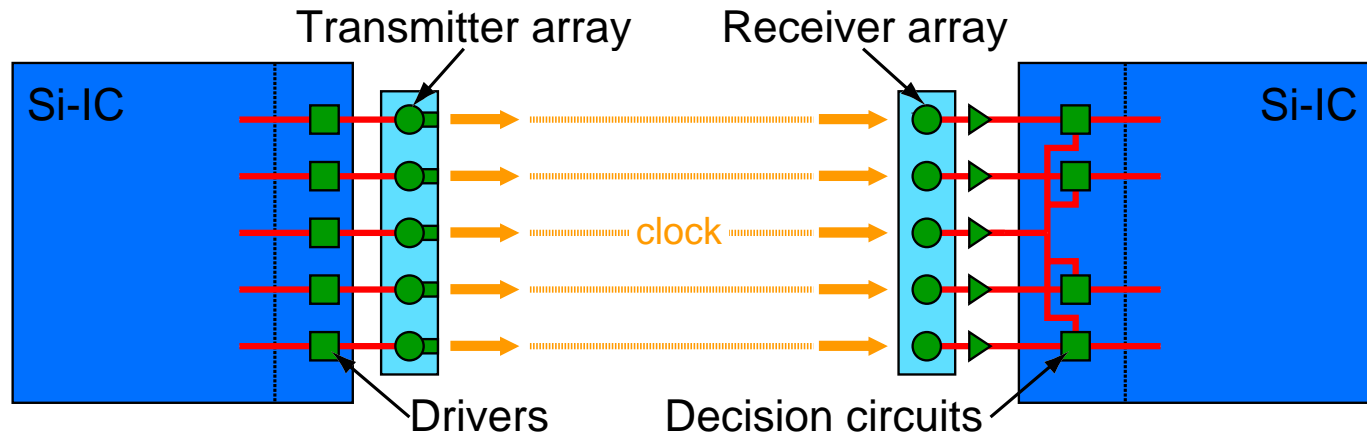
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- **Introduction**
 - Photonic Interconnect
 - State-of-the-Art High-Speed VCSELs
- **Device Structure**
 - Tapered oxide aperture
 - Deep oxidation layers
 - Optimized p -DBR mirror
- **Device Performance**
 - Static performance
 - RF performance
- **Potential Improvement**
 - Lateral carrier confinement
- **Conclusion**

- **Interconnect is becoming the bottleneck for continuous scaling microprocessor's performance**
- **Photonics is a viable alternative to current copper-based electrical interconnect**
 - Lower signal delay
 - Higher bandwidth
 - Consume less power
 - Resistant to electromagnetic interference (EMI)
- **VCSELs are attractive for photonic interconnect**
 - Small footprint
 - Ease of fabrication in arrays
 - On-wafer testing
 - High-speed operation at lower power dissipation



Challenges for the transmitters in photonic interconnect

- Thermal restriction ⇒ Low power dissipation
- Bandwidth demand ⇒ High data rates (20+ Gb/s)
- Compatibility with Si-IC ⇒ Driver integrability
- Cost effectiveness ⇒ Mass manufacturability with good yield

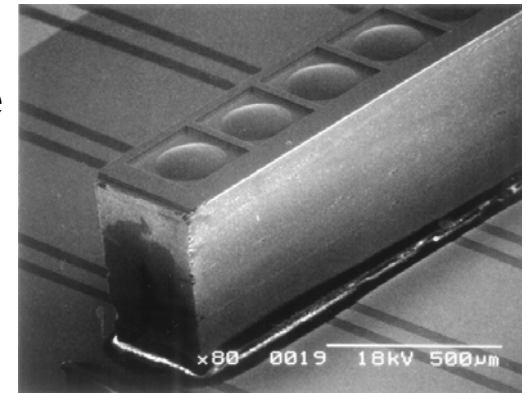
State-of-the-Art High-Speed VCSELs

Wavelength	Authors	Features	Achievements
850 nm	K.L. Lear <i>et al.</i> ¹	<ul style="list-style-type: none"> • Proton Implantation • <i>P</i>-substrate (<i>n</i>-side up) 	<ul style="list-style-type: none"> • 21.5 GHz bandwidth • MCEF=14.2 GHz/mA^{1/2}
980 nm	Y.-C. Chang <i>et al.</i> ²	<ul style="list-style-type: none"> • Improved oxide aperture • Deep oxidation layers • Optimized <i>p</i>-mirror 	<ul style="list-style-type: none"> • >20 GHz bandwidth • MCEF=16.7 GHz/mA^{1/2} • 35 Gb/s operation
1.1 μm	T. Anan <i>et al.</i> ³	<ul style="list-style-type: none"> • Buried type II tunnel junction • Proton Implantation 	<ul style="list-style-type: none"> • 24 GHz Bandwidth • 40 Gb/s operation

1. K. L. Lear *et al.*, *Proc. Conf. on Lasers and Electro-Optics*, paper no. WA1, 1997.
2. Y.-C. Chang *et al.*, *Electron. Lett.*, vol. 43, pp. 1022–1023, 2007.
3. T. Anan *et al.*, *Proc. Optical Fiber Communication Conf.*, paper no. OThS5, 2008.

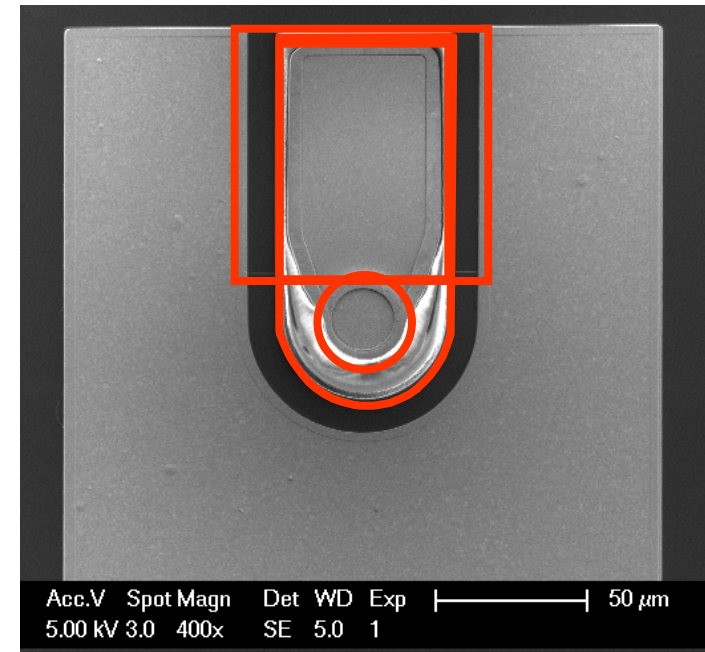
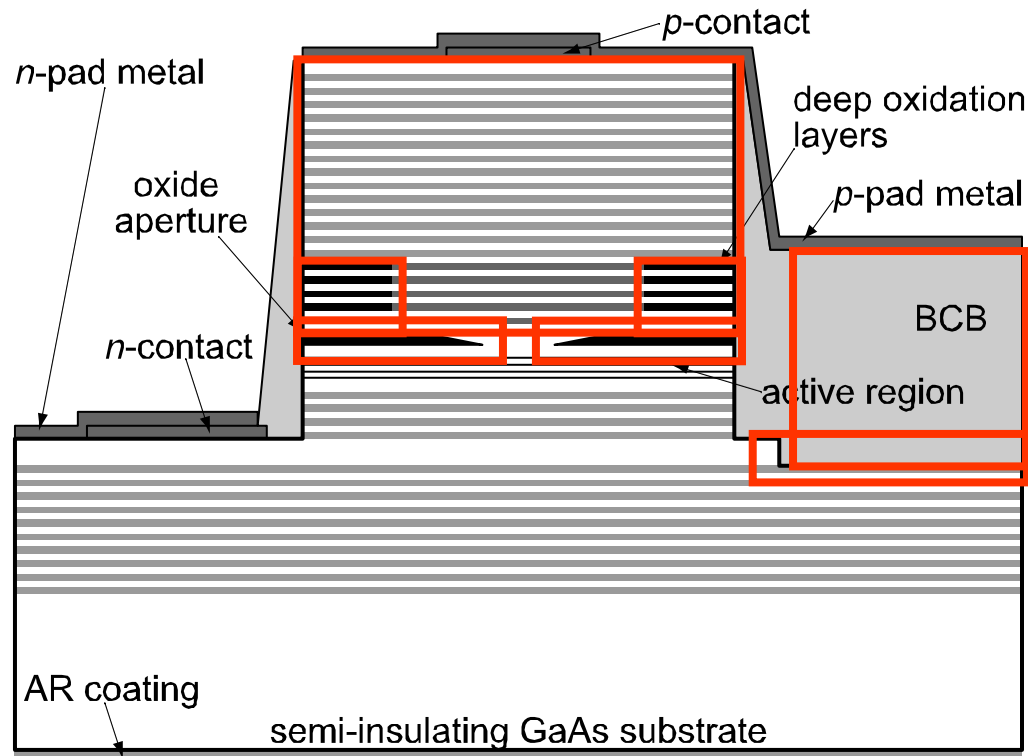
N-intracavity, bottom-emitting, tapered-oxide-aperture VCSELS emitting at 980 nm wavelength

- N-intracavity contact scheme \Rightarrow semi-insulating substrate
 - Direct driver integration using flip-chip bonding
 - No parasitics associated with conducting substrate and wire bonding
- Bottom-emission \Rightarrow Backside microlenses
 - Collimated output beams for better alignment tolerance
 - Reduce package costs
- Oxide aperture \Rightarrow carrier and photon confinement
 - Increased modal gain
 - Reduce sidewall losses
- 980 nm wavelength emission \Rightarrow strained InGaAs QWs
 - Lower transparency and higher differential gain
 - Better reliability
 - Transparency for GaAs substrate



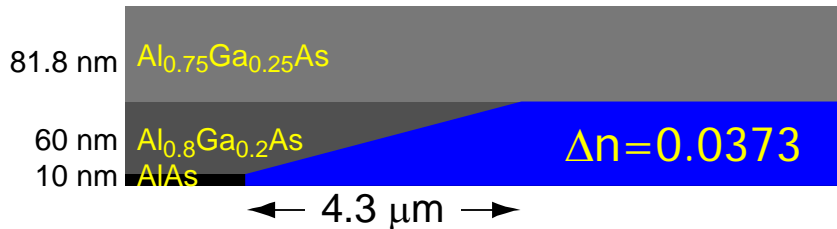
Some key features of our devices:

- Improved tapered oxide aperture
- Deep oxidation layers
- Optimized p -mirror
- Low k dielectric BCB
- N -contact layer removal
- Pad dimension reduction



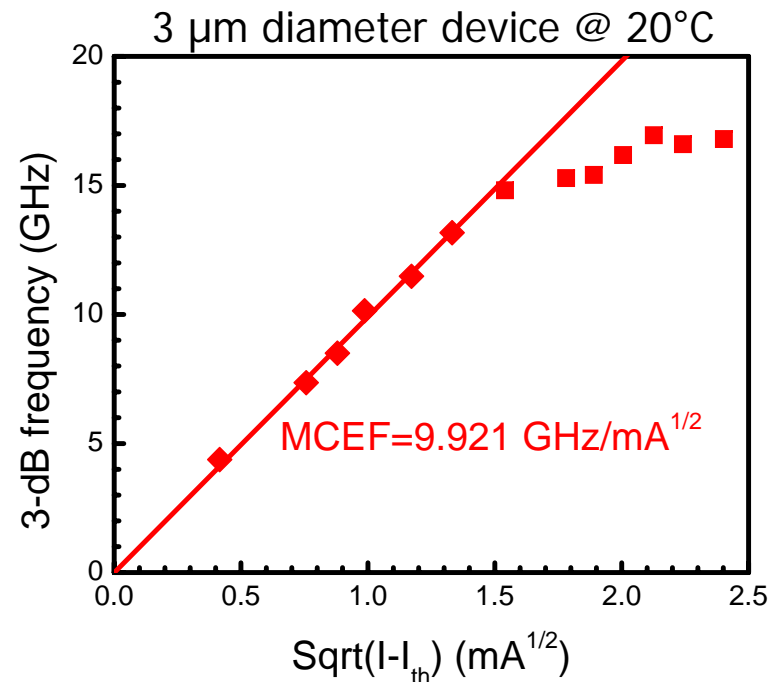
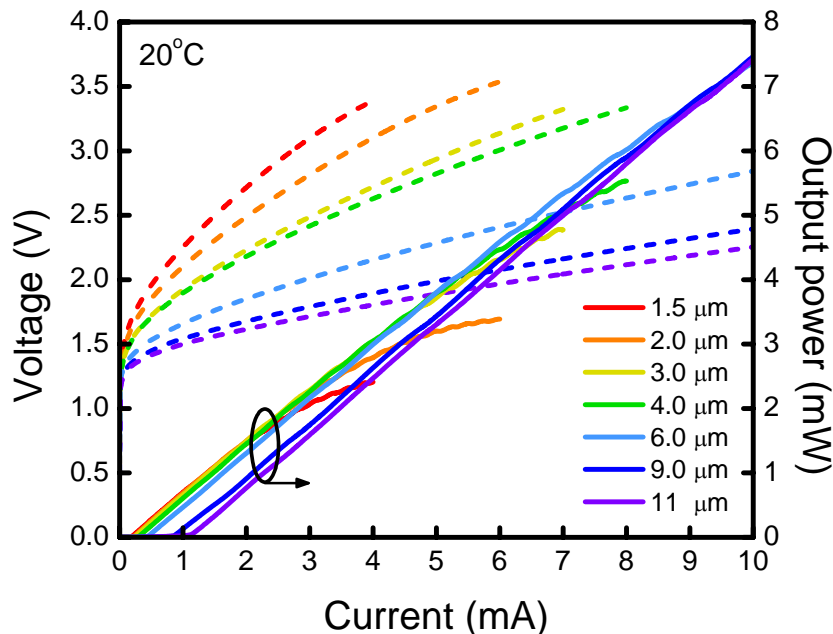
Original Tapered Oxide Aperture

Original design with long taper



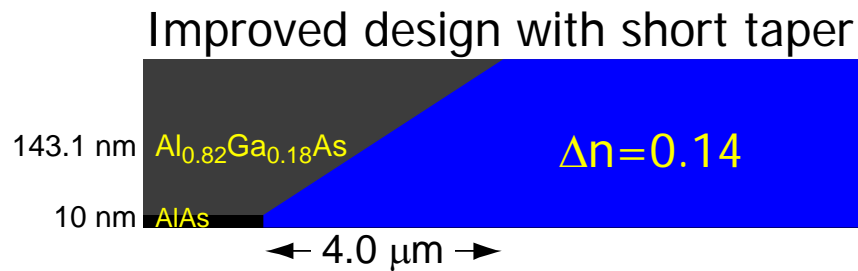
With long tapered oxide aperture:

- Constant DQE of 67%
- ⇒ Optical scattering loss is negligible down to $1.5 \mu\text{m}$ diameter devices
- MCEF = $9.9 \text{ GHz}/\text{mA}^{1/2}$
- ⇒ Insufficient lateral mode confinement



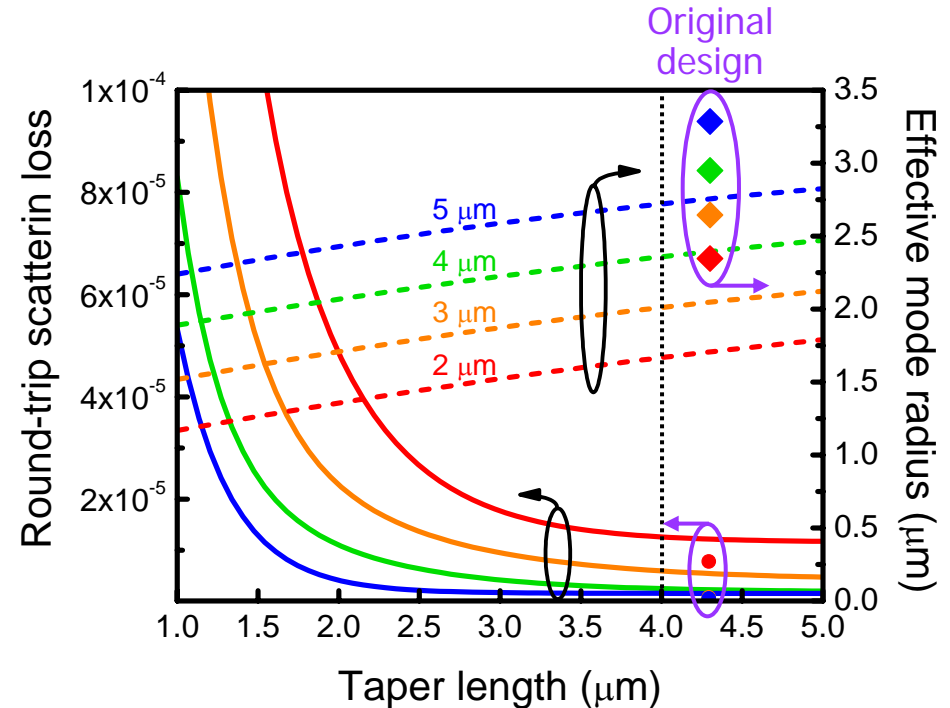
Improved Tapered Oxide Aperture

$$f_r = \frac{1}{2\pi} \sqrt{\frac{v_g a}{h\nu V_p} \eta_i (I - I_{th})}$$



Advantages:

- Better mode confinement
- ($V_p \rightarrow V_p/1.73$; $f_R = 1.31X$ with DBR)
- Does not introduce significant optical loss
- Lower parasitic capacitance due to thicker oxide



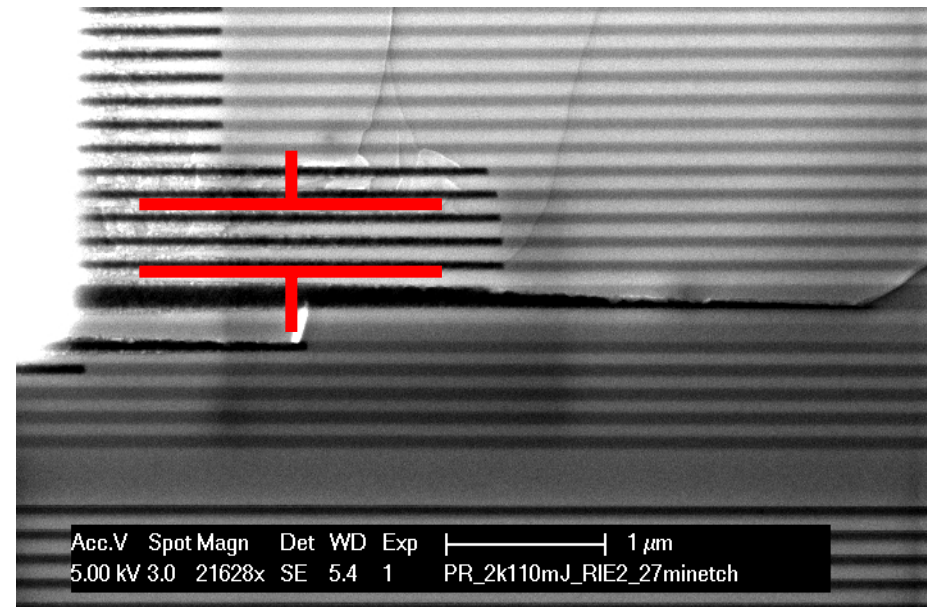
E. R. Hegblom *et al.*, *IEEE J. Sel. Top Quantum Electron.*, vol. 3, pp. 379–389, 1997

How to reduce the parasitic capacitance?

- **Common approach: Proton implantation**
 - >400 keV is needed to get close to the active region
 - Require thick mask material, e.g. 2.3 μm Au, complicating the process
 - Extra expense
- **Our approach: Deep oxidation layers**
 - Increase Al fraction of 5 AlGaAs DBR layer from 85% to 93% to form deep oxidation layers

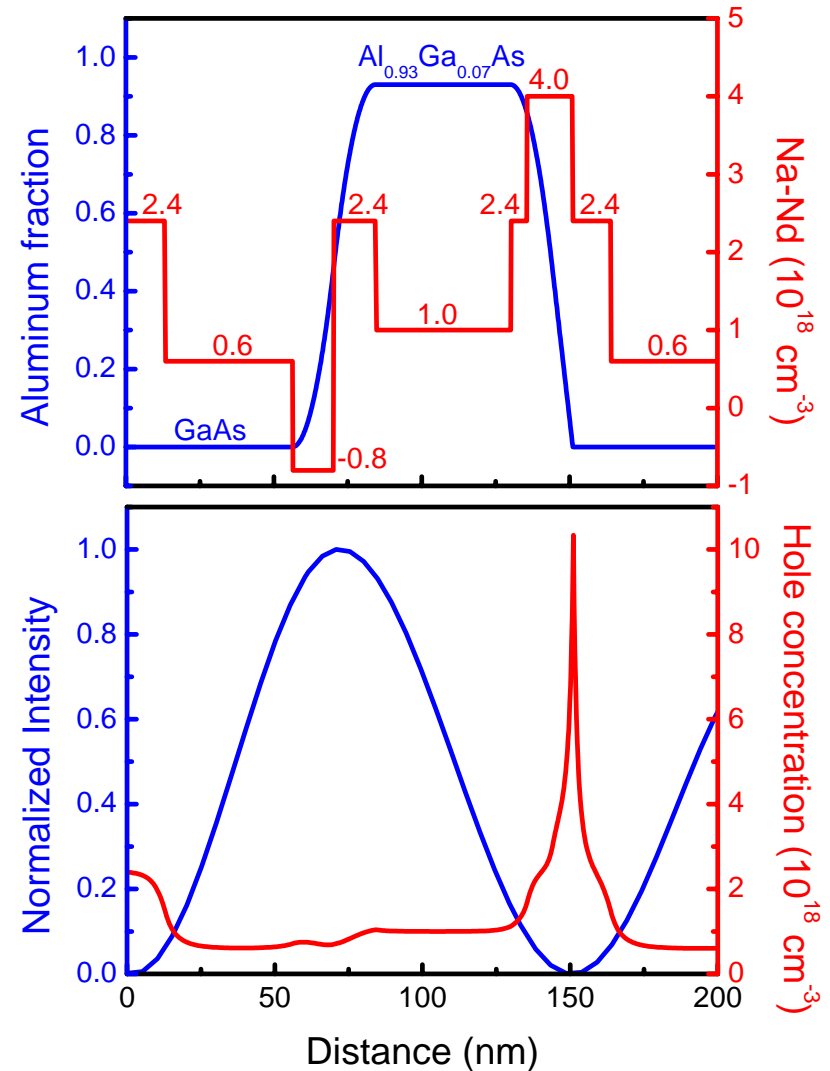
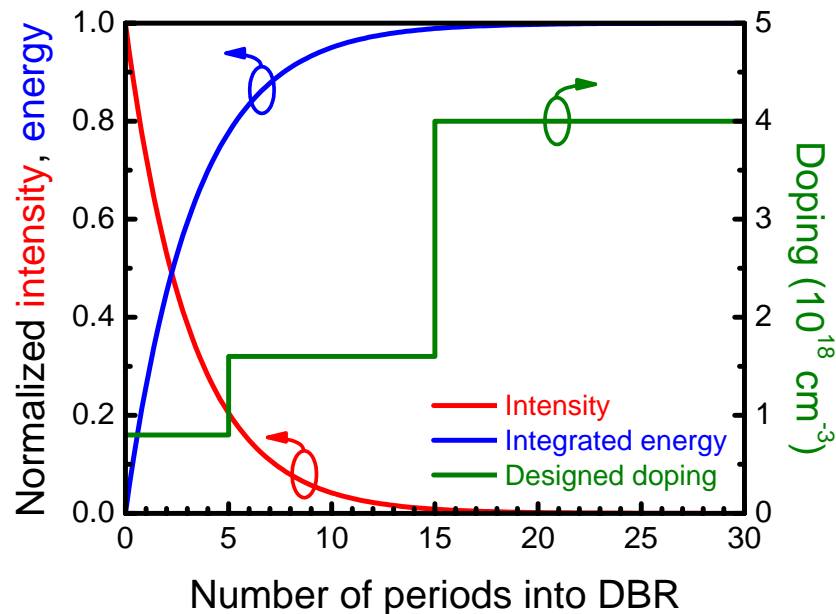
Advantages:

- Process remains unchanged
- Shorten the effective cavity length in the unoxidized region ($f_R +$)
- Cost effective



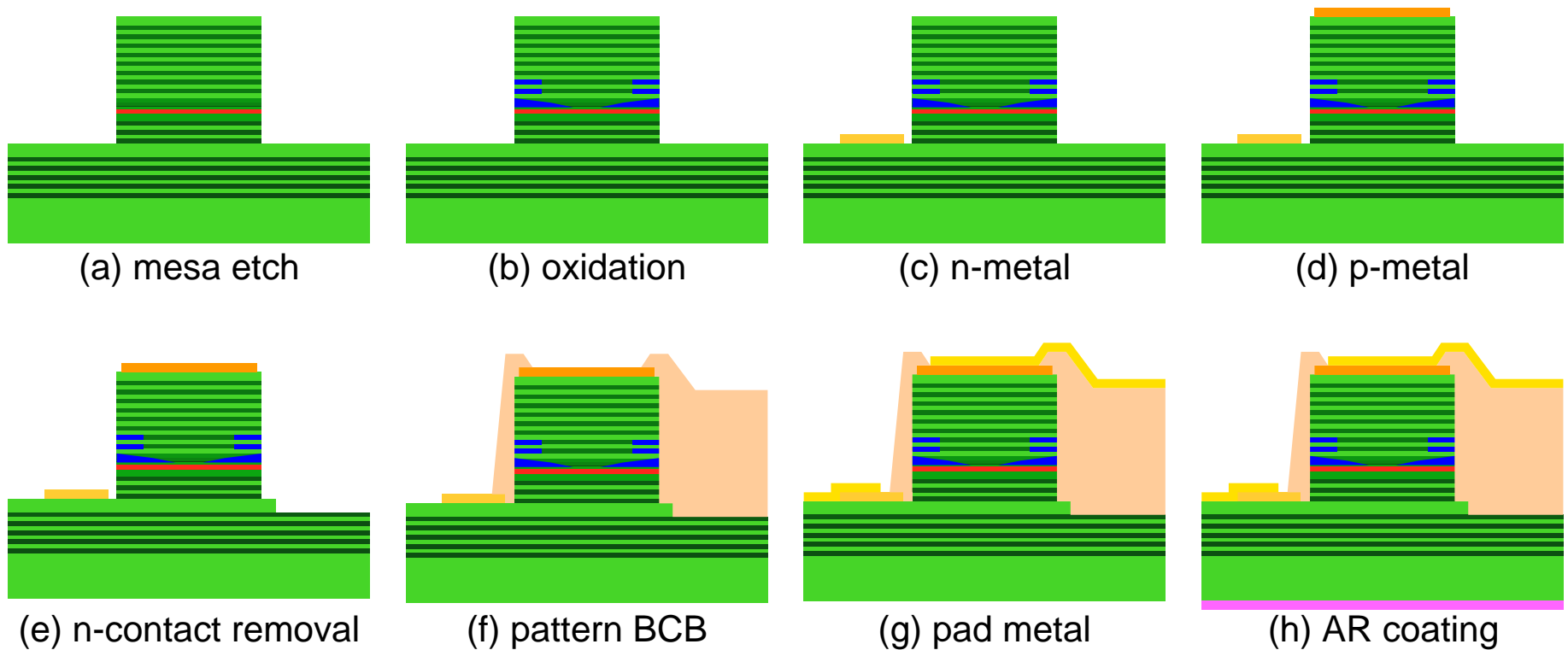
P-DBR Doping Schemes

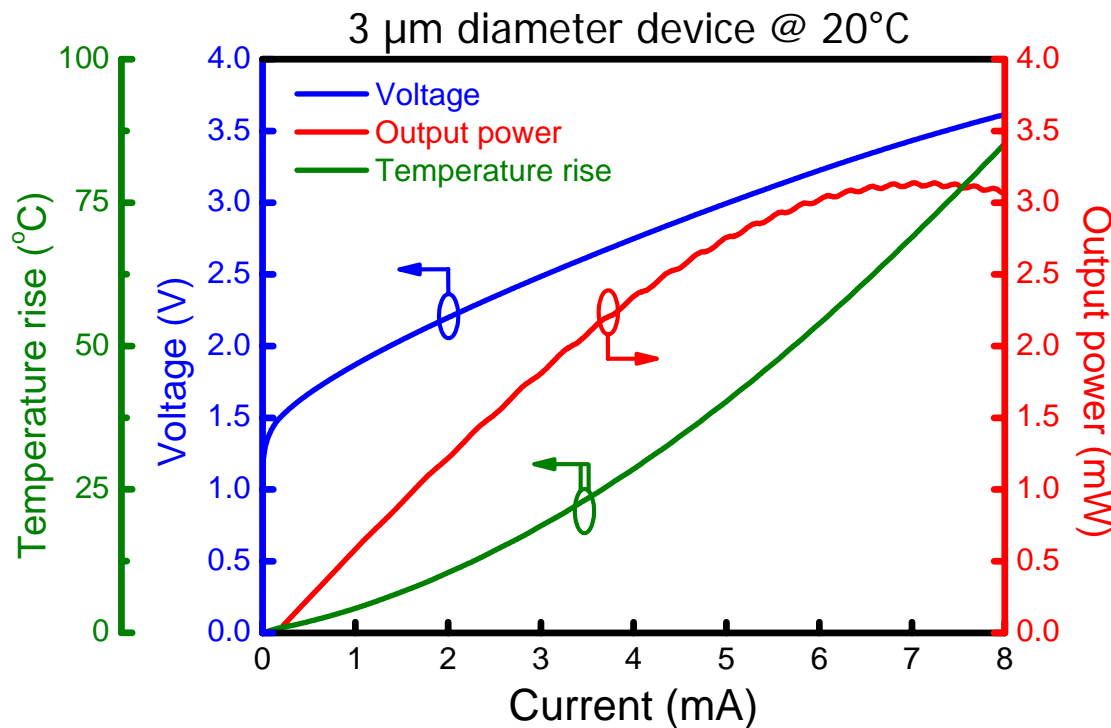
- Overall p -mirror doping profile
 - Optimize for loss-resistance product
 - Individual DBR doping profile
 - Reduce hetero-barriers for valence band
 - Minimize free carrier absorption loss
- ⇒ Standing-wave peaks: bi-parabolic scheme¹
 ⇒ Standing-wave nulls: uni-parabolic scheme²



1. M.G. Peters *et al.*, *Appl. Phys. Lett.*, vol. 63, pp. 3411–397, 1993
 2. K.L. Lear *et al.*, *Appl. Phys. Lett.*, vol. 68, pp. 605–607, 1996

- Fabrication is compatible with existing VCSEL process
- Can be easily mass manufactured in large volume
- Do not require proton implantation





Extracted parameters:

$$I_{th} = 0.144 \text{ mA}$$

$$\text{DQE} = 54\% \text{ (} 0.67 \text{ W/A)}$$

$$V_{th} = 1.47 \text{ V}$$

$$R_s \sim 250 \ \Omega \text{ @ } 4.4 \text{ mA}$$

$$\eta_{w-p} = 31\%$$

$$P_{max} = 3.1 \text{ mW}$$

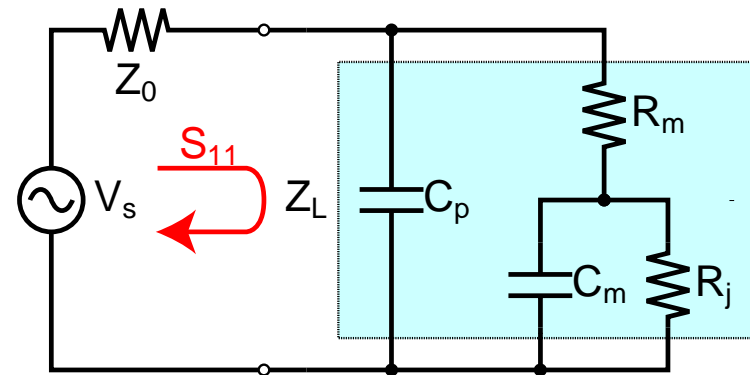
$$R_{th} = 3.3 \text{ }^\circ\text{C/mW}$$

- Very low threshold current and high slope efficiency
 \Rightarrow Short tapered oxide aperture does not introduce excess scattering loss
- Low threshold voltage (220 meV larger than photon energy)
 \Rightarrow Optimized p -doping and low threshold current

Parasitic Extraction

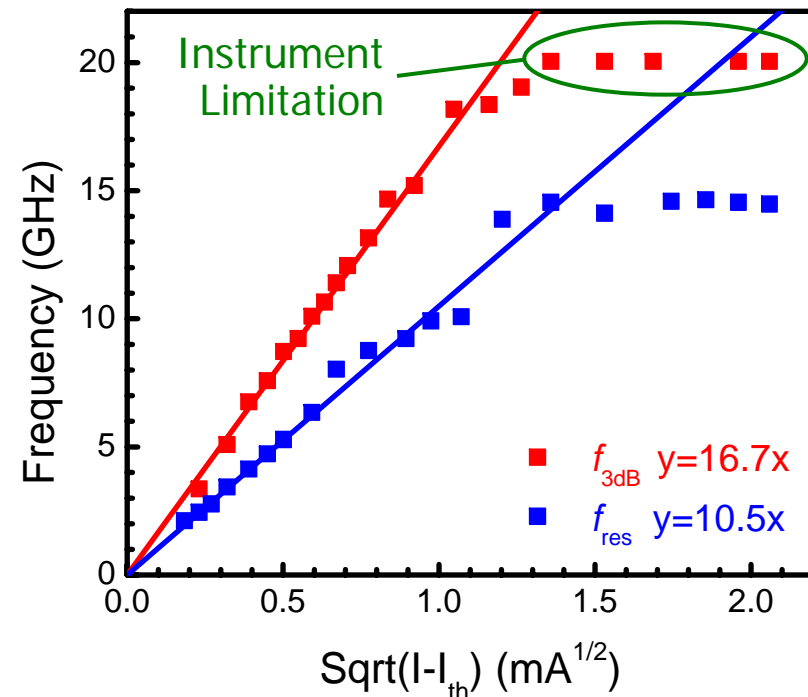
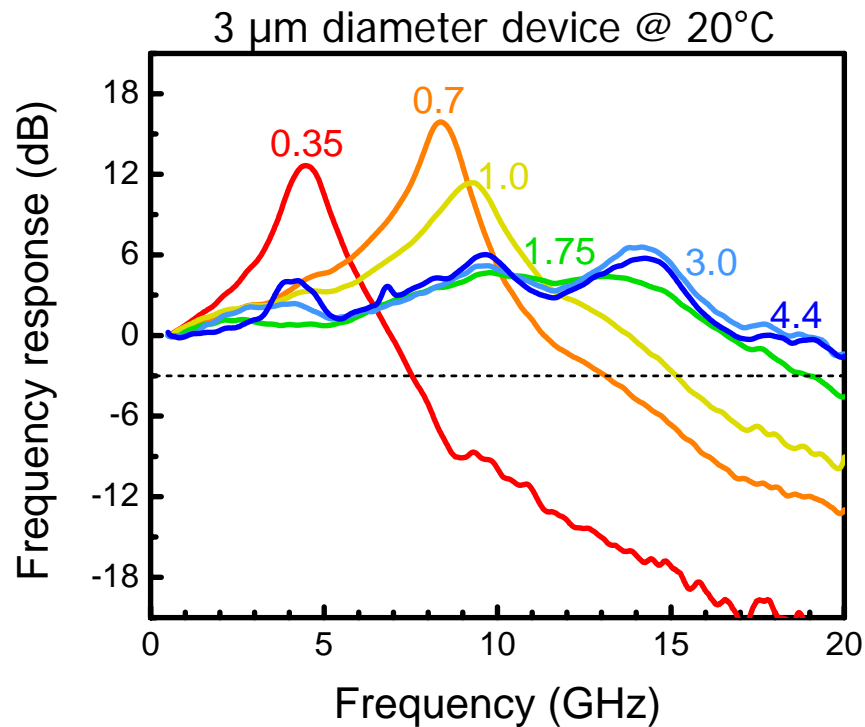
Parasitics are extracted by fitting S11 parameters at different bias currents

- R_m and C_p are bias independent
- R_j and C_m are bias dependent
- Fitted $R_m = 102 \Omega$, $C_p = 29 \text{ fF}$



Current (mA)	1.0	2.0	3.0	4.5	6.0
R_j (Ω)	274.4	192.7	168.2	146.5	126.7
C_m (fF)	57.1	66.7	75.4	87.9	100
Parasitic BW (GHz)	27	25.9	24.6	22.8	21.8

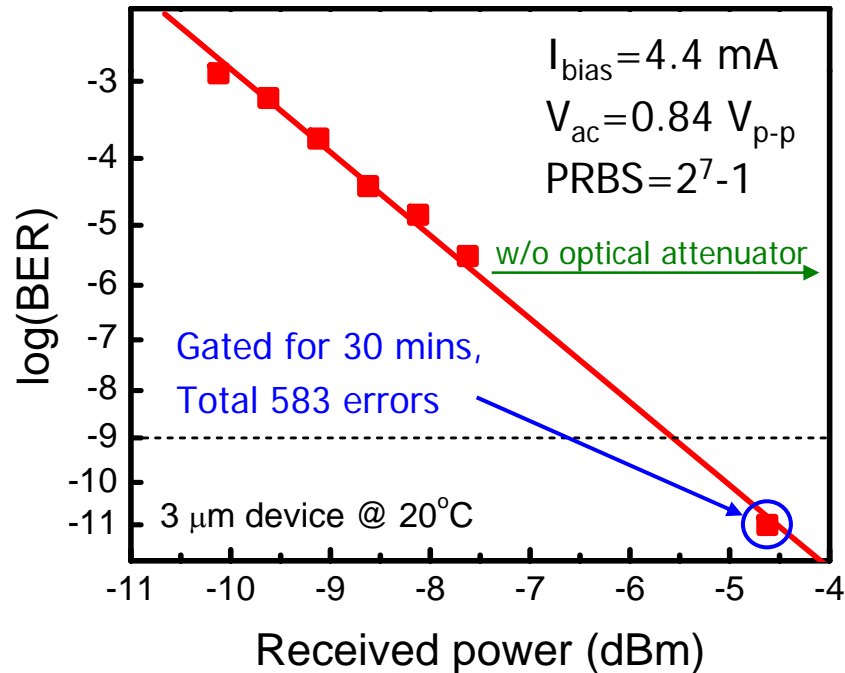
- BCB, n -contact removal, and small pad \Rightarrow Low C_p
- Deep oxidation layers and thicker oxide aperture \Rightarrow Low C_m
- Small size \Rightarrow High R_m and R_j



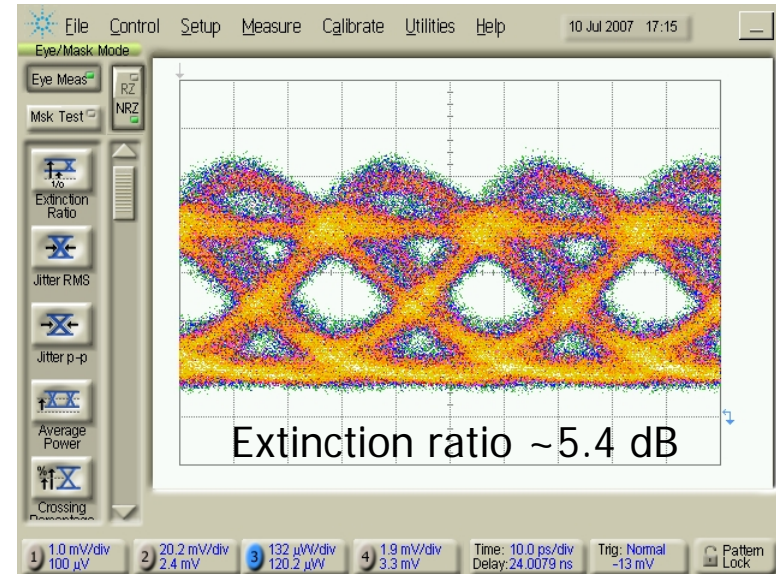
- Bandwidth exceeding 20 GHz at bias currents >2 mA, highest for 980 nm VCSELs
- MCEF = $16.7 \text{ GHz}/\text{mA}^{1/2}$, very close to the highest reported $16.8 \text{ GHz}/\text{mA}^{1/2}$ for quantum-well-based VCSELs¹

1. K. L. Lear *et al.*, *Electron. Lett.*, vol. 32, pp. 457–458, 1996.

BER curve @ 35 Gb/s

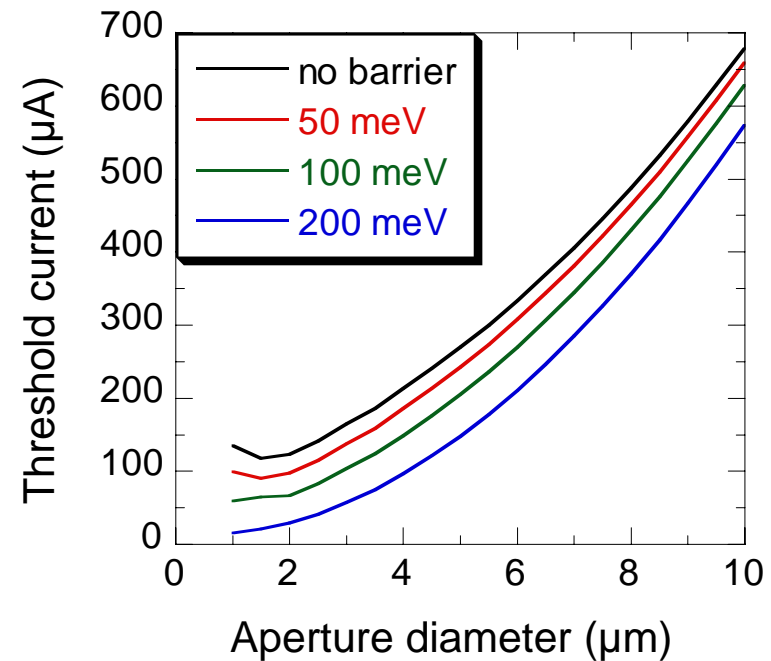
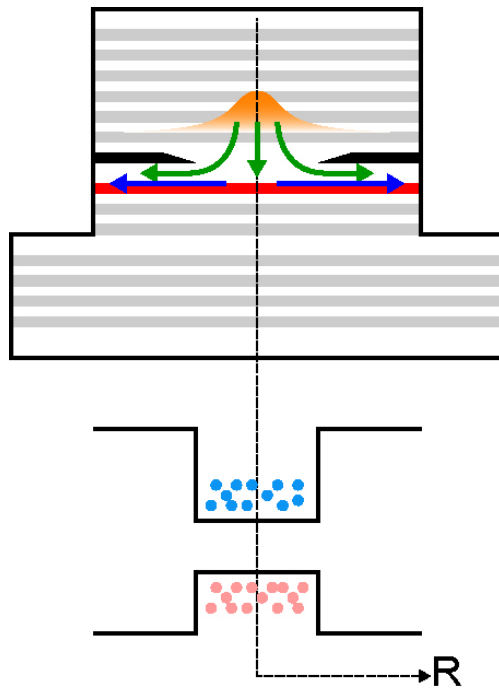


Optical eye diagram @ 35 Gb/s



- First demonstration of 35 Gb/s error-free operation for directly modulated VCSELs
- Bias current is 4.4 mA, corresponding to 10 mW power dissipation. Highest data-rate/power-dissipation ratio of 3.5 Gbps/mW

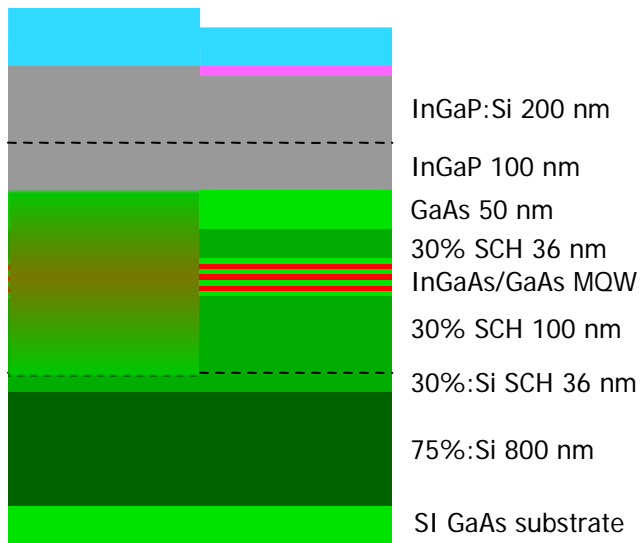
Why Lateral Carrier Confinement?



- Once carriers enter the QWs, they diffuse outwards and do not provide gain
- Confine carriers by creating barriers laterally using quantum well intermixing
- For smaller devices, a large portion of carriers are wasted
- Lateral carrier confinement can significantly reduce the threshold current

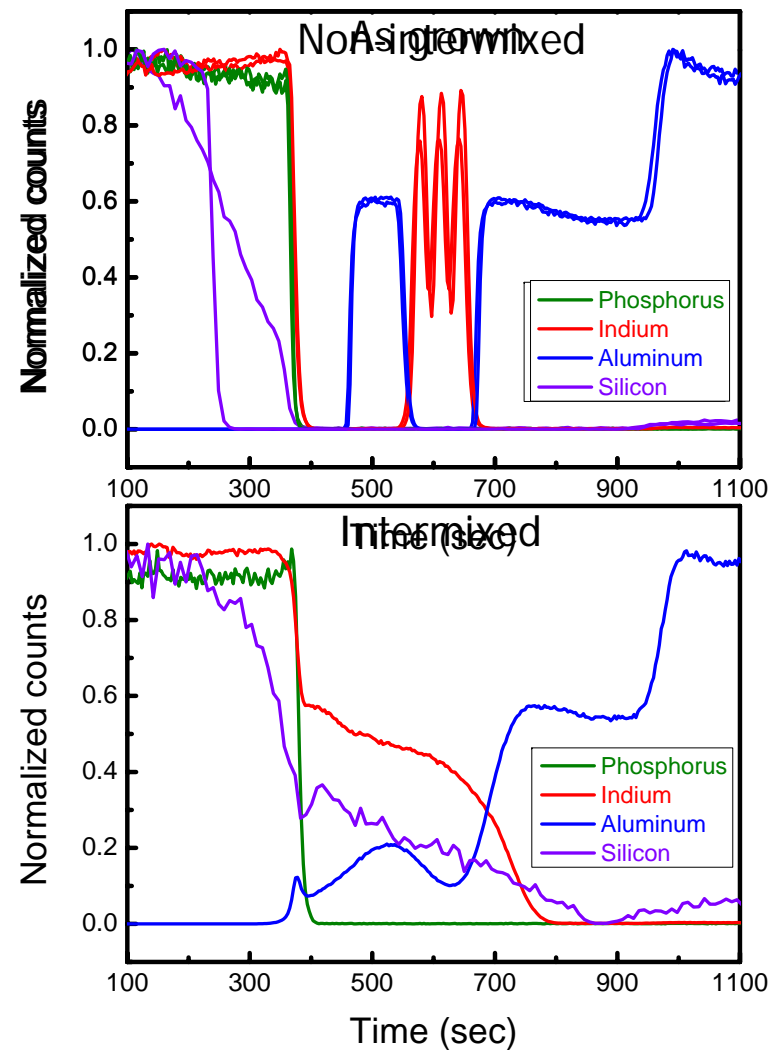
Quantum Well Intermixing Process

- Cap with SiO₂ enhances intermixing
 - Absorb Ga atoms and leave Ga vacancies
- Fluorination suppresses intermixing
 - Bond Ga atoms and not create vacancies
- QWI Process
 - Deposit 100 nm SiO₂ and pattern it
 - Fluorinates surface using CF₄ in RIE
 - Deposit 200 nm SiO₂
 - RTA 850°C 8 min

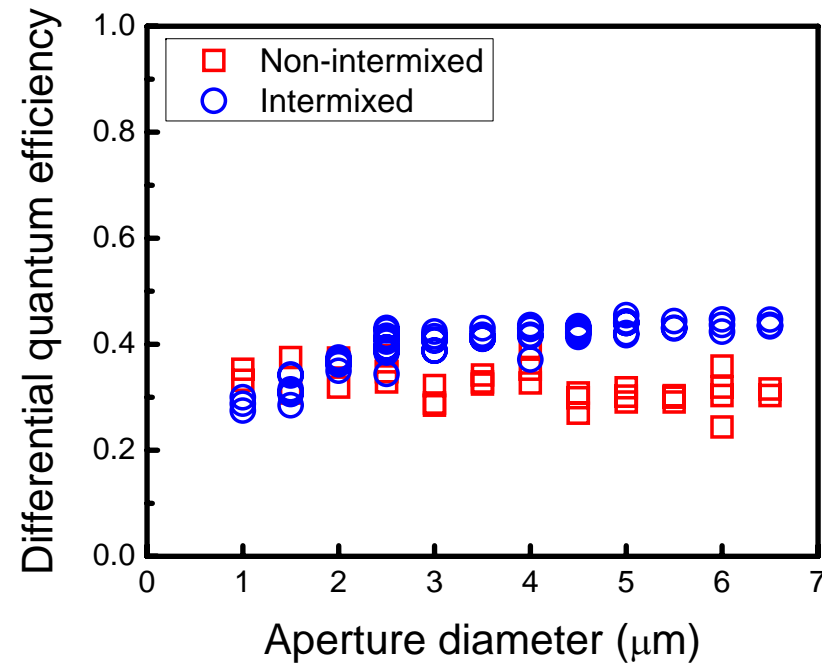
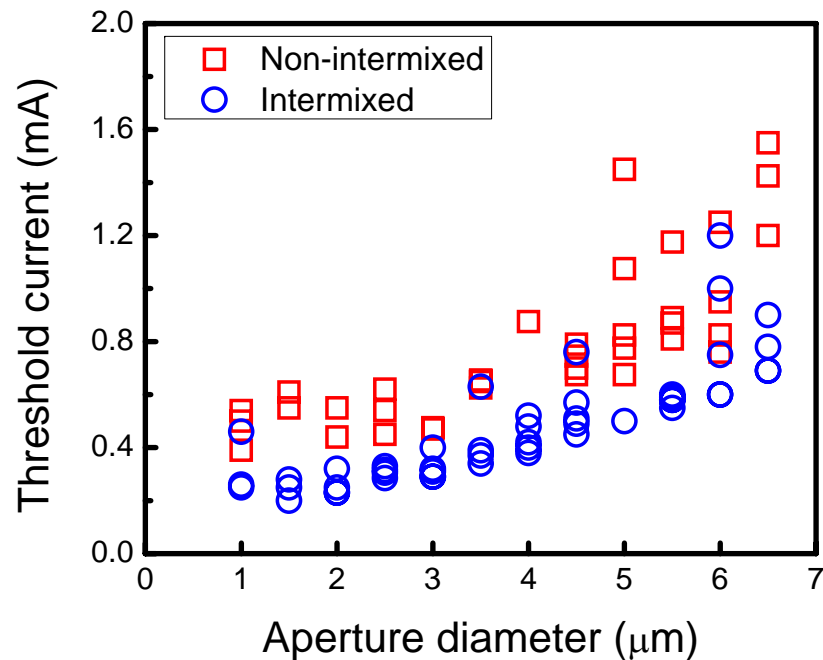


Intermixing test structure

SIMS results



Preliminary QWI VCSEL Results



- Overall threshold currents are increased, most likely due to increased loss from the regrowth interfaces
- However, devices that have been intermixed do show improvement over non-intermixed devices

To improve VCSEL high-speed performance:

- Redesign oxide aperture for better mode confinement but still maintain low optical losses: ($V_p \rightarrow V_p/1.73$; $f_R = 1.31 X$ with high Δ DBR)
- Reduce parasitics with deep oxidation layers and optimized p -mirror

We have demonstrated:

- Highest bandwidth (>20 GHz) for 980 nm VCSELs
- Error-free operation at 35 Gb/s at $I_{\text{bias}} = 4.4$ mA, $P_{\text{diss}} = 10$ mW
 - First demonstration of directly modulated VCSELs up to 35 Gb/s
 - Highest data-rate/power-dissipation ratio of 3.5 Gbps/mW

Potential improvement using quantum well intermixing to achieve lateral carrier confinement in VCSELs

- Process developed
- Preliminary results are promising