

Combinational Logic Building Blocks and Bus Structure

ECE 152A – Winter 2012

Reading Assignment

- Brown and Vranesic
 - 3 Implementation Technology
 - 3.8 Practical Aspects
 - 3.8.7 Passing 1s and 0s Through Transistor Switches
 - 3.8.8 Fan-In and Fan-Out in Logic Gates
 - Tri-State Buffers (only this section of 3.8.8)
 - 3.9 Transmission Gates
 - 3.9.2 Multiplexer Circuit

Reading Assignment

■ Brown and Vranesic (cont)

- 6 Combinational-Circuit Building Blocks
 - 6.1 Multiplexers
 - 6.1.1 Synthesis of Logic Functions Using Multiplexers
 - 6.1.2 Multiplexer Synthesis Using Shannon's Expansion
 - 6.2 Decoders
 - 6.2.1 Demultiplexers
 - 6.3 Encoders
 - 6.3.1 Binary Encoders
 - 6.3.2 Priority Encoders
 - 6.4 Code Converters

Reading Assignment

■ Roth

- 9 Multiplexers, Decoders and Programmable Logic
 - 9.1 Introduction
 - 9.2 Multiplexers
 - 9.3 Three State Buffers
 - 9.4 Decoders and Encoders

Multiplexer

- Passes one of several data inputs to output
 - Generally 2^n data inputs and always a single data output
 - n control lines determine which input is “steered” to the output
- Allows logical (not “tri-state” or electrical) implementation of buses
 - Buses and register transfer operations fundamental to digital system design

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Multiplexer

- Also possible to implement arbitrary combinational logic with multiplexers
 - Universal, combinational logic element
- Also known as “Data Selector” and “Mux”
- In sequential operation, provides parallel to serial conversion

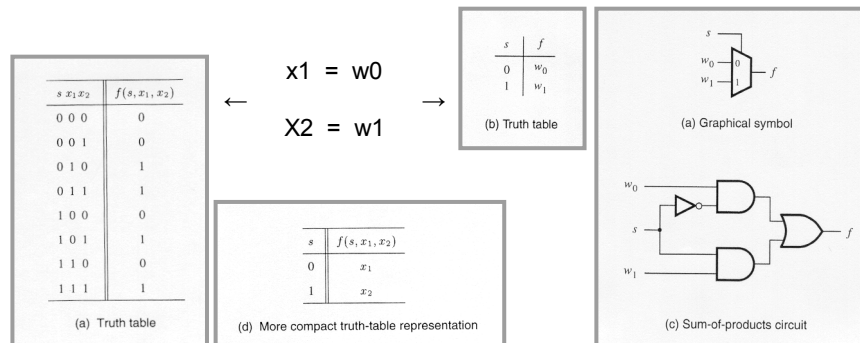
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Two-to-One Multiplexer

■ $F = \text{Select}' \cdot x_0 + \text{Select} \cdot x_1$



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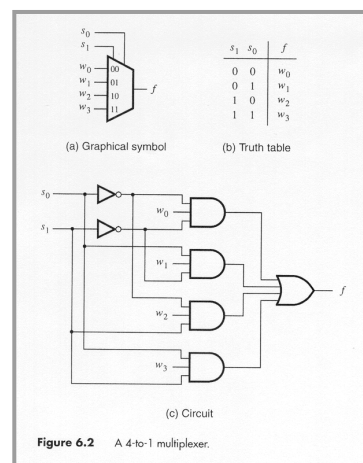
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Four-to-One Multiplexer

- i^{th} data input ANDed with minterm m_i
 - Embedded circuit generating minterms will become known as a decoder

$$f = \bar{s}_1 \bar{s}_0 w_0 + \bar{s}_1 s_0 w_1 + s_1 \bar{s}_0 w_2 + s_1 s_0 w_3$$

$m_0 w_0$ $m_1 w_1$ $m_2 w_2$ $m_3 w_3$



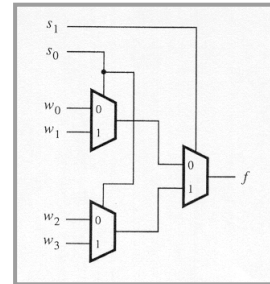
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Building Larger Multiplexers

- 4-to-1 (4:1) Mux using 2-to-1 (2:1) Muxes
 - Simple and modular
 - Adds 2 levels of gate (propagation) delay



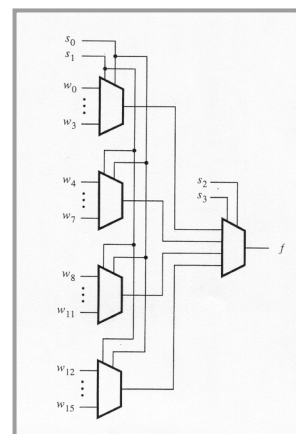
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Building Larger Multiplexers

- 16:1 Mux constructed from 4:1 Muxes
 - Expandable to 32:1 and 64:1 with additional 2:1 and/or 4:1 Muxes
 - With additional levels of propagation delay



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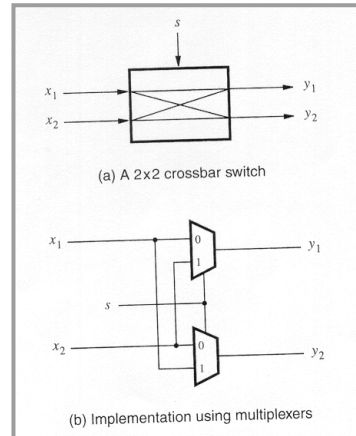
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Multiplexer Application

■ Crossbar Switch

- In general, n-inputs by n-outputs
 - Connectivity is any input to any output
- Important component of networking hardware
 - The bigger, the faster, the better...



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Combinational Design Using Multiplexers

■ Input variables applied to Mux select lines

- “Steer” (constant) value of function to output
 - Allows implementation of n-variable function with 2^n -to-1 multiplexer
- “Steer” derived function (a variable, its complement, the constant 1 or the constant 0) to the output
 - Allows implementation of n-variable function with 2^{n-1} -to-1 multiplexer

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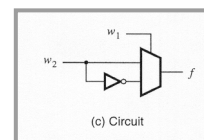
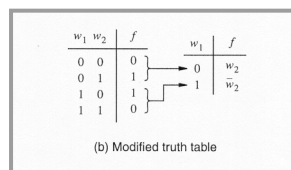
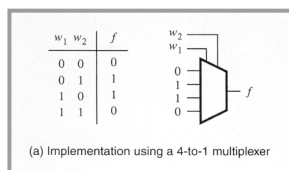
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Combinational Design Using Multiplexers

■ Example 1: XOR Function

- Using a 4:1 Mux
- The modified Truth Table
 - Possibilities are $x, x', 0, 1$
- The 2-input XOR using a 2:1 Mux



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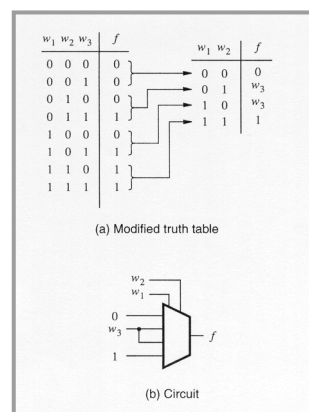
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Combinational Design Using Multiplexers

■ Example 2 : Three input majority function

- Three input function with $(2^{n-1}-to-1)$ 4:1 Mux



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Combinational Design Using Multiplexers

■ Multiplexer Synthesis Using Shannon's Expansion

- By adding gate level circuitry to Mux inputs, an arbitrary combinational function can be realized with a 2-to-1 Mux
 - Externally generating a function of one of the variables

Shannon's Expansion Theorem Any Boolean function $f(w_1, \dots, w_n)$ can be written in the form

$$f(w_1, w_2, \dots, w_n) = \overline{w_1} \cdot f(0, w_2, \dots, w_n) + w_1 \cdot f(1, w_2, \dots, w_n)$$

Combinational Design Using Multiplexers

■ Example 3 : Three input majority function with 2:1 Mux

- Algebraic expansion

$$f(w_1, w_2, w_3) = (w_1 w_2 + w_1 w_3 + w_2 w_3)$$

$$f(w_1, w_2, w_3) = (w_1 w_2 + w_1 w_3 + w_2 w_3)(w_1' + w_1)$$

$$f = w_1'(w_1 w_2 + w_1 w_3 + w_2 w_3) + w_1(w_1 w_2 + w_1 w_3 + w_2 w_3)$$

... and from Shannon

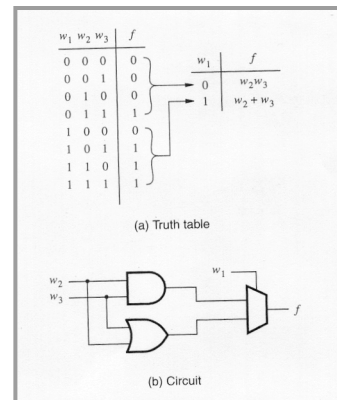
$$f = w_1'(0w_2 + 0w_3 + w_2 w_3) + w_1(1w_2 + 1w_3 + w_2 w_3)$$

$$f = w_1'(w_2 w_3) + w_1(w_2 + w_3)$$

Combinational Design Using Multiplexers

■ Example 3: Three input majority function with 2:1 Mux

- Truth Table and circuit implementation



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Combinational Design Using Multiplexers

■ Shannon's Expansion with 4:1 Mux

- Three input majority function
 - Expansion in terms of w_1 and w_2
 - Verifies earlier (heuristic) solution

$$\begin{aligned}
 f(w_1, w_2, w_3) &= (w_1 w_2 + w_1 w_3 + w_2 w_3) \\
 f &= w_1' w_2' (00 + 0w_3 + 0w_3) + w_1' w_2 (01 + 0w_3 + 1w_3) \\
 &\quad + w_1 w_2' (10 + 1w_3 + 0w_3) + w_1 w_2 (11 + 1w_3 + 1w_3) \\
 f &= w_1' w_2' (0) + w_1' w_2 (w_3) + w_1 w_2' (w_3) + w_1 w_2 (1)
 \end{aligned}$$

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Multiplexers and Buses

- Bus allows data transfers between multiple sources and single or multiple destinations over a shared path (wires)
 - Bus includes multiple bits
 - Parallel data bus
 - Only one source on the bus at any time
 - Bus contention

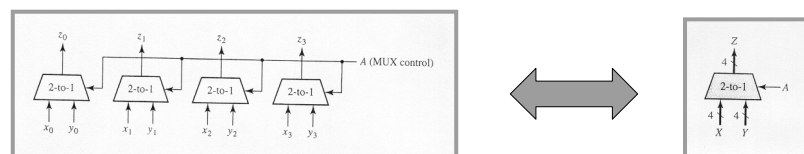
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Multiplexers and Buses

- Example below illustrates two, four-bit words (X and Y) multiplexed onto the Z bus
 - Register transfer operations
 - $A' : Z \leftarrow X, A : Z \leftarrow Y$



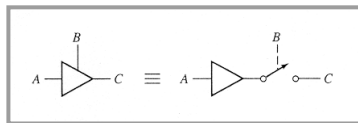
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Tri-State Outputs

- Utilizes third, high impedance output state
 - In Hi-Z state, output appears as an open circuit to bus connection
 - Mux disconnects from bus logically, tri-state output device disconnects electrically



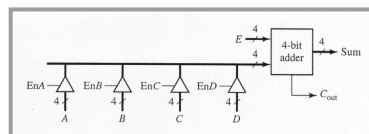
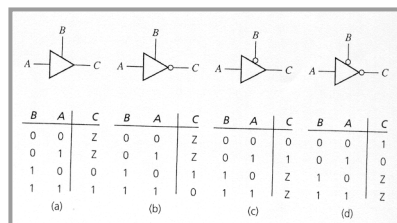
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Tri-State Outputs (cont)

- Flavors of tri-state outputs and control
- Bus implementation



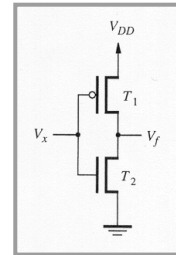
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NMOS and PMOS Transistors

- Recall static CMOS circuits
 - Logic high output passed to output through PMOS transistor(s)
 - PMOS transistor passes “good” 1 and “bad” 0
 - Logic low output passed to output through NMOS transistor(s)
 - NMOS transistor passes “good” 0 and “bad” 1
 - “Good” 0s and 1s are GND and V_{DD}
 - “Bad” 0s and 1s have degraded DC voltage (logic) levels



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NMOS and PMOS Transistors

- Degradation of DC signal levels is a result of the “threshold voltage” (V_T) of transistor and the “body effect”
 - To “turn on” the transistor, the gate to source voltage (V_{GS}) must exceed the transistor’s threshold voltage (V_T)
 - An NMOS transistor has a positive V_T
 - A PMOS transistor has a negative V_T
 - The threshold voltage itself is increased by the body effect by a factor of ~ 1.5

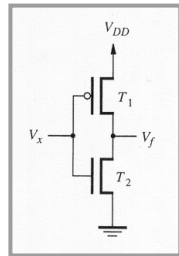
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NMOS and PMOS Transistors

- For the inverter below, assume the NMOS device has a V_T of 1V ($V_{GS} > 1V$) and the PMOS device has a V_T of -1V ($V_{GS} < -1V$) and $V_{DD} = 5V$



Input = 5V, $V_{GS}(T1) = 5V$ (off), $V_{GS}(T2) = 5V$ (on)
Output = 0V (GND)

Input = 0V, $V_{GS}(T1) = -5V$ (on), $V_{GS}(T2) = 0V$ (off),
Output = 5V (V_{DD})

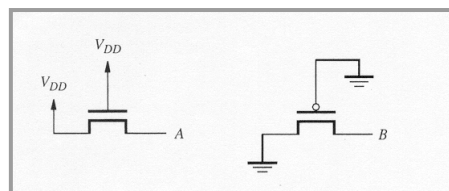
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NMOS and PMOS Transistors

- Bad 1s (NMOS) and Bad 0s (PMOS)
 - $V_A = V_{DD} - V_T$ (NMOS)
 - Input going high; turns off at $V_{GS} = V_T$
 - $V_B = -V_T$ (PMOS)
 - Input going low; turns off at $V_{GS} = V_T$



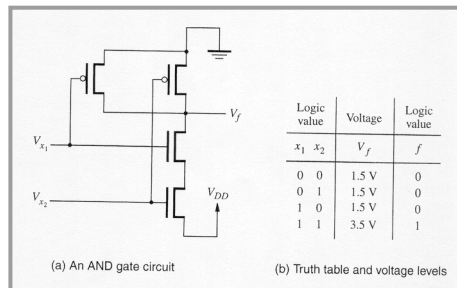
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CMOS AND Gate

- Note degradation in DC signal (logic) levels
 - AND Gates are never built this way in CMOS



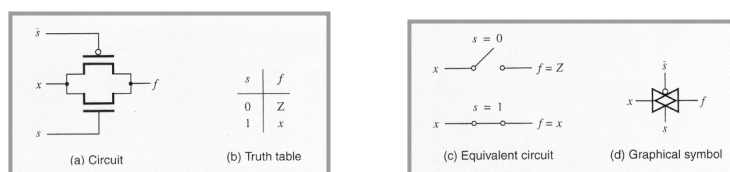
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The CMOS Transmission Gate

- When enabled, the CMOS Transmission Gate:
 - Passes “good” 1s (through the PMOS transistor)
 - Passes “good” 0s (through the NMOS transistors)
- When disabled, the CMOS Transmission gate acts like a Tri-State Buffer



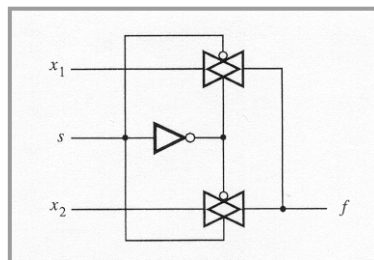
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CMOS Transmission Gate MUX

- 2:1 Multiplexer implementation with transmission gates



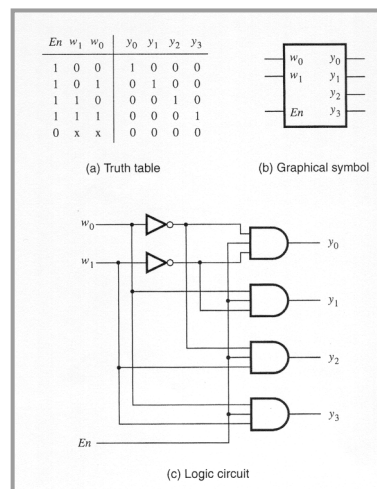
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Decoders

- 2-to-4 Decoder shown
 - 2-to- 2^n in general
 - Enable input allows construction of decoder tree and demultiplexer
 - Generates all minterms when enabled
 - Multiple output circuits
 - One hot decoding



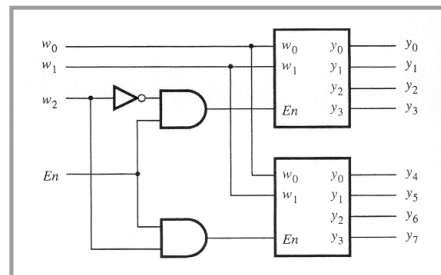
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Decoder Tree

- One-bit expansion (3-to-8) by adding external decoding circuitry



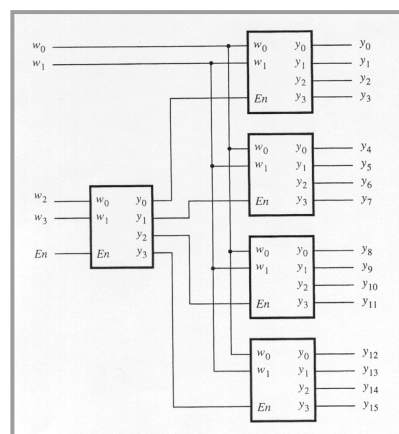
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Decoder Tree

- Two-bit expansion (4-to-16) by adding another 2-to-4 decoder



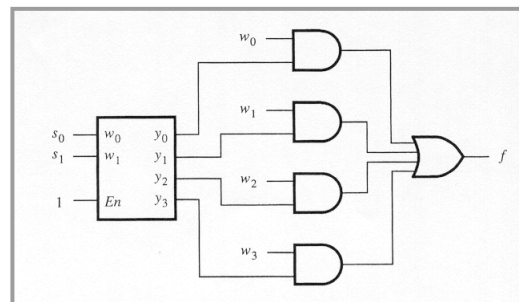
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Decoder Applications

- Multiplexer from decoder
 - Recall “embedded decoder”



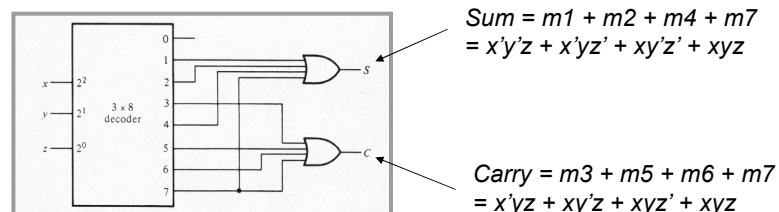
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Decoder Applications

- Multiple Output Circuits
 - Full Adder using 3 X 8 Decoder



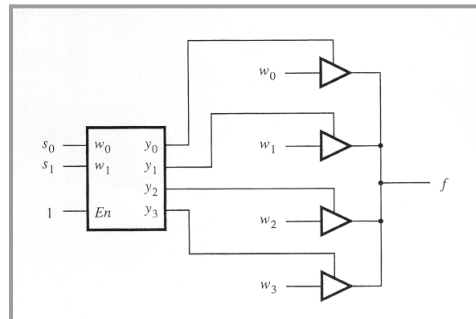
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Decoder Applications

■ Decoder Bus Control/Multiplexer



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Demultiplexers

- Serial to parallel conversion
 - Send a single data bit to a specific address
- A 1-to- 2^n demultiplexer is implemented using an n -to- 2^n decoder
 - The (value of) the data is applied via the enable input
- Valuable circuit in sequential circuits
 - Not so much in combinational circuits
- Also referred to as Dmux's

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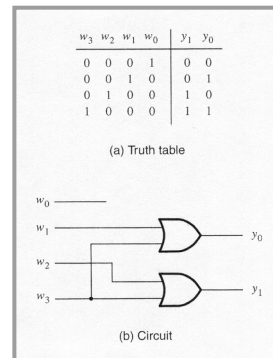
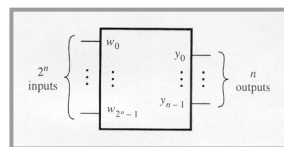
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Encoders

■ Binary Encoders

- “One hot” input, binary (or other code) representation output
- Reverse of decoder



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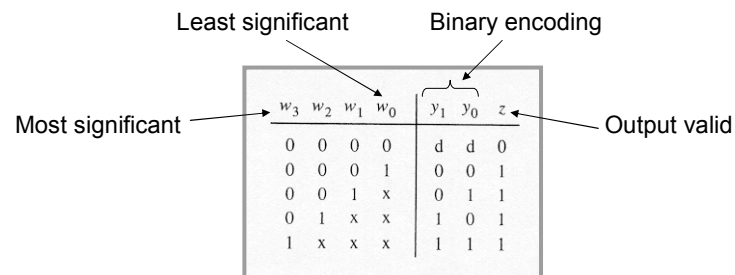
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Encoders

■ Priority Encoders

- Used in prioritizing interrupts (or other events)



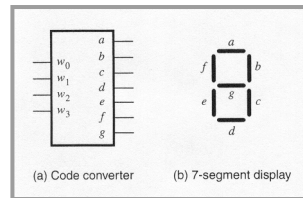
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Code Converters

■ BCD to 7-Segment Display Code Converter



| w_3 | w_2 | w_1 | w_0 | a | b | c | d | e | f | g |
|-------|-------|-------|-------|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

(c) Truth table