

ECE137a Lab project 3

You will first be designing and building an op-amp. The op-amp will then be configured as a narrow-band amplifier for amplification of voice signals in a public address system .

Part 1

You must first design and construct an op-amp using a mixture of MOSFETs and bipolar transistors. The class AB output transistors must be MOSFETs. The VN0104 / VP0104 are recommended for this.

Design an operational amplifier to the following specifications:

Differential gain: greater than 10,000 at 1 Hz.

CMRR > 40 dB at 1 Hz

Power supplies = ± 5 V

Must be able to drive ± 2 Volts into $R_L = 10$ kOhm

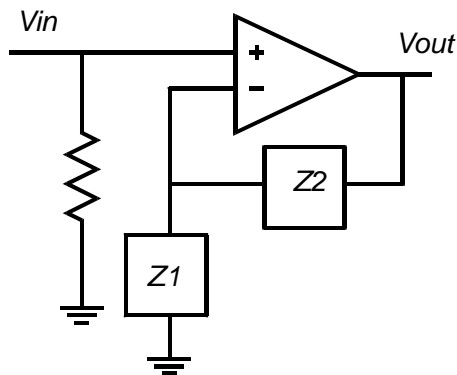
Differential input resistance > 20 kOhm.

*For stability of the feedback loop, the differential gain must vary as

$A_d(j\omega) = A_{dc}(1 + j\omega/\omega_{pole})^{-1}$, e.g. a single-pole rolloff with unity gain at

$\omega_{unity} = 2\pi f_{unity} = A_{dc}\omega_{pole}$. The unity-gain frequency f_{unity} should be designed to be between 1 MHz and 2 MHz. This point will be discussed in the background section.

Part 2



The circuit is then to be connected as so with impedances Z2 and Z1, both being RC networks. The network must be designed so that

$$V_{out}/V_{in} = 1 + \frac{jf/f_{low}}{1 + jf/f_{low}} \frac{A_{MB}}{1 + jf/f_{high}}$$

where $A_{MB} = 10 \pm 2\%$

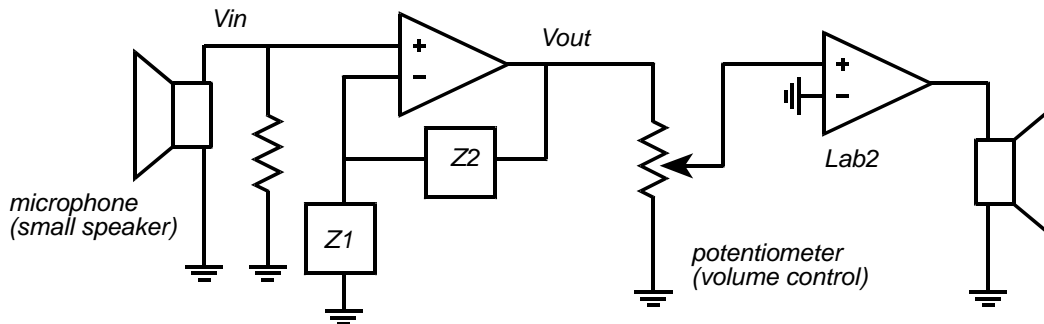
$f_{LOW} = 400$ Hz $\pm 10\%$

$f_{High} = 4$ kHz $\pm 10\%$

Gains are to be tested at 1 kHz, 40 Hz, 400 Hz, 4 kHz, and 40 kHz to verify.

The specific gain-frequency filtering is to band limit a voice signal to only those frequencies most important for intelligibility, removing high and low-frequency acoustic interference.

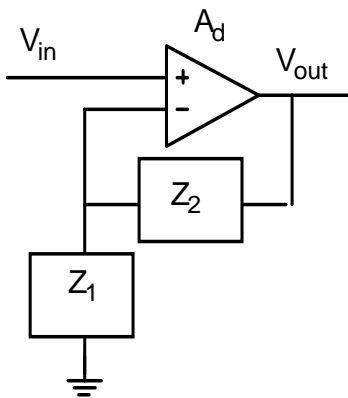
Part 3 (optional---for fun)



The op-amp will then be connected as such. This is a small public address system. Or, with long wires, a telephone. Verify the operation of the system, including the total gain at 1 kHz. Determine experimentally the microphone voltage produced with normal speech at 4 inch distance. Based upon this, is the overall gain sufficient to drive the power amplifier to its +/- 3 Volts clipping?

Background

Closed-Loop gain relationships with op-amps



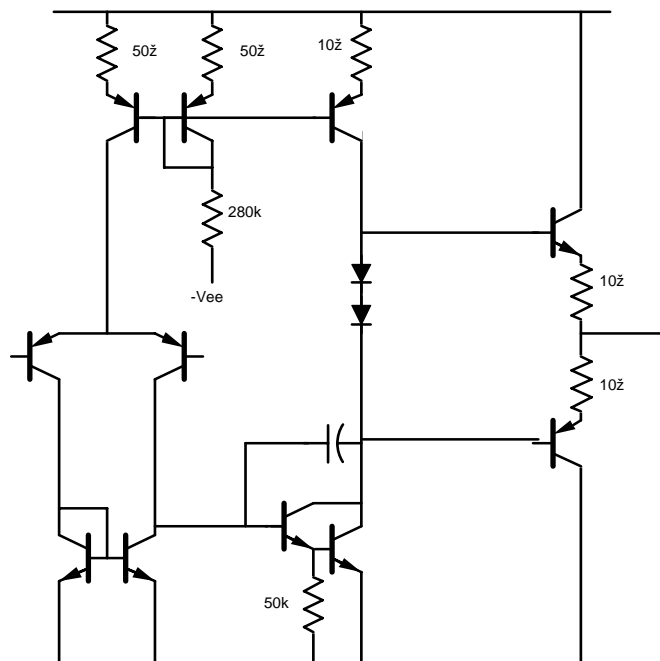
$$V_{out} / V_{in} = \frac{Z_1 + Z_2}{Z_1} \times \frac{A_d Z_1 / (Z_1 + Z_2)}{1 + A_d Z_1 / (Z_1 + Z_2)}$$

If the amplifier gain is reasonably large, so that $A_d Z_1 / (Z_1 + Z_2) \gg 1$, then

$$V_{out} / V_{in} \cong \frac{Z_1 + Z_2}{Z_1}, \text{ which is the desired mode of operation.}$$

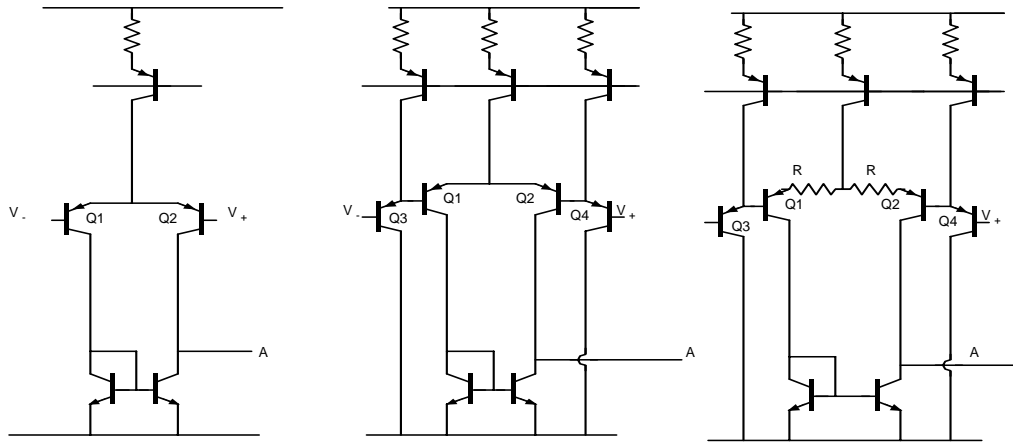
Amplifier stability and compensation

Negative feedback can become positive if there is 180° phase shift in the amplifier. This can and will happen at sufficiently high frequencies because of the amplifiers' high-frequency rolloff (due to transistor capacitances). If the feedback is positive and of magnitude greater than 1, then the feedback circuit will oscillate. To avoid this, the op-amp high-frequency response must be tailored so that the gain of the feedback loop decreases gracefully to below unity before the phase shifts add up to more than 180° . This is called compensation.



Above is one example op-amp circuit.

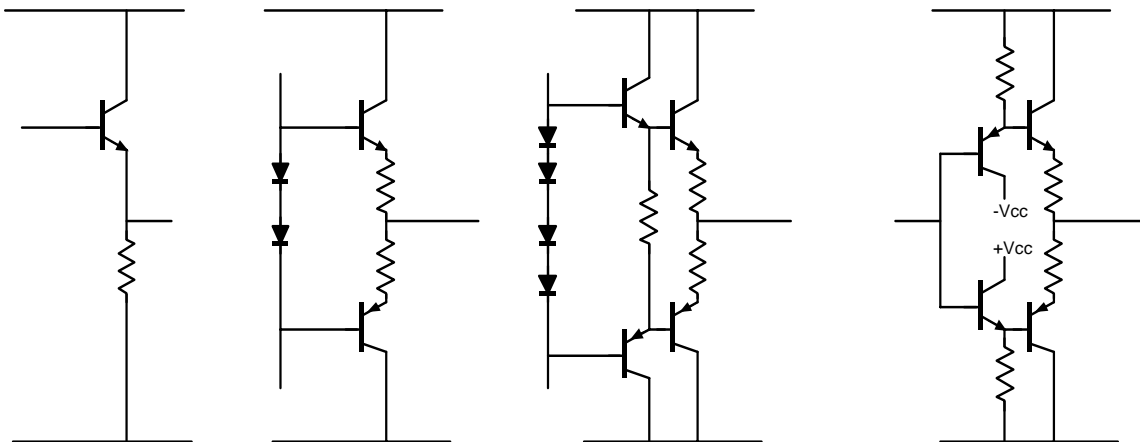
Most op-amps can be broken down into three parts: A differential input stage, a second voltage-gain stage, and an output buffer stage.

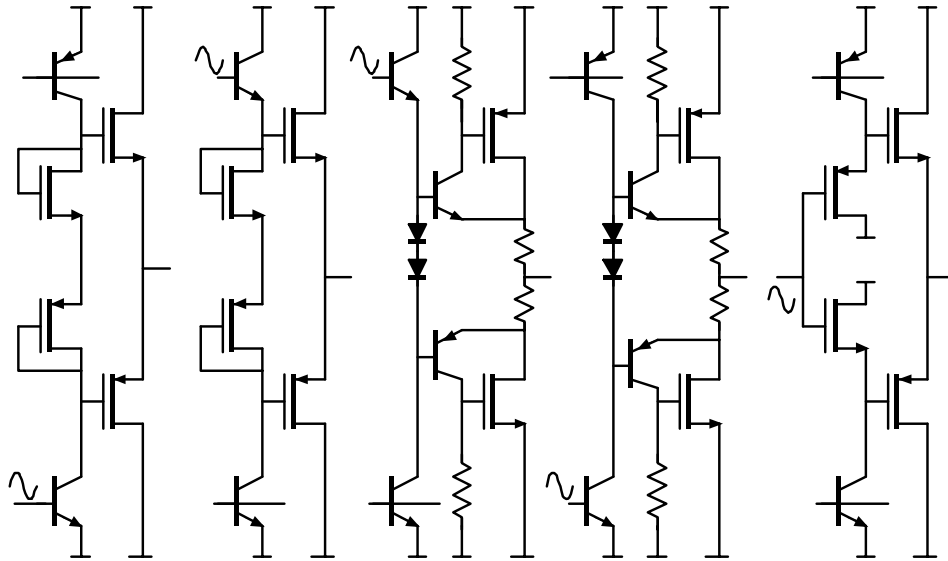


The input stage might look like any of the above 3 examples. If we apply symmetry, so that $g_{m1} = g_{m2}$, and the emitter-follower buffers have identical voltage gains $A_{v3} = A_{v4}$, then the overall voltage gains of these three input stage examples are:

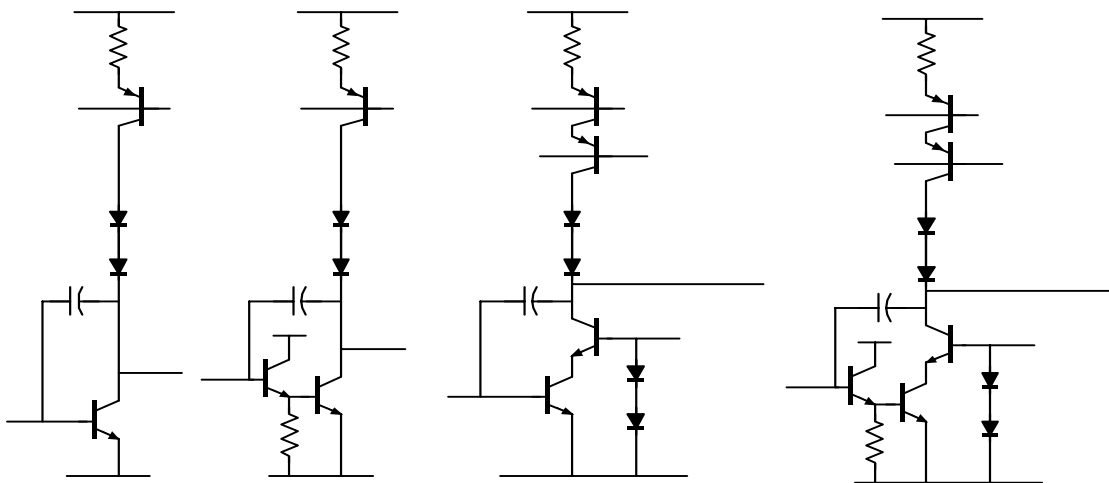
$A_v = g_{m1}R_{leq}$ (first example), $A_v = A_{v3}g_{m1}R_{Leq}$ (second example), and $A_v = A_{v3}R_{Leq}/(R + 1/g_{m1})$ (third example). You get the picture, and can generalize to any input stage design you like. (The factor of 1/2 has vanished in the gain expressions because of the current-mirror load: read the class notes...).

In general, from the above, we can always write the voltage gain of the input stage to be $A_{v,input} = g_{m,input}R_{Leq}$ where $g_{m,input}$ is some number $\{g_{m1}, A_{v3}g_{m1}, \text{ and } A_{v3}/(R + 1/g_{m1})\}$ in the 3 examples above}.





The third stage, the output stage, is almost always some kind of compound emitter follower stage, or source follower stage. A few are illustrated above. Note that you are required to use an MOS output stage. Note that the high threshold voltage of MOSFETs makes the designs above incapable of producing signal swings close to the power supplies. Better MOSFET output stages are quite complex (see the text by Jaeger). In general, the output stage simply has some voltage gain slightly less than, unity, which we will call $A_{v,output}$



In between these two stages is a voltage-gain stage, usually a common-emitter stage with perhaps an emitter-follower buffer and/or a cascode connection. One can find its gain at low frequencies by the usual methods. This stage, however, almost always has a compensation capacitor connected between its input and output, as shown. Skipping the

analysis (you can ask me...), the overall differential gain of the op-amp, at higher frequencies is given by:

$$A_d(f) \cong \frac{g_{m,\text{input}}}{j2\pi fC} A_{v,\text{output}}$$

So, in you lab design, choose C such that the differential gain has a magnitude of 1 at a frequency somewhere between 1 and 2 MHz.

Measuring the gain and CMRR of op-amps

This is covered in the document op_amp_comments.pdf.