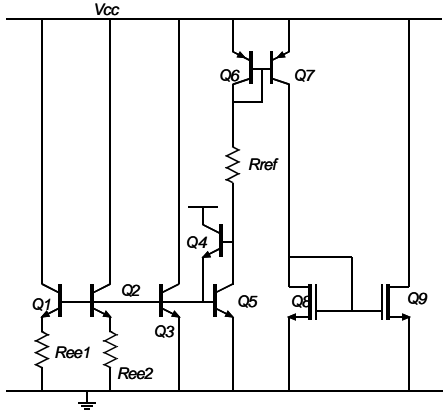
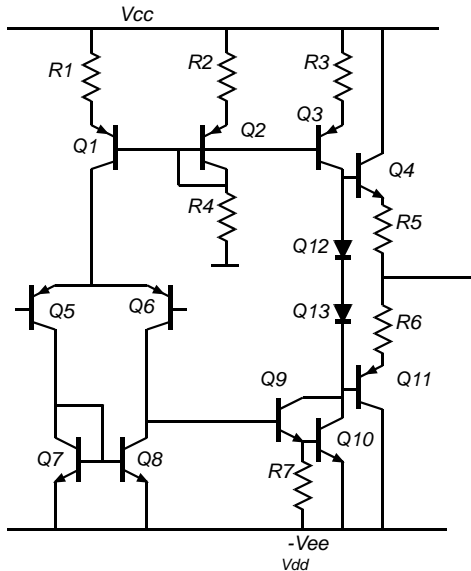


ECE137A Problem set 7

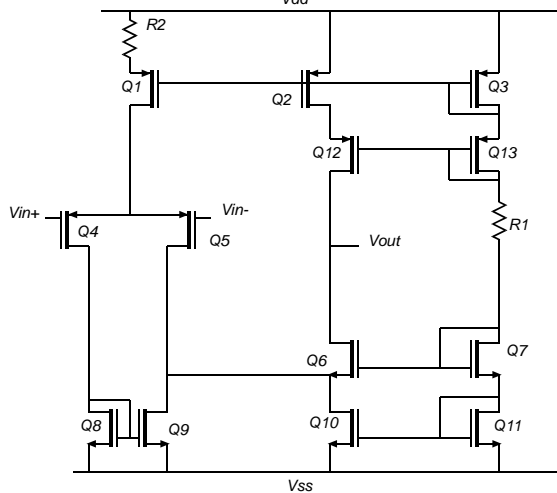


Problem 1:

$I_{s6} = 2I_{s7}$.
 $I_{s5} = I_{s4}/3 = I_{s3}/4 = I_{s2} = 3I_{s1}$.
 V_{cc} is 10 volts.
 NPNs have $\beta = 200$. PNP's have $\beta = 10$.
 $V_a = \infty$. The MOSFETs have a 0.3 V threshold, $v_{sat} C_{ox} W_g = 2 \text{ mA/V}$ (use constant-velocity model), and $\lambda = 1/100 \text{ volts}$.
 Find R_{ref} so that $I_{c5} = 1 \text{ mA}$. Find R_{ee2} so that $I_{c2} = 0.1 \text{ mA}$. $R_{ee1} = 1 \text{ k}\Omega$. Find the collector and drain currents of all transistors

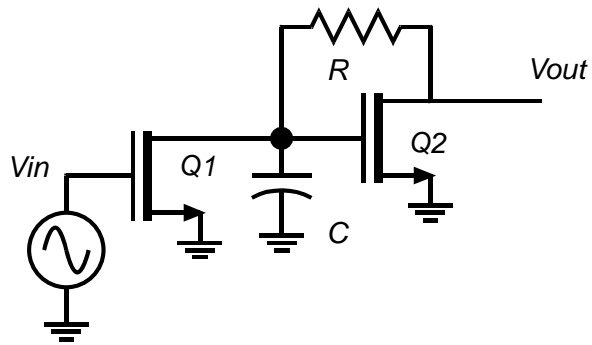


Problem 2: All transistors have $\beta = 200$ and $V_a = 100 \text{ V}$. The supplies are $\pm 5 \text{ V}$. This is an op-amp...it has to be biased using a feedback network: bias conditions have to be worked assuming that the differential input voltage is whatever is required to make $V_{out} = 0 \text{ volts DC}$. Q12 and Q13 are diode-connected transistors. R2 is to have 300 mV DC voltage drop. $I_{c1} = 100 \text{ uA}$. $I_{c9} = 200 \text{ uA}$. $I_{c10} = 2 \text{ mA}$. $I_{c2} = 0.5 \text{ mA}$. $I_{c4} = I_{c11} = 1 \text{ mA}$. Find all resistor values and all collector currents. Find the DC input voltage necessary to obtain $V_{out} = 0 \text{ volts}$. Given a 5k Ω load, find the differential voltage gain, the CMRR and the max. peak-peak signal swing. Inputs are biased at $\sim 0 \text{V DC}$



Problem 3: This, again, is an op-amp. The NMOS FETs have 1.2 nm oxide thickness, 250 nm gate length, and a 0.4 V threshold. Mobility is $400 \text{ cm}^2/(\text{V}\cdot\text{s})$, and $1/\lambda = 25 \text{ V}$. The PMOS FETs are the same, except have -0.4 V threshold and $200 \text{ cm}^2/(\text{V}\cdot\text{s})$ mobility.

Ignore the effects of λ in DC analysis but not in AC analysis. Q4,5 are to be biased at 50 uA each, and Q2 and Q3 at 100 uA. The FET widths are all selected so that the V_{gs} of all has a magnitude of 0.6 Volts, **except** for Q1, which has the same width as Q2. The DC inputs are at zero volts. (a) find all FET widths, resistor values and all DC bias currents and voltages. b) Given an INFINITE load resistance, find the



differential voltage gain, the CMRR and the max. peak-peak signal swing. Inputs are biased at $\sim 0V$ DC

Problem 4: Nodal Analysis exercise: a transconductance-transimpedance amplifier. Ignore DC bias analysis. You don't need it. The two transistors have transconductance g_{m1} and g_{m2} respectively. Their output resistances R_{ds1} and R_{ds2} are both infinity. The capacitor C has value = zero Farads. (a) Find, by nodal analysis, a small-signal expression for V_{out}/V_{in} . (b) $G_{m1} = 20$ mS. $G_{m2} = 10$ mS. $R = 1k\Omega$. Again find V_{out}/V_{in} .