Final Exam, ECE 137A

Wednesday March 18, 2015  7:30-10:30 PM

Name: __________________________

Closed Book Exam: Class Crib-Sheet and 3 pages (6 surfaces) of student notes permitted
Do not open this exam until instructed to do so. Use any and all reasonable
approximations (5% accuracy), after stating & justifying them.

Show your work:
Full credit will not be given for correct answers if supporting work is missing.

Good luck

<table>
<thead>
<tr>
<th>Time function</th>
<th>LaPlace Transform</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\delta(t)$</td>
<td>impulse</td>
</tr>
<tr>
<td>$U(t)$</td>
<td>unit step-function</td>
</tr>
<tr>
<td>$e^{-\alpha}U(t)$</td>
<td></td>
</tr>
<tr>
<td>$e^{-\alpha}\cos(\omega_d t)U(t)$</td>
<td></td>
</tr>
<tr>
<td>$e^{-\alpha}\sin(\omega_d t)U(t)$</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Part</th>
<th>Points Received</th>
<th>Points Possible</th>
<th>Part</th>
<th>Points Received</th>
<th>Points Possible</th>
</tr>
</thead>
<tbody>
<tr>
<td>1a</td>
<td>5</td>
<td>5</td>
<td>2c</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>1b</td>
<td>6</td>
<td>6</td>
<td>2d</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>1c</td>
<td>4</td>
<td>4</td>
<td>3a</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>1d</td>
<td>10</td>
<td>10</td>
<td>3b</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>1e</td>
<td>10</td>
<td>10</td>
<td>3c</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>2a</td>
<td>10</td>
<td>10</td>
<td>3d</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>2b</td>
<td>10</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>total</td>
<td>100</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Problem 1, 35 points

This is an NOT an Op-Amp: Analyze under the assumption that the differential and common mode input voltages are at zero volts.

All the transistors have the same (matched) \( I_s \), have \( \beta = 250 \), and \( V_A = \infty \) Volts.

\( V_{CE(sat)} = 0.5 \text{V} \). \( V_{be} \) is roughly 0.7 V, but use \( V_{be} = (kT/q) \ln(I_E/I_s) \) when necessary and appropriate. The supplies are +2.5 Volts and -2 Volts.

Q1ab,2ab,4a,5a,6a are to be biased at 100 \( \mu \text{A} \) collector current.
Q4B,5B,6B are to be biased at 2 mA collector current.
Q8ab are to be biased at 500 \( \mu \text{A} \) collector current.
Q9ab are to be biased at 125 \( \mu \text{A} \) collector current.

\( R_L = 250\Omega \) R1a=R1b=500 Ohms
Part a, 5 points
DC bias---to simplify, assume $\beta = \infty$ for the DC analysis only.

On the circuit diagram above, label the DC voltages at ALL nodes, the DC currents through ALL resistors, and the DC collector currents of all transistors.
Part b. 6 points
DC bias:

Find the value of all resistors.
R3=____ R4a=____ R6a=____ Rref=____ R8a=____ R8b=____
R9a=____ R9b=____
Part c, 4 points

Find the transconductance of the transistors below:
\[ \text{gm1a=} \quad \text{gm1b=} \quad \text{gm5a=} \quad \text{gm7a=} \]
\[ \text{gm7b=} \quad \text{gm9a=} \quad \text{gm9b=} \]
Part d, 10 points.

Find the following, using the actual value of \( \beta \), i.e. \( \beta = 250 \)

<table>
<thead>
<tr>
<th>Transistor combination</th>
<th>Voltage Gain</th>
<th>Input impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q2a,2b,1a,1b</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q5a</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q7a or 7b</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q9a or 9b</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall differential</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vout/Vin</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Part e, 10 points

Maximum peak-peak output voltage \((\text{show all your work})\)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>magnitude and sign of maximum output signal swing due to \textit{cutoff}</th>
<th>magnitude and sign of maximum output signal swing due to \textit{saturation}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor Q4a</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor Q5a</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor Q7a</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor Q7b</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor Q9a</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor Q9b</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Be warned: In some cases a limit is not relevant at all. Mark those answers "not relevant". But, give a 1-sentence statement below as to why it is not relevant. Q7ab and Qab form a push pull stage, so be careful about your answers here.
Problem 2, 35 points

This is an Op-Amp---analyze the bias under the assumption that DC output voltage is zero volts, that the positive input \( V_{i+} \) is zero volts, and that we must determine the DC value of the negative input voltage \( (V_{i-}) \) necessary to obtain this.

The NMOSFETs and the PMOSFETS have a 0.20 V threshold, a 22nm gate length, 300 cm\(^2\)/Vs mobility, a 10\(^7\) cm/s saturation drift velocity, and \( 1/\lambda = 3 \) Volts. The gate oxide thickness is 1.0nm and the dielectric constant is 3.8. This gives

\[
\mu c_{ox} W_g / 2L_g = 15 \text{ mA/V}^2 \cdot (W_g / 1 \mu \text{m}) \quad \text{and} \quad v_{sat} c_{ox} W_g = 3.36 \text{ mA/V} \cdot (W_g / 1 \mu \text{m})
\]

(both are a bit unrealistic for a real technology).

and \( v_{sat} L_g / \mu = 0.113 \text{ V} \)

\[ V_{DD} = +0.75 \text{ V}, \quad -V_{SS} = -0.75 \text{ V}, \]
Part a, 10 points
DC bias.

**Approximation: ignore the term** \((1 + \lambda V_{DS})\) **in DC bias analysis.**

Analyze the bias under the assumption that DC output voltage is zero volts, that the positive input \(V_{i+}\) is zero volts, and that we must determine the DC value of the negative input voltage \(V_{i-}\) necessary to obtain this.

Q1ab,2ab are to be biased at 25 \(\mu\text{A}\) drain current.
Q4ab,5ab,6ab,7ab are to be biased at 100 \(\mu\text{A}\) drain current.
All transistors are to operate with \(|V_{gs}| = 0.25\text{V}\).

Find the gate widths of all transistors.

Find:
\[
\begin{align*}
W_{g1a} &= \quad \quad W_{g1b} = \quad \quad W_{g2a} = \quad \quad W_{g2b} = \quad \quad W_{g3} = \quad \\
W_{g4a} &= \quad \quad W_{g4b} = \quad \quad W_{g5a} = \quad \quad W_{g5b} = \quad \\
W_{g6a} &= \quad \quad W_{g6b} = \quad \quad W_{g7a} = \quad \quad W_{g7b} = \quad \\
R_{\text{ref}} &= \quad 
\end{align*}
\]
Part b, 10 points

DC bias

On the circuit diagram above, label the DC voltages at ALL nodes the drain currents of ALL transistors, and the gate widths of ALL transistors.
Part c, 15 points.

You will now compute the op-amp differential gain. You must consider the \((1 + \lambda V_{DS})\) term in the FET IV characteristics when you do this.

The capacitors C1-C4 are all zero Ohms AC impedance. (They would not be present in a real design; they are added here to simplify the exam).

Find the following

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(Alternative----if you very skilled, you might be able to compute the combined gain of Q2a,2b,1a,1b and Q5a, all together, in a single step using Norton or Thevenin methods. If you do so, first, don't ask for hints on how to do this and, second, do please also calculate the input impedance of Q5a. )
Part d, 10 points

Maximum peak-peak output voltage at the positive output Vo+ (*show all your work*)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>magnitude and sign of maximum output signal swing due to <em>cutoff</em></th>
<th>magnitude and sign of maximum output signal swing due to:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor Q5a</td>
<td></td>
<td><em>knee voltage</em> (saturation)</td>
</tr>
<tr>
<td>Transistor Q6a</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor Q2a</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transistor Q2b</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Be warned: in some cases a limit is not relevant. Mark those answers "not relevant". But, give a 1-sentence statement why below.
Problem 3, 30 points

You will be working on the circuit to the left. Ignore DC bias analysis. You don’t need it.

The transistor has transconductance \(g_m\). Its output resistance \(R_{ds}\) is infinity, so you don't need to include this element in the circuit diagram!

Part a, 7 points

Draw a small-signal equivalent circuit of the circuit.
Part b, 8 points

gm=10 mS. L=1 \mu H. R= 1000 Ohms

Find, by nodal analysis, a small-signal expression for Vout/Vin. Be sure to give the answer with **correct units** and in ratio-of-polynomials form, i.e.

\[
\frac{V_{out}(s)}{V_{gen}(s)} = K \cdot \frac{1 + b_1s + b_2s^2 + ...}{1 + a_1s + a_2s^2 + ...} \quad \text{or (as appropriate)} \quad \frac{V_{out}(s)}{V_{gen}(s)} = K \cdot (s \tau)^n \cdot \frac{1 + b_1s + b_2s^2 + ...}{1 + a_1s + a_2s^2 + ...}
\]

Note that an expression like

\[
\frac{V_{out}(s)}{V_{gen}(s)} = \frac{1}{1 + (3 \cdot 10^{-6})s}
\]

is dimensionally wrong; \[
\frac{1}{1 + (3 \cdot 10^{-6} \text{seconds})s}
\]

is dimensionally correct

Vout(s)/Vin(s) = __________________
Part c, 7 points

Find any/all pole and zero frequencies of the transfer function, in Hz:

__________________________

Draw a clean Bode Plot of Vout/Vin,
LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes
Part d, 8 points

Vin(t) is a 0.1 V amplitude step-function.

Find Vout(t)=___________________________

Plot it below. Label axes, show initial and final values, show time constants.