Final Exam, ECE 137A

Wednesday March 20, 2019, Noon - 3 p.m.

Name: _____

Closed Book Exam:
Class Crib-Sheet and 2 pages (4 surfaces) of student notes permitted
Do not open this exam until instructed to do so. Use any and all reasonable
approximations (5% accuracy), *after stating & justifying them*.
Show your work:
*Full credit will not be given for correct answers if supporting work is missing.*
Good luck

Time function	LaPlace Transform
$\delta(t)$ impulse	1
$U(t)$ unit step-function	$1/s$
$e^{-\alpha t}U(t)$	$\dfrac{1}{s+\alpha} = \dfrac{1/\alpha}{1+s/\alpha}$
$e^{-\alpha t}\cos(\omega_d t)U(t)$	$\dfrac{s+\alpha}{(s+\alpha)^2 + \omega_d^2}$
$e^{-\alpha t}\sin(\omega_d t)U(t)$	$\dfrac{\omega_d}{(s+\alpha)^2 + \omega_d^2}$

Part	Points Received	Points Possible	Part	Points Received	Points Possible
1a		6	2c		15
1b		5	2d		10
1c		4	3a		7
1d		10	3b		8
1e		10	3c		7
2a		10	3d		8
2b		10			
total		100			

a

Problem 1, 35 points

This is an NOT an Op-Amp: Analyze under the assumption that the differential and common mode input voltages are at zero volts
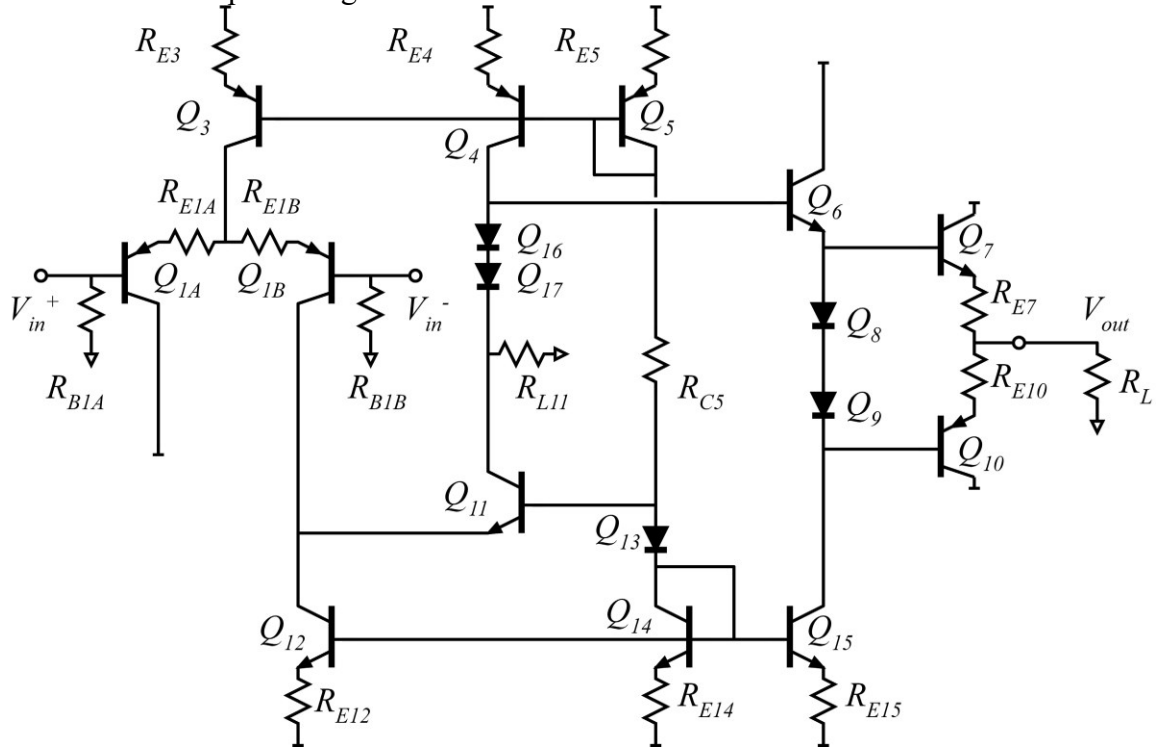
All the transistors have the same (matched) I_S, have $\beta = 100$, and $V_A = \infty$ Volts.

$V_{CE(sat)} = 0.5\text{V}$.

V_{be} is approximately 0.7 V,

but use $V_{be} = (kT/q)\ln(I_E/I_S)$ when necessary or appropriate.

The supplies are +4 Volts and -4 Volts.

All transistors (and diodes) have the same I_S

Q1A,1B,5,11 are biased at 10mA collector current.

Q6 is biased at 25mA collector current.

Q7 and Q10 are biased at 3mA collector current.

The DC voltage drops across RE5 and RE14 are both 400mV.

RB1A=RB1B=2kOhm. RE1A=RE1B=44.8Ohm. RL11=1.1kOhm.

RL=1kOhm.

Part a, 6 points

DC bias---to simplify ,assume $\beta = \infty$ *for the DC analysis only.*

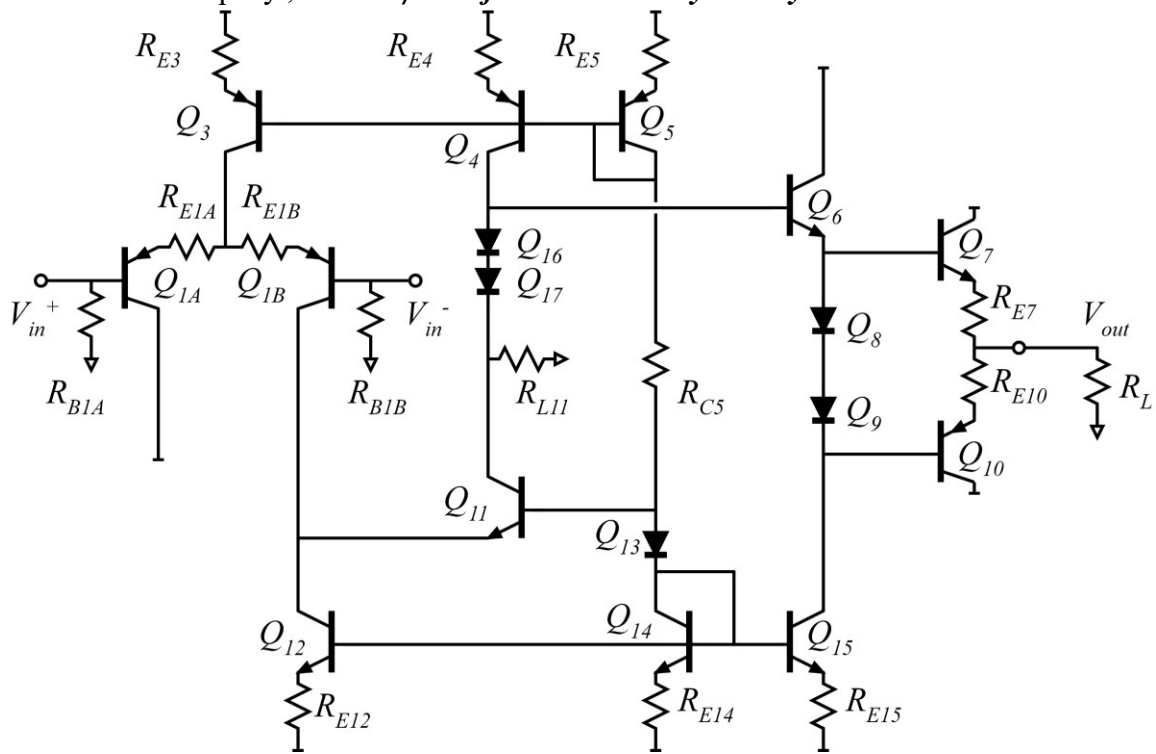Find the value of the following resistors:

Re5=_____   Re14=_____   Re4=_____

Re15=_____   Re12=_____   Re3=_____

Re7=_____   Re10=_____

a

Part b, 5 points

DC bias---to simplify ,assume $\beta = \infty$ *for the DC analysis only.*

On the circuit diagram above, label the DC voltages at **ALL nodes**, and the DC collector currents of **all transistors**. Label the values of all resistors (except RC5).

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Part c, 4 points

find the following

device	Q1AB	11	12	4	6	15	7	10
gm, mS								

Part d, 10 points.

Find the following, ***using the actual value of*** β ***, i.e.*** β***=100***

	Voltage Gain	Input impedance
Q1AB		
Q11		
Q6		
Q7		
Overall differential Vout/Vin		

Note: with some insight, you can find the combined gain of Q1AB/11 in a single step. If would would like to do so, omit the separate answers for Q1AB and Q11 in the table above, and instead fill in the table below,

	Voltage Gain	Input impedance
Q1AB/ Q11 combination.		

a

9

a

11

a

Part e, 10 points

Maximum peak-peak output voltage (***show all your work***)
For this, you must use the full circuit diagram, not the half circuit diagram.

|	magnitude and sign of maximum output signal swing due to *cutoff*	magnitude and sign of maximum output signal swing due to *saturation*
Transistor Q7		
Transistor Q10		
Transistor Q6		
Transistor Q15		
Transistor Q4		
Transistor Q11		
Transistor Q1A		
Transistor Q1B		

Be warned: In some cases a limit is not relevant at all. Mark those answers "not relevant".
But, give a 1-sentence statement below as to why it is not relevant. Q7/10 form a push
pull stage, so be careful about your answer there. .

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a

a

Problem 2, 35 points

This is an Op-Amp---analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.
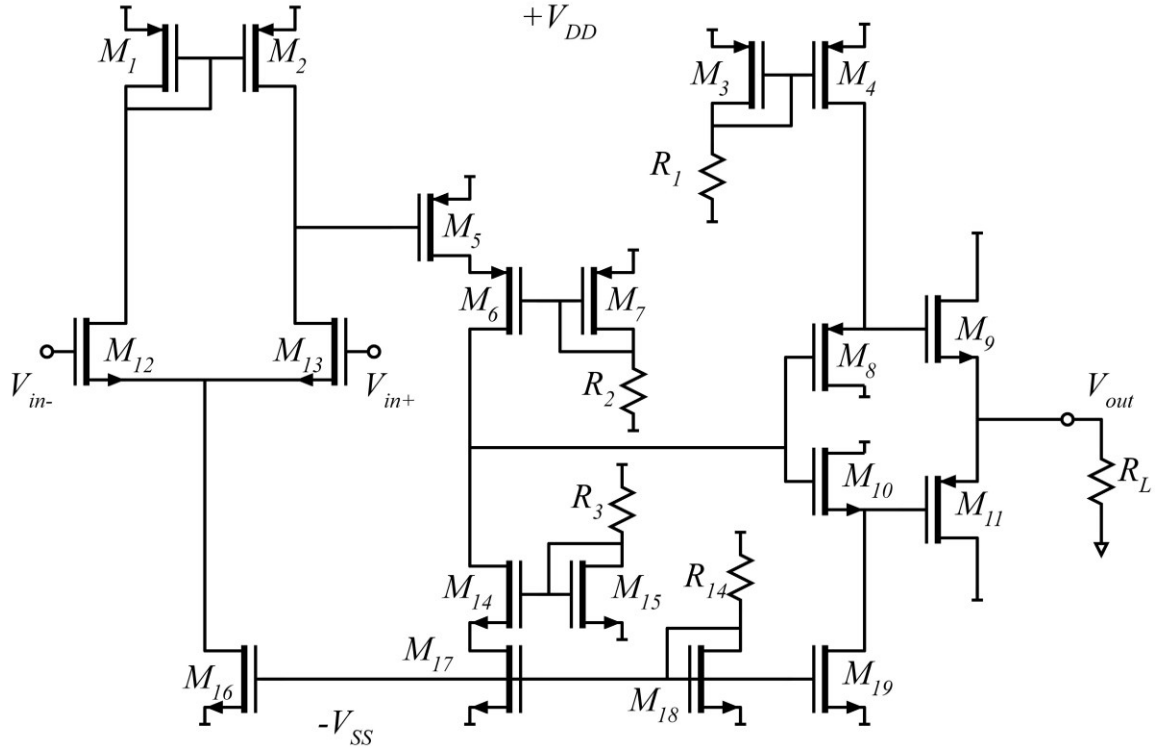
The NMOSFETs have $K_\mu = \mu c_{gs} W_g / 2L_g = 0.55 \text{mA/V}^2 \cdot (W_g / 1\mu m)$

$K_v = c_{gs} v_{inj} W_g = 0.69 \text{mA/V} \cdot (W_g / 1\mu m)$, $\Delta V = v_{inj} L_g / \mu = 0.625 \text{V}$, $V_{th} = 0.25 \text{V}$,

$1/\lambda = 20 \text{V}$

The PMOS have identical parameters, except, of course, V_{th} is negative.

$V_{DD} = +1$ V, $-V_{SS} = -1$ V, $R_L = 50$ kOhm

All transistors have |Vgs|=0.35V, ***except for M7 and M15***, which have |Vgs|=0.45V, ***and except for M8,9,10,11***, which have |Vgs|=0.30V

M12,13 are biased at $I_D = 25$ µA.

M5,7,15 are biased at $I_D = 50$ µA.

M8,9,10,11 are biased at $I_D = 50$ µA.

Part a, 10 points
DC bias.
Analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.
(Hint, this should give Vi- = 0V)

Find the following:
Gate widths of M12 and M13 = _____
Gate width of M7 =_____
Gate width of M8 =_____
Gate width of M9 =_____

a

a

Part b, 10 points

DC bias

On the circuit diagram above, label the DC voltages at **ALL nodes,** the drain currents of **ALL transistors,** and the gate widths of **ALL transistors**

a

Part c, 15 points.

You will now compute the op-amp differential gain. Find the following

	Voltage Gain	Input impedance
Transistor combination M1,2,13, 13		
M5,6 combination		
Q9 or Q12.		
Q8 or Q15		
Overall differential Vout/Vin		

Notes:

1) You can analye M5 and M6 as separate stages, or as a combined stage using Norton/Thevenin methods. Don't ask for hints as to how to do this.

2) For M8/9and for M10/11, you can assume that M8 and M9 are on for the positive signal swing and M10 and M11 are on for the negative signal swing. More accurately, you can assume, for the signal swing near zero volts, that all are on. If you take the latter approach (and do it correctly), you will receive a couple of extra credit points. One hint (don't ask for any other hints): use symmetry.

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a

a

Part d, 10 points

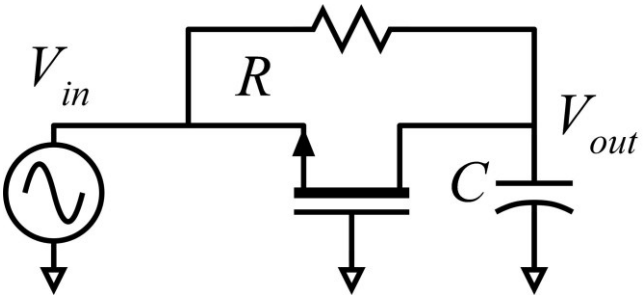Maximum peak-peak output voltage at the positive output Vo+ (***show all your work***)

	magnitude and sign of maximum output signal swing due to *cutoff*	magnitude and sign of maximum output signal swing due to: *knee voltage* (saturation)
Transistor M9		
Transistor M11		
Transistor M8		
Transistor M10		
Transistor M4		
Transistor M19		
Transistor M6		
Transistor M14		

Be warned: in some cases a limit is not relevant. Mark those answers "not relevant".

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Problem 3, 30 points

You will be working on the circuit to the left

Ignore DC bias analysis. You don't need it.

The transistor has transconductance gm.

Its output resistance Rds is infinity...so you don't need to include this element in the circuit diagram !

<u>Part a, 7 points</u>

Draw a small-signal equivalent circuit of the circuit.

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<u>Part b, 8 points</u>

gm=10 mS. C=1pF. R= 1000 Ohms
Find, by nodal analysis, a small-signal expression for Vout/Vin. Be sure to give the
answer with **correct units** and in ratio-of-polynomials form, i.e.

$$\frac{V_{out}(s)}{V_{gen}(s)} = K \cdot \frac{1 + b_1 s + b_2 s^2 + ...}{1 + a_1 s + a_2 s^2 + ...} \text{ or (as appropriat e) } \frac{V_{out}(s)}{V_{gen}(s)} = K \cdot (s\tau)^n \cdot \frac{1 + b_1 s + b_2 s^2 + ...}{1 + a_1 s + a_2 s^2 + ...}$$

Note that an expression like

$$\frac{V_{out}(s)}{V_{gen}(s)} = \frac{1}{1 + (3 \cdot 10^{-6})s} \text{ is dimensiona lly wrong; } \frac{1}{1 + (3 \cdot 10^{-6} \text{ seconds })s} \text{ is dimensiona lly correct}$$

Vout(s)/Vin(s)= _____

a

a
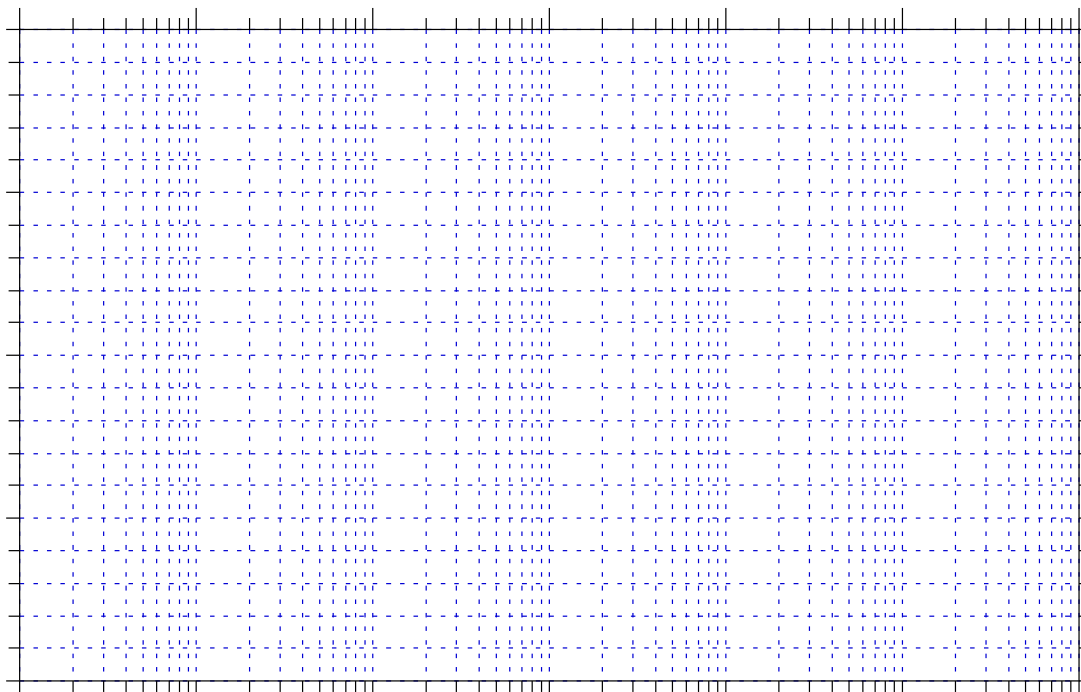
Part c, 7 points

Find any/all pole and zero frequencies of the transfer function, in Hz:

_____,_____,_____,_____

Draw a clean Bode Plot of Vout/Vin,
LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes

a

a

Part d, 8 points

Vin(t) is a 0.1 V amplitude step-function.

Find Vout(t)=_____

Plot it below. Label axes, show initial and final values, show time constants.