ECE137A Notes Set 12: IC process flows, Current mirror biasing, IC design

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MOS process flow

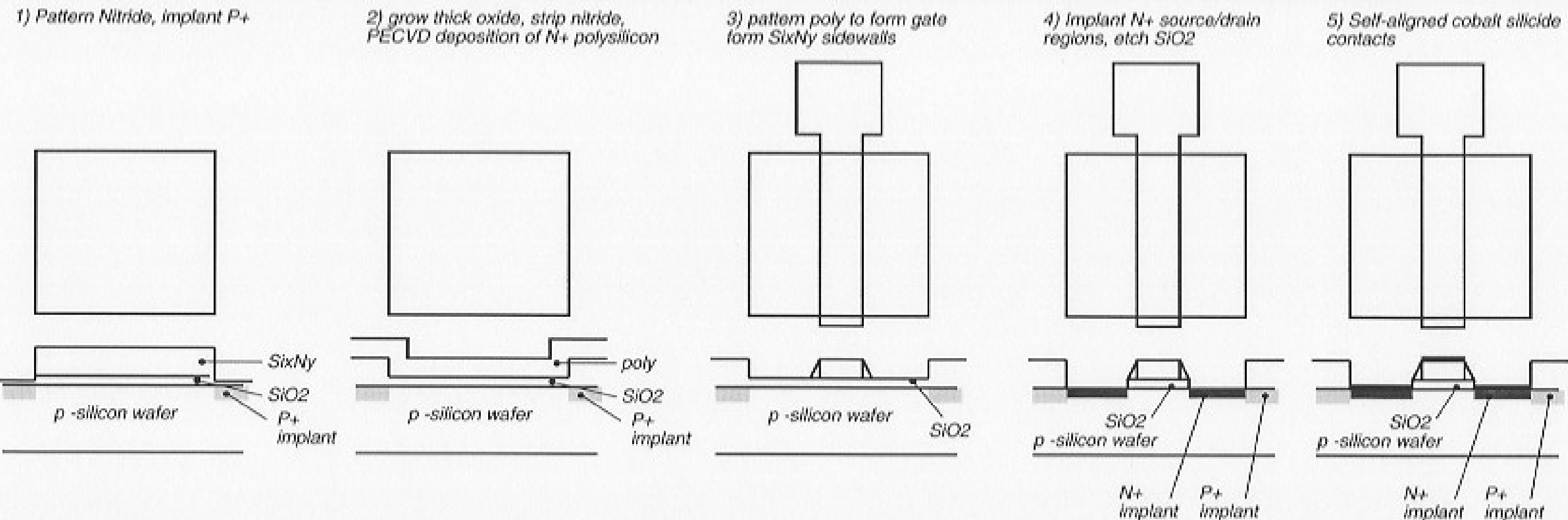
1) Pattern Nitride, implant P+

2) grow thick oxide, strip nitride, PECVD deposition of N+ polysilicon

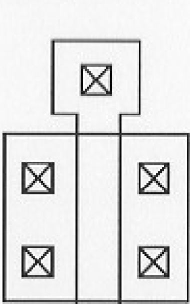
3) pattern poly to form gate form SixNy sidewalls

4) Implant N+ source/drain regions, etch SiO2

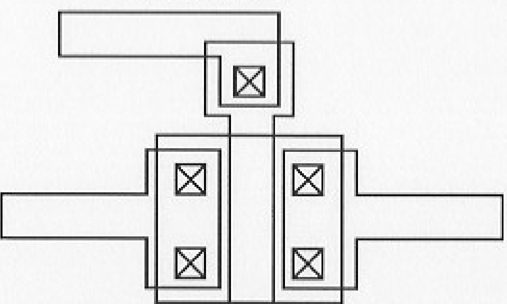
5) Self-aligned cobalt silicide contacts

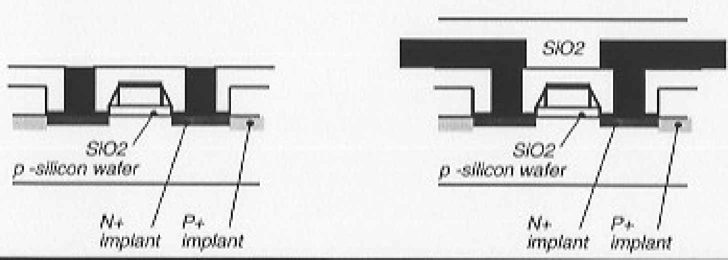


6) Coat with SiO2, form open holes, form W vias

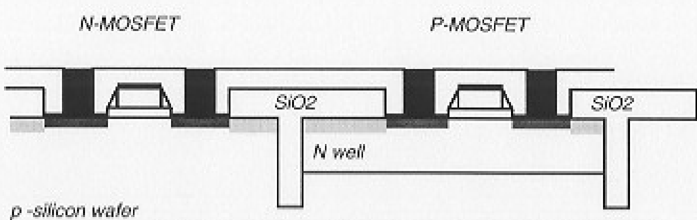


7) aluminum interconnects and dielectric insulators

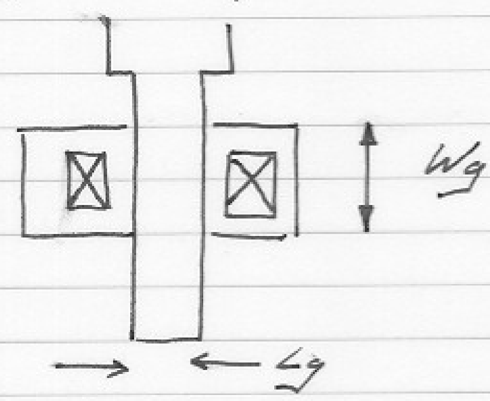




CMOS (NMOS + PMOS) process is similar but more complex...

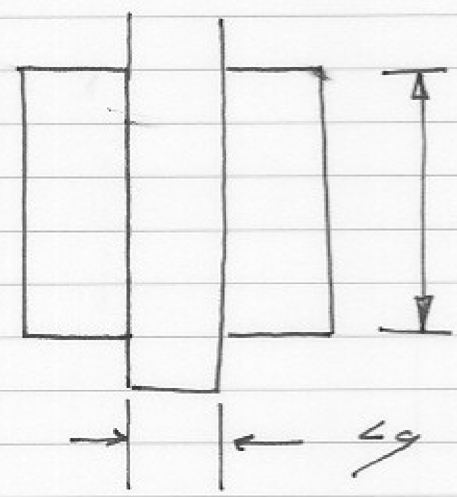


Varying the "size" of a MOSFET



$$I_d = C_{ox} v_{sat} W_g (V_{gs} - V_{th})$$

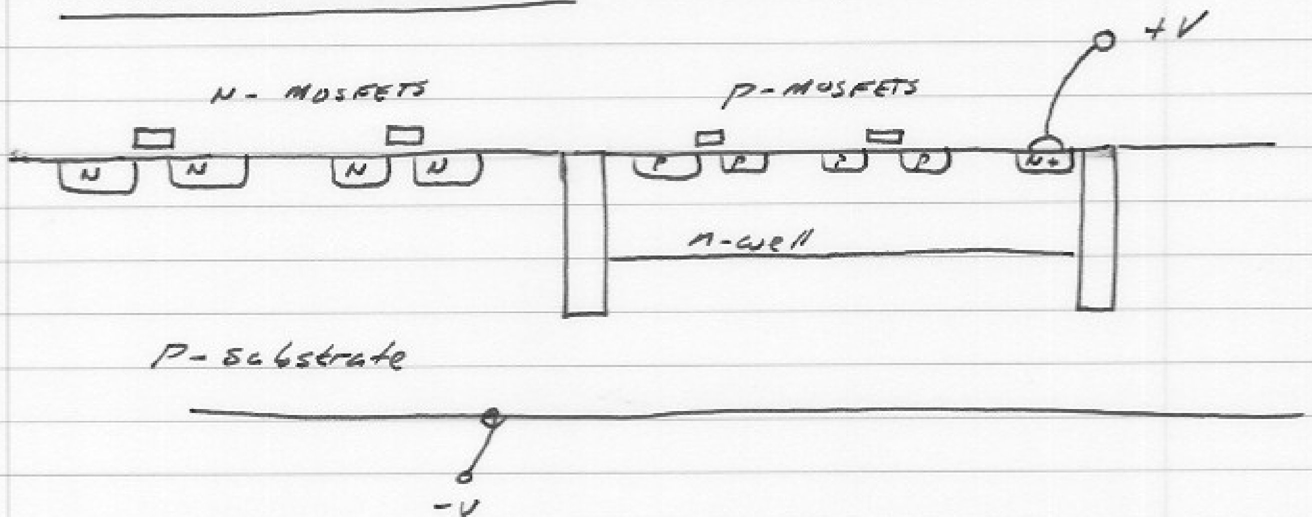
vs



W_g increased

L_g kept constant

Substrate connections - MOSFETS.



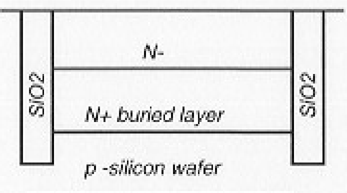
There are P-N junctions from the source & drains of the N-MOSFETS to the P substrate. The P substrate must be connected to the most negative voltage in the circuit

There are N-P junctions from the source and drains of the P-MOSFETS to the N-wells in which they sit. The N wells must be connected to the most positive voltage in the circuit

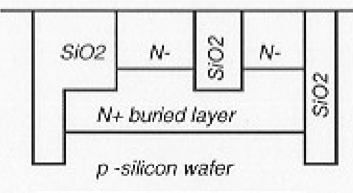
There are depletion capacitances from the wells/substrate to the source/drain regions.

SiGe HBT process flow

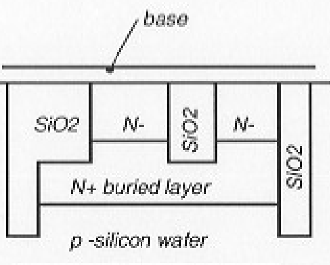
1) P- wafer, form N+ buried layer, form N- collector drift layer, etch isolation trenches, fill with insulator



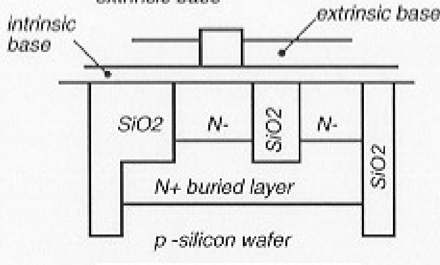
2) etch primary collector pedestal replanarize by Spin-on-glass and chemical-mechanical polishing



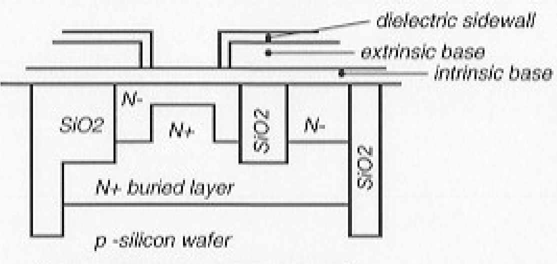
3) grow P SiGe intrinsic base layer



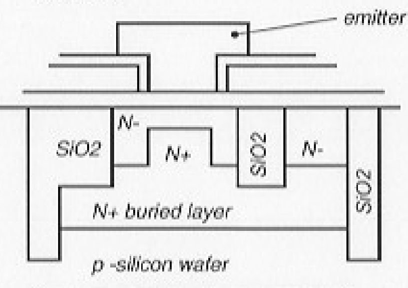
4) deposit Si3N4 dummy emitter, use this to control location of growth of extrinsic base



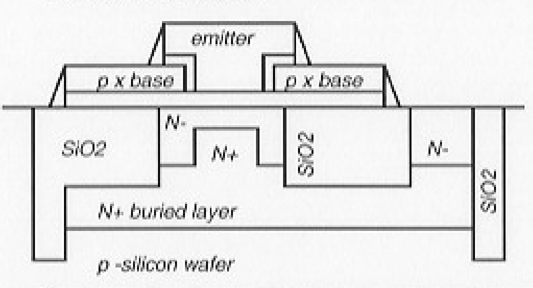
5) remove dummy emitter, form dielectric sidewalls, implant second collector pedestal



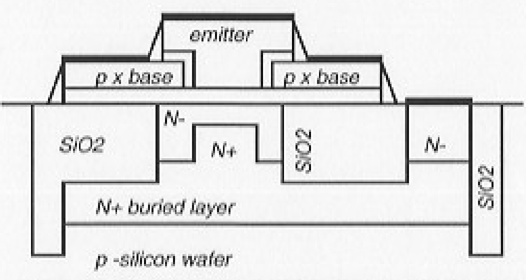
6) grow polysilicon N+ emitter, pattern and etch



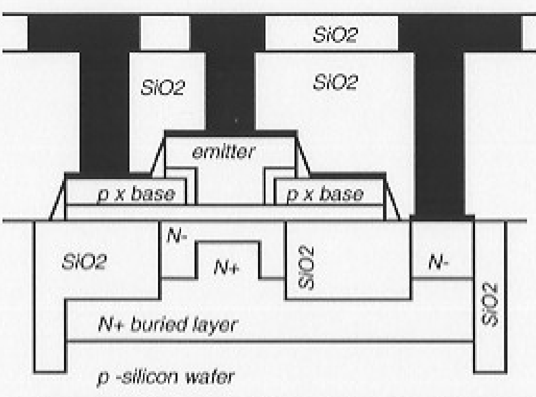
7) etch through dielectric, pattern/etch base, form new dielectric sidewalls



8) form self-aligned cobalt/tungsen silicide contacts



9) interconnect back end (W plugs, Al wiring, SiO2 dielectric)

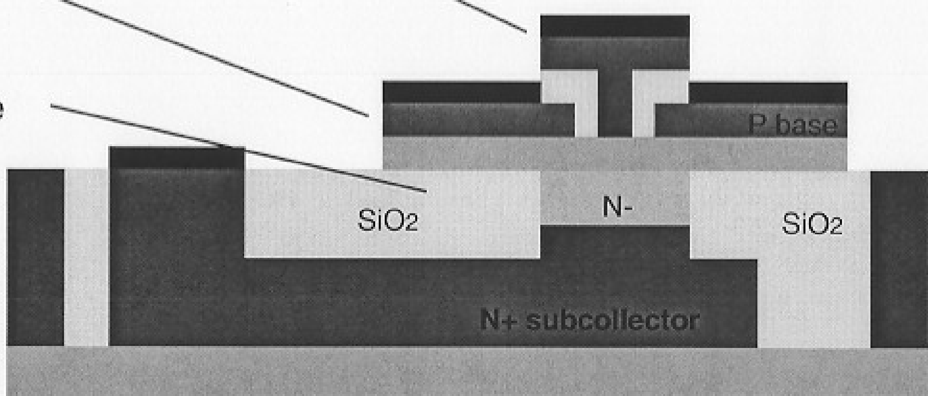


Modern SiGe BJT

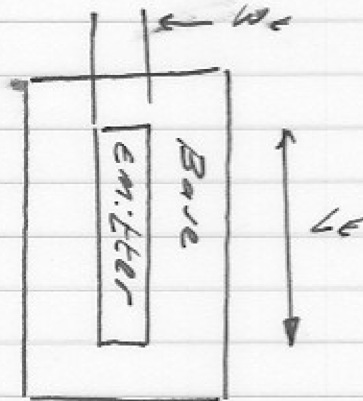
wide emitter contact: low resistance
narrow emitter junction: scaling (low R_{bb}/A_e)

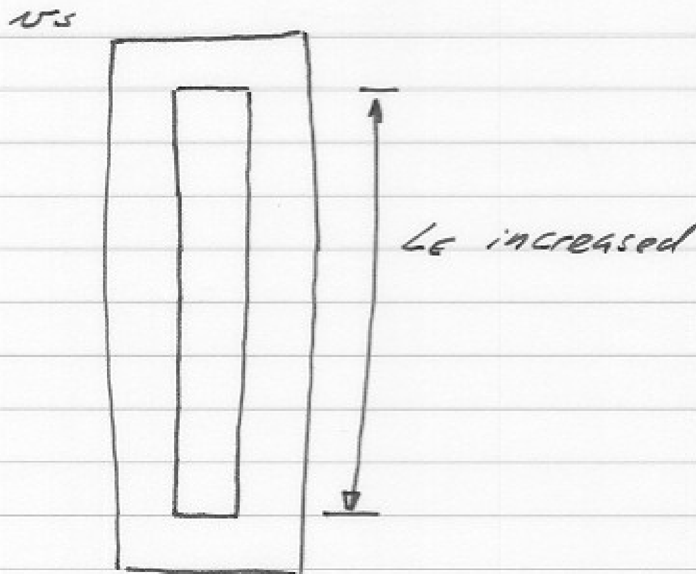
thick extrinsic base : low resistance
thin intrinsic base: low transit time

wide base contacts: low resistance
narrow collector junction: low capacitance

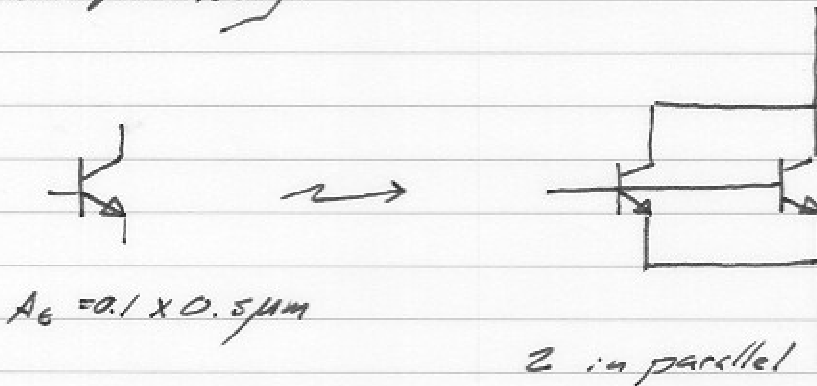


varying the "size" of a bjt:





or, more precisely:

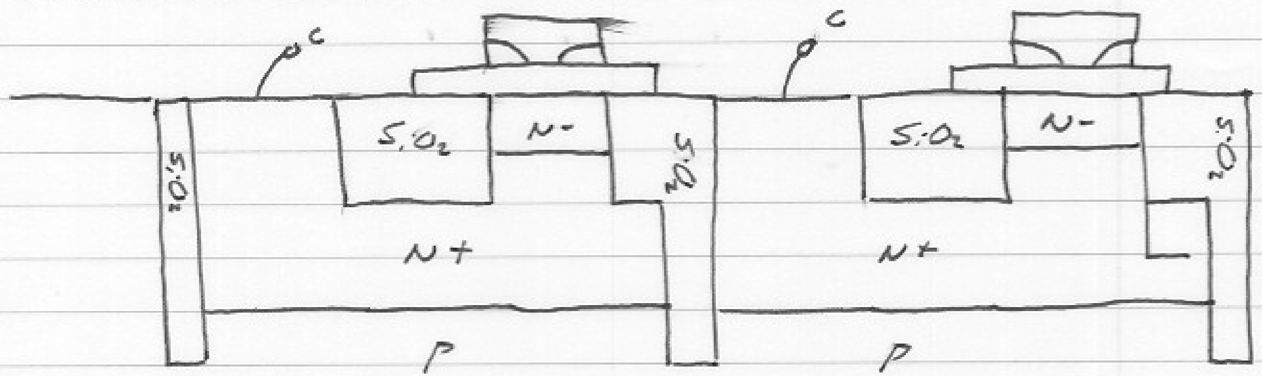


each $A_E = 0.1 \times 0.5 \mu m$

$$I_S = \frac{q n_{po} D_n}{W_B} \cdot A_E \propto A_E$$

varying $A_E \rightarrow$ varies I_S.

Substrate connections: BJTs



There are p-N junctions from each collector to the substrate. The p substrate must be tied to the most negative voltage in the circuit.

There is a depletion capacitance from each collector to the substrate.

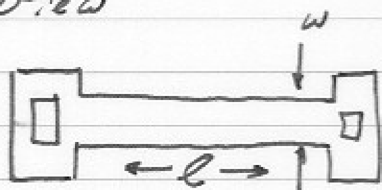
To make resistors:

= These can be made from the gate polysilicon in MOS PROCESSES or the base or emitter polysilicon in bjt processes.

= or, they can be formed from n^+ source diffusions

= or through extra layers of resistive metal such as Ni:cr alloys or w Nitride.

Top view



$R = 2R_{end} + \rho l / wT$

T = thickness
ρ = bulk resistivity.

defining $\rho_{sheet} = \rho / T$ = "# Ω per square"
= sheet resistivity

$R = 2R_{end} + \rho_{sheet} \cdot l / w$

Resistors made from semiconductor layers

- vary with temperature considerably
- have poor absolute tolerance

(doping & thickness & linewidth variations)

Identical-geometry resistors placed close together will have matching of a few %

sheet resistivities are in the range of 10-100 Ω/□

The 10Ω value is typical of thicker, heavily doped layers. Large resistance values therefore require very large L/W ratios, and consume large IC areas.

On a bipolar IC

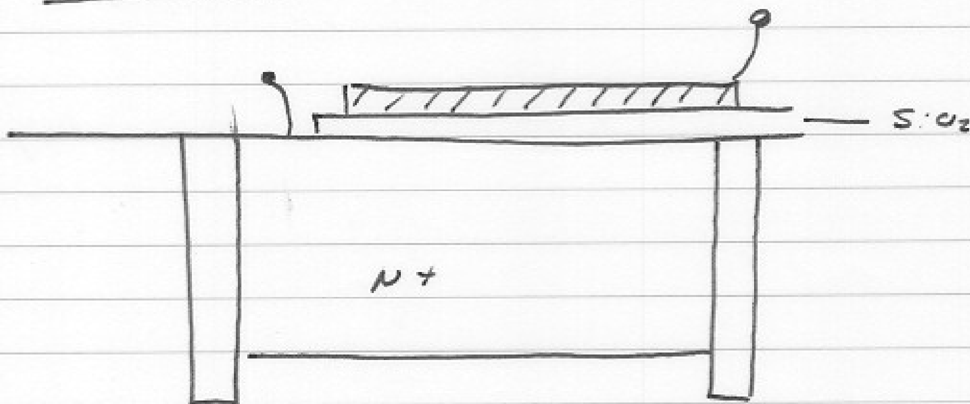
- transistors are small & cheap.
- transistors of identical A_E will have similar I_s
- Transistors obey $I = I_s \exp(qV_{be}/kT)$
  - exploit this to control currents!
- Resistors formed from silicon layers
  - are not high in absolute precision
  - are somewhat better, but not great, in matching
  - have parasitic capacitance to substrate

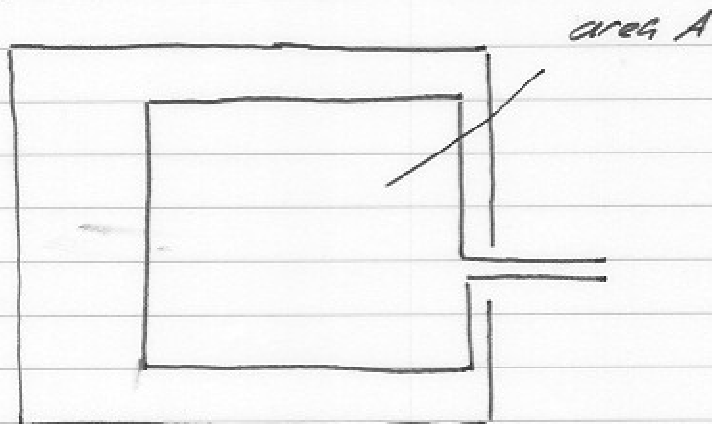
Resistors formed from thin metal films

- can be added at added cost
- are more precise → ADC processes etc
- low sheet resistance → low values only.

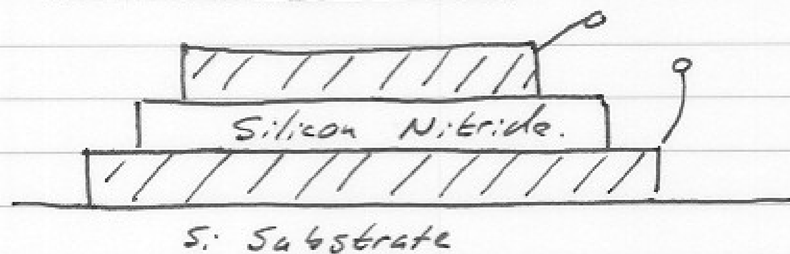
Capacitors of more than a few pF are very large and therefore very expensive

Capacitors:





or:



SiO_2: $\epsilon_r = 3.8$

Si_3N_4: $\epsilon_r = 7.5$

capacitance per unit area.

$$C = \epsilon A/T = (\epsilon_r \epsilon_0 / T) \cdot A$$

$C/A = 0.34\ fF/\mu m^2$ for a 1000Å thick SiO_2 layer

A 1pf capacitor would an area of 55×55µm

A 100pF capacitor would be 550×550 µm

Consequences: IC design

In most analog applications, resistors and capacitor use should be minimized. Biasing is therefore DC coupled and bias currents supplied by current mirrors

In Radio-Frequency IC designs, inductors and capacitors and resistors are key components determining IC performance. In these ICs, passive element quality is key, and IC density is constrained by the large size of those elements.

Conculsions : IC design

" transistors are small = cheap

" ~~bjts~~ bits of identical size will match well in V_{be} but not β.

" MOSFETS of identical size will match reasonably in $v_{sat} C_{ox} W_g$ and V_{th}

But

Resistor absolute precision is poor

Resistor matching is reasonable

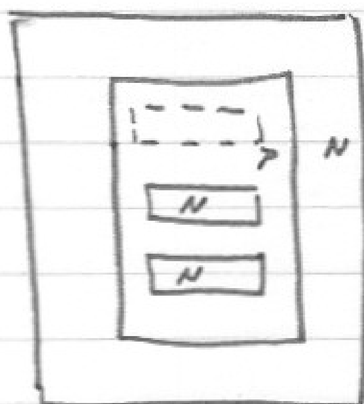
Large resistor values are large area = very expensive

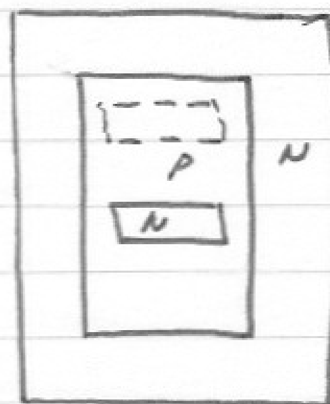
=> Avoid using large resistors whenever possible

Capacitors above 1pF are very large and very expensive

Ratios in current mirrors

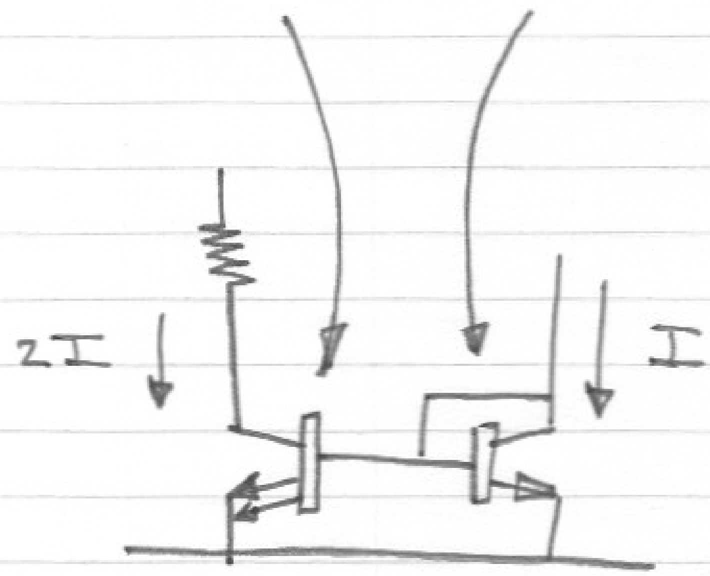
(top views)





transistor with emitter area = $2A_E$

transistor with emitter area = A_E



Notation: