Goals of this note set:

Rough physical sense of FET operation

FET current - voltage characteristics.

Rough mathematical models of MOSFETs
    old - fashioned mobility - limited model.
    slightly less old fashioned velocity - limited model
N-Channel MOSFET
Field-Effect Transistor Operation

Positive Gate Voltage → reduced energy barrier → increased drain current
Field-Effect Transistor Operation

Positive Gate Voltage
→ reduced energy barrier
→ increased drain current
N-Channel MOSFET

Plot common-source characteristic:

- \( V_{gs} \)
- \( V_{ds} \)
- \( I_D \)

Regions:
- Ohmic region
- Constant-current region

\( V_{gs} = V_f \)
Physical Sketch

Diagram showing a MOSFET with labeled parts:
- Source (S)
- Gate (G)
- Drain (D)
- Oxide, dielectric constant
- Thickness of Oxide
- P channel
- N+ regions
- Top view:
  - Gate
  - Electrons
  - Source
  - Drain
  - Width of Gate (Wg)
MOSFET Physical Structure: ~130nm node

Cross-Section

- Gate metal (silicide)
- Dielectric sidewall
- Gate oxide
- N+ poly gate
- Source contact (silicide)
- N+ source
- Drain contact (silicide)
- N+ drain
- P substrate

Layout

(6 FETs, each of gate width $W_g$, connected in parallel)
MOSFET I-V characteristics (approximate)

If we have drain voltages above the knee voltage:

\[ I_D \text{ vs. } V_{DS} \]

- If not at \( V_{GS} \):
  - Increasing \( V_{GS} \)

\[ \text{HERE} \]

\[ \text{HERE} \]
MOSFET I-V characteristics (approximate)

Then we can plot $I_D$ vs. $V_{GS}$:

$$I_d/W_g$$

The **3 regions in the $I_D - V_{GS}$ curve:

1) Subthreshold = almost but not quite off

2) mobility - limited: $I_D \sim (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$

3) velocity - limited: $I_D \sim (V_{gs} - V_{th} - \Delta V / 2)^1 (1 + \lambda V_{DS})$
MOSFETs: Three Regions of Gate Voltage

When $V_{gs}$ is less than threshold, transistor is (almost) off: "subthreshold"

When $V_{gs}$ is a little above threshold, current is mobility – limited

$$I_D \propto (V_{gs} - V_{th})^2$$

When $V_{gs}$ is far above threshold, current is velocity – limited

$$I_D \propto (V_{gs} - V_{th} - \Delta V / 2)$$
MOSFET DC Characteristics: Mobility-Limited Case

mobility-limited current:

\[ I_D \cong (\mu c_{ox} W / 2 L_g)(V_{gs} - V_{th})^2 (1 + \lambda V_{DS}); \text{ this is only approximate} \]

for \( V_{th} < V_{gs} < V_{th} + \Delta V \)

where \( \Delta V \approx L_g V_{sat} / \mu \)

Applies for drain voltages larger than the knee voltage,
MOSFET DC Characteristics: Velocity-Limited Case

velocity – limited current

\[ I_D \approx c_{ox} W_g v_{sat} (1 + \lambda V_{DS})(V_{gs} - V_{th} - \Delta V / 2) \]: this is only approximate

for \( V_{gs} > V_{th} + \Delta V \)

where \( \Delta V \approx L_g v_{sat} / \mu \)

Applies for drain voltages larger than the knee voltage,
DC Characteristics: *Somewhat* Better Approximation

Generalized Expression

\[
\left( \frac{I_D}{I_{D,1}} \right)^2 + \left( \frac{I_D}{I_{D,2}} \right) = 1
\]

\[
I_{D,1} = \left( \mu c_{ox} W_g / 2L_g \right) (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})
\]

\[
I_{D,2} = c_{ox} W_g v_{sat} (1 + \lambda V_{DS}) (V_{gs} - V_{th})
\]

This expression is too complex for us to use in this class:

Instead use **as appropriate** either the velocity - limited or mobility limited expressions.
How well does our approximation work?

Black: actual curve

Our fit: **mobility region** and **velocity region**

Observe: for very large \((V_{gs} - V_{th})\), a better fit would be \(I_D \approx c_{ox} W_g v_{sat} (V_{gs} - V_{th} - \Delta V)\).

This is the dotted line.

No simple expression can fit perfectly at all \(V_{gs}\)!

Our simple (red/blue) model will suffice for this class.
Parameters and Typical #s

\[ \nu_{sat} = \text{saturation drift velocity} \sim 10^7 \text{ cm/s for N-MOSFETs} \]

\[ \mu = \text{carrier mobility at surface} \sim 300 - 400 \text{ cm}^2/(\text{V} \cdot \text{s}) \text{ for N-MOSFET} \]

For P-channel FETs, both \( \nu_{sat} \) and \( \mu \) are about half that of N-FETs

\[ c_{ox} = \text{gate capacitance per unit area} = \epsilon_r \epsilon_0 / T_{ox} \quad (\epsilon_r = 3.8 \text{ for SiO}_2) \]

\[ T_{ox} = \text{equivalent oxide thickness} - \text{about 1 nm} = 10^{-9} \text{ m} \]

\[ V_{th} = \text{threshold voltage} -\text{usually 0.2 - 0.4 V for modern N-FETs} \]

\( \lambda \) gives slope of output characteristics: \( 1/\lambda \) typically 3 - 20 V
The knee voltage defines the boundary between the Ohmic and constant-current regions.

In the mobility-limited regime, \( V_{GD} = V_{th} \) - 
the knee in curve occurs when \( V_{dg} = V_{ds} - V_{gs} = -V_{th} \).

The Knee Voltage is further increased by voltage drops across the parasitic source & drain resistances.
Knee Voltage: Velocity-Limited Case

In the velocity-limited regime, the knee in curve occurs when \( V_{ds} = v_{sat} L_g / \mu \)

Again, the Knee Voltage is further increased by voltage drops across the parasitic source & drain resistances.
Which Model to use When?

If $V_{gs} - V_{th} < \Delta V$, where $\Delta V \approx v_{sat}L_g / \mu$, use the mobility-limited model.

If $V_{gs} - V_{th} > \Delta V$, use the velocity-limited model.
Linear vs. Square-Law Characteristics: 90 nm
Which Model to use When?

For 90 nm CMOS, ΔV is about 0.2-0.3 V

For 45 nm CMOS, ΔV is about 0.15 V

Short gate length devices obey the velocity model.

-but-

Short gate length devices have very low breakdown voltage.

-so-

Analog circuit design is very hard with short-gate-length devices.
90 nm MOSFET DC Characteristics

N-channel

\[ g_m / W_g = c_{ox} v_{sat} = 1.4 \text{ mS/\(\mu\)m} = 1.4 \text{ S/mm} \]

\[ V_{th} = 0.6 \text{ V} \quad 1/\lambda \sim 3 \text{ V} \]

P-channel

\[ g_m / W_g = c_{ox} v_{sat} = 0.7 \text{ mS/\(\mu\)m} = 0.7 \text{ S/mm} \]

\[ |V_{th}| = 0.6 \text{ V} \quad 1/\lambda \sim 3 \text{ V} \]
180 nm MOSFET DC Characteristics

\[ g_m / W_g = c_{ox} v_{sat} = 35 \text{mA} / (2 \text{V} \cdot 80 \mu \text{m}) \]

\[ = 0.22 \text{mS/\mu m} = 0.22 \text{S/mm} \]

This is lower than typical of a 180 nm device

\[ V_{th} = 0.5 \text{ V} \]
To turn the device on, the gate must be more negative than the source, by an amount exceeding the threshold voltage, $V_{th}$.,
P-Channel MOSFET

\[ I_{D,\mu} = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2 (1 + \lambda V_{DS}) \]

\[ I_{D,v} = c_{ox} W_g V_{sat} (1 + \lambda V_{DS})(V_{gs} - V_{th} - \Delta V / 2) \]

\[ \Delta V \approx V_{sat} L_g / \mu \]
The device is in the constant current region if $V_{ds}$ above the knee voltage.

Example: Constant mobility model:

$k_\text{m} \propto V_{dg} < -V_{th}$

Example: Suppose the threshold voltage is -1V.

Then the P-MOSFET is in the constant current region if the drain is at most 1V more positive than the gate.
FET Small-Signal Model: Mobility-Limited

Drain Current

\[ I_D = (\mu c_{ox} W_g / 2 L_g) (V_{gs} - V_{th})^2 (1 + \lambda V_{DS}) \]

Transconductance

\[ g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = (\mu c_{ox} W_g / L_g) (V_{gs} - V_{th}) (1 + \lambda V_{DS}) \approx (\mu c_{ox} W_g / L_g) (V_{gs} - V_{th}) \]

Output Conductance

\[ G_{ds} = \frac{1}{R_{ds}} = \frac{\partial I_D}{\partial V_{DS}} = \frac{\lambda I_D}{1 + \lambda V_{DS}} \approx \lambda I_D \text{ to within the accuracy of the models we are using} \]

Note that \( R_{ds} \) varies roughly as \( 1/I_D \).
FET Small-Signal Model: Velocity-Limited

Drain Current

\[ I_D = c_{ox} v_{sat} W_g (1 + \lambda V_{DS}) (V_{gs} - V_{th} - \Delta V / 2) \]

Transconductance

\[ g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = c_{ox} v_{sat} W_g (1 + \lambda V_{DS}) \approx c_{ox} v_{sat} W_g \]

Output Conductance

\[ G_{ds} = \frac{1}{R_{ds}} \equiv \frac{\partial I_D}{\partial V_{DS}} = \frac{\lambda I_D}{1 + \lambda V_{DS}} \]

\[ \approx \lambda I_D \]
Transconductance vs Vgs

mobility – limited

\[ I_{D,\mu} = \mu c_{ox} W_g (V_{gs} - V_{th})^2 / 2L_g \]

\[ \rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu c_{ox} W_g (V_{gs} - V_{th}) / L_g \]

velocity – limited

\[ I_D = c_{ox} W_g v_{sat} (V_{gs} - V_{th} - \Delta V / 2) \]

\[ \rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = c_{ox} W_g v_{sat} \]
These are rough numbers - not real USCI parameters

Case 1  250nm  NMOS

\[ \mu = 400 \text{ cm}^2/\text{V}s \quad \text{Threshold} = 2 \text{nm}, \quad \gamma = 3.8 \]

\[ L_g = 114 \mu\text{m} \quad V_{sat} \approx 10^{7} \text{ cm/s} \]

\[ V_{BS} \approx 0.5 \text{ V} \]
Rough Estimate: 250 nm NMOS Characteristics

\[ V_{gs} = \frac{V_{th}}{2} \ln \frac{g_{m}}{I_{d}} \]

\[ I_{d} = \frac{(1.35 \text{ mA} \mu \text{m})}{(1.68 \text{ mA} \mu \text{m})} \times (V_{gs} - V_{th})^{2} \]

\[ V_{gs} = 0.5 \text{ V} \]

\[ AV = 0.625 \text{ V} \]
Rough Estimate: 250 nm PMOS Characteristics

\[ \mu = 200 \text{ cm}^2/\text{V.s} \]

\[ L_g = 114 \mu \text{m} \]

\[ V_{sat} = 0.5 \times 10^{-7} \text{ cm/s} \]

\[ V_{th} = 0.5 \text{ V} \]

\[ \Delta V = V_{sat} \frac{L_g}{\mu} = 0.625 \text{ V} \]

\[ C_{ox} = \varepsilon_0 \varepsilon_r W \frac{L}{t} \]

\[ C_{ox} \cdot W_g / 2L_g = \left( 0.67 \text{ mA/V}^2 \right) \cdot \left( W_g / 1 \mu \text{m} \right) \]

\[ V_{sat} \cdot C_{ox} \cdot W_g = \left( 0.84 \text{ mA/V} \right) \cdot \left( W_g / 1 \mu \text{m} \right) \]
Rough Estimate: 250 nm PMOS Characteristics

For the 250 nm NMOS & PMOS FETs, well Vgs must exceed Vth by more than 0.6V before constant-velocity parameters are observed.
\[ \mu = 300 \text{ cm}^2/\text{V.s} \]

\[ L_g = 45 \text{ nm} \]

\[ V_{th} = 0.3 \text{ V} \]

\[ V_{sat} \cdot L_g / \mu = \Delta V = 0.15 \text{ V} \]

\[ \mu \cdot \text{Cox} \cdot W_g / 2L_g = (9.35 \text{ mA/V}^2) \cdot (W_g/1 \mu m) \]

\[ \text{Cox} \cdot V_{sat} \cdot W_g = (2.8 \text{ mA/V}) \cdot (W_g/1 \mu m) \]
Rough Estimate: 45 nm NMOS Characteristics

Note: this device is velocity-limited once \( V_{gs} - V_{th} \) exceeds about 0.2V

Note: production 45nm NMOS FETs, circa 2007, have roughly 1/2 the current calculated above; the physical parameters I have used are rough estimates.
Rough Estimate: 45 nm PMOS Characteristics

\[ \mu \approx 150 \text{ cm}^2/\text{V.s} \]

\[ L_g = 45 \text{nm} \]

\[ V_{gs} = 5 \times 10^6 \text{ cm/s} \]

\[ U_{th} = 0.3 \text{ V} \]

\[ V_{gs}L_g/\mu = \Delta U = 0.15 \text{ V} \]

\[ \mu \cdot \text{sat} \cdot W_g L_g = (4.7 \text{ mA/m}^2) \cdot (W_g 1 \text{mm}) \]

\[ V_{gs} \cdot \text{sat} \cdot W_g = (1.4 \text{ mA/m}) \cdot (W_g 1 \text{mm}) \]
Rough Estimate: 45 nm PMOS Characteristics

Once again, for this short-lg device, very little gate overdrive (Vgs-Vth) is needed before Id vs Vgs becomes velocity-saturated (Icur (Vgs-Vth-ΔV)) once again, these rough hand-tgt give currents ~2:1 larger than real 45nm PMOS FETS.
Our MOSFET model: Some comments

1) MOS models in most undergraduate texts ignore velocity saturation, yet velocity saturation is a huge effect in modern MOSFETs.
2) Given (1), there is no consensus on how to teach velocity saturation in undergraduate classes.
3) The 137ab method, here, is my attempt at a reasonably accurate yet simple model.
4) The more accurate expression given here is derived by assuming an exit velocity $v_{sat}$ at the drain end of the channel.
5) Even the more accurate expression is only very approximate for highly scaled MOSFETs: for detailed design, we use foundry CAD models.
6) The exit velocity is not actually $v_{sat}$, but is the thermal or Fermi velocity; I am simply following prevailing (and incorrect) terminology.
7) See publications by M. Lundstrom and D. Antoniadis for good derivations of modern FET I-V characteristics.