Multi-stage amplifiers

To analyze:
1) Find bias, working from input to output
2) Separate into individual stages

\[ V_o = V_{o13} \]
First find $V_{d3}/V_{G3}$ and find $R_{in3}$

Then find $V_{d2}/V_{G2}$ and $R_{in2}$
- Note that $R_{in3}$ enters into the above calculation

Then find $V_{S1}/V_{G1}$ and $R_{in1}$
- Note that $R_{in2}$ enters into the above calculation.

Then find $V_{G1}/V_{G2}$
- depends upon $f_{ren}$ and $R_{in1}$

We can then find

\[
\frac{V_o}{V_{G_{en\ overall}}} = \frac{V_{in}}{V_{G_{en}}} \cdot \frac{V_{S1}}{V_{G1}} \cdot \frac{V_{d2}}{V_{G2}} \cdot \frac{V_{d3}}{V_{G3}}
\]
Explicitly:

Q3:
\[ \text{\textbf{R}_{2g3}} = \text{\textbf{R}_2} \parallel \text{\textbf{R}_{o2}} \parallel \text{\textbf{R}_{o3}} \]
\[ A_r = \frac{V_{o3}/V_{g3}}{R_{o3}} = -9\text{mS} \text{\textbf{R}_{2g3}} \]

\[ R_{in,3} = \infty \]

Q2:
\[ \text{\textbf{R}_{2g2}} = \frac{R_{in,2}}{\text{\textbf{R}_{o2}}} = \infty \parallel \text{\textbf{R}_{o2}} = \text{\textbf{R}_{o2}} \]
\[ R_{in,source,2} = \left( \frac{1}{1.9m_2} \right) \left( \frac{R_{2g2} + R_{o2}}{R_{o2}} \right) \]
\[ A_r = \frac{V_{o2}/V_{s2}}{R_{2g2}/R_{in,source,2}} \]
\[ R_{in,2} = \frac{R_{in,source,2}}{\text{\textbf{R}_{o2}}} \]

Q1:
\[ \text{\textbf{R}_{2g1}} = \text{\textbf{R}_{o1}} \parallel \text{\textbf{R}_{in,2}} \]
\[ A_{r1} = \frac{V_{o1}/V_{g1}}{R_{2g1}} = \frac{R_{2g1}}{R_{2g1} + 1.9m_1} \]

\[ R_{in,1} = R_{g1} \]

generally:
\[ V_{2}/V_{gen} = \frac{R_{in,1}}{R_{in,1} + R_{gen}} \]
To find output impedances, we must work in the opposite direction...

\[ R_{out1} = R_e || \frac{1}{g_{m1}} \]

\[ R_{out2} = R_{out2} || \left\{ R_{out2} \cdot \left( 1 + g_{m2} \cdot R_{out1} \right) \right\} \]

\[ R_{out3} = R_{out3} || R_{out3} \]
The stage-stage interactions are much more significant with bipolar transistors.
for this bipolar example:

Q3/ Common-emitter with degeneration.

\[ R_{\text{eq}3} = R_{e3} || R_\text{ec} || R_\text{ec}' \text{collectors} \]

\[ Q_e \approx R_{e3} (1 + R_\text{ec}/R_{e3}) \]

\[ \alpha_r = \frac{V_{e3}}{V_{eb}} = \frac{R_{\text{eq}3}}{R_{e3} + R_{\text{ec}}'} \]

\[ R_{i3} = \beta (R_{e3} + R_{\text{ec}}') \]

Q2/ Common-base

\[ R_{\text{eq}2} = R_{i3} || R_{e2} \]

\[ R_{\text{emitter}2} = R_{e2} \left(1 + \frac{R_{\text{eq}2}}{R_{e2}}\right) = R_{i2} \]

\[ \alpha_r = \frac{V_{e2}}{V_{eb}} = \frac{R_{\text{eq}2}}{R_{i2}} \cdot \frac{1}{R_{\text{emitter}2}} \]

Q1/ Common-collector

\[ R_{\text{eq}1} = R_{e1} \text{||} R_{\text{ec}1} \text{||} R_{i1} \]

\[ \alpha_r = \frac{V_{e1}}{V_{eb}} = \frac{R_{\text{eq}1}}{R_{e1} + R_{i1}} \]

\[ R_{i1} = \frac{\beta (R_{\text{eq}1} + R_{i1})}{R_{e1}} \]
Multi-stage amplifier example

\[ V_{cc} = 3.3V \]

Q2: \( \beta = 50 \) \( V_A = 100V \)
Q1: \( \beta = 100 \) \( V_A = 100V \)

\[ R_{e1} = 200\Omega \]
\[ R_{e2} = R_L * \]
\[ E_{r} \]
\[ 1.55V \]
\[ 0.55V \]
\[ 0.5V \]
\[ 106mA = I_{e2} \]

*This is a small speaker. To simplify the design, we have not isolated the speaker from the dc bias current of Q2.

\[ I_{e1} = 20mA \]

Bias:

Assume initially that \( \beta_1 = \beta_2 = \infty \)

\[ V_{e1} = V_{cc} (R_6) / (R_6 + R_6) = 1.238V \]
\[ V_{e1} = V_{cc} - 0.7V = 0.538V \]
\[ I_{e1} = V_{cc} / (R_{e1} + R_{e1}) = 21.5mA = I_{e2} \]
\[ V_{coll} = V_{cc} - R_{e1} I_{e1} = 1.58V \]
\[ V_{e2} = V_{e1} - 0.7V = 0.89V \]
\[ I_{e2} = V_{e2} / R_{e2} = 110mA \]

[The subsequent bias analysis is much clearer if done step-by-step on the circuit diagram itself]
we can now repeat bias analysis with finite β:

\[ I_{C1} = 21.5 \text{mA} / \beta, = 21.5 \text{mA} \]

\[ \Rightarrow V_{E1} = 1.238V - I_{E1} R_{E1} = 1.238V - 32.2 \text{mV} = 1.206V \]

\[ V_{E1} = V_{E2} - 0.7V = 0.5V \]

\[ I_{E1} = V_{E1} / (R_{E1} + R_{E2}) = 20.0 \text{mA} \]

\[ I_{E1} = I_{E2} / \beta = 20.0 \text{mA} / 100 = 200 \mu \text{A} \]

\[ \text{close to prior estimate; don't iterate again} \]

\[ I_{C1} = I_{E1} - I_{E2} = 19.8 \text{mA} \]

\[ V_{C1} = V_{CC} - R_{C1} \cdot (I_{C1} + I_{E2}) = 1.516V \]

\[ I_{E2} = 12.5 \text{mA} / 50 = 2.5 \text{mA} \]

\[ V_{E2} = V_{C1} - 0.7V = 0.816V \]

\[ I_{E2} = V_{E2} / R_{E2} = 102 \text{mA} \]

\[ I_{E2} = 102 \text{mA} / 3.2 = 2.04 \text{mA} \]

\[ \text{far from prior estimate; iterate again} \]

\[ V_{C1} = V_{CC} - R_{C1} (I_{C1} + I_{E2}) = 1.55V \]

\[ V_{E2} = V_{C1} - 0.7V = 0.85V \]

\[ I_{E2} = V_{E2} / R_{E2} = 106 \text{mA} \]

\[ \text{close enough; don't iterate again!} \]

\[ \text{Real design: must check} \]

"design corners" (\( \beta_{\text{min}}, \beta_{\text{max}} \))

(V_{CC}, V_{EE, min})

Etc
AC small signal analysis:

Q21 emitter follower

$R_{eq} = 8.2$

$\beta = \frac{26mV}{106mA} = 0.242$

$N_v = \frac{R_{eq}}{R_{eq} + \beta}$

$R_{in} = \beta (\beta + R_{eq}) = 412 \Omega$

Q21 common emitter with degeneration:

$R_{CE} = \frac{V_A}{I_C} = 541 \Omega$

$R_{EB} = \frac{26mV}{20mA} = 1.3 \Omega$

$R_{eb} \text{ collector } \approx R_{CE} (1 + \frac{R_{EC}}{R_{BE}}) >> R_{E1}$

- neglect $R_{EB} \text{ collector}$

$R_{eq1} = R_{CE} \parallel R_{E1} \parallel R_{in1} \approx R_{EC} \parallel R_{in2}$

$= \frac{541 \Omega \times 412 \Omega}{541 \Omega + 412 \Omega} = 67.0 \Omega$

$N_v = \frac{-R_{eq1}}{R_{E1} + R_{EC1}} = -67 \Omega \div (61 \Omega + 1.3 \Omega)$

$= -9.18$

$R_{in, F1} = \frac{1}{\beta} \left( \frac{R_{E1} + R_{EC1}}{R_{E1}} \right) = 100 \left( \frac{61 \Omega + 1.3 \Omega}{61 \Omega} \right) = 730 \Omega$

$R_{in, amplifier} = R_{in, F1} \parallel R_{in1} \parallel R_{in2} = 124.4 \Omega$

overall $N_v = N_v1 \cdot N_v2 = -9.18 \cdot 0.971 = 8.71$
Maximum Signal Swings:

**Q2 Saturated**

\[ V_{CE2,Q} = 3.8V - 0.85V = 0.95V \]
\[ V_{CE, sat} = 0.5V \]
\[ \Delta V_{CE} = 2.45V - 0.5V = 1.95V = \Delta V_{C} - \Delta V_{E} \]
\[ \Delta V_{max} = 1.95V \]

**Q2 Cutoff**

\[ I_{C2,Q} = 106mA \]
\[ RL = 8.12 \]
\[ \Delta V_{max} = 8.12 \cdot 106mA = 0.848V \]

**Q1 Saturated**

\[ V_{CE1,Q} = 1.55V - 1.50V = 0.05V \]
\[ V_{CE, sat1} = 0.5V \]
\[ \Delta V_{CE1} = 1.05V - 0.5V = 0.55V = \Delta V_{C} \]
\[ \Delta V_{max1} = \Delta V_{C1} \cdot AV_2 = 0.55V \cdot 0.97 = 0.53V \]

**Q1 Cutoff**

\[ I_{C1,Q} = 20mA \]
\[ \Delta V_{C1} = 20mA \cdot RL = 20mA \cdot 0.572 = +1.144V \]
\[ \Delta V_{C1} = \Delta V_{C1} \cdot AV_2 = +1.30V \]

Maximum positive swing is +1.30V (Q1 cutoff)
Maximum negative swing is -0.53V (Q1 saturation)
If this were a real design, or if this were a lab project, one would need to check:

- maximum range of the key specifications as supply and component values vary over their full permissible range (\(\beta_{\text{max}}\), \(\beta_{\text{min}}\), \(V_{\text{CEmax}}\), \(V_{\text{CEmin}}\), resistor tolerances)

- DC power dissipation in \(kA\) and \(\text{MW}\)

- currents relative to \(I_{\text{E, max}}\)

- voltages relative to breakdown

- junction temperature rise - need to keep safe?

- etc.