LM118-N/LM218-N/LM318-N Operational Amplifiers

Check for Samples: LM118-N, LM218-N, LM318-N

 FEATURES

• 15 MHz Small Signal Bandwidth
• Ensured 50V/μs Slew Rate
• Maximum Bias Current of 250 nA
• Operates from Supplies of ±5V to ±20V
• Internal Frequency Compensation
• Input and Output Overload Protected
• Pin Compatible with General Purpose Op Amps

 DESCRIPTION

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM218-N is identical to the LM118 except that the LM218-N has its performance specified over a –25°C to +85°C temperature range. The LM318-N is specified from 0°C to +70°C.

Fast Voltage Follower

Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings\(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td>±20V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Dissipation (^{(3)})</td>
<td></td>
<td>500 mW</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Current (^{(4)})</td>
<td></td>
<td>±10 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage (^{(5)})</td>
<td></td>
<td>±15V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Short-Circuit Duration</td>
<td></td>
<td>Continuous</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td>lm118-n: −55°C to +125°C</td>
<td>LM218-N: −25°C to +85°C</td>
<td>LM318-N: 0°C to +70°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td>−65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec.)</td>
<td></td>
<td>TO-99 Package: 300°C</td>
<td>PDIP Package: 260°C</td>
<td></td>
</tr>
</tbody>
</table>

#### Soldering Information

- TO-99 Package: 300°C
- PDIP Package: 260°C

#### Electrical Characteristics \(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM118-N/LM218-N</th>
<th>LM318-N</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>(T_A = 25°C)</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>(T_A = 25°C)</td>
<td>6</td>
<td>50</td>
<td>30</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>(T_A = 25°C)</td>
<td>120</td>
<td>250</td>
<td>150</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>(T_A = 25°C)</td>
<td>1</td>
<td>3</td>
<td>0.5</td>
</tr>
<tr>
<td>Supply Current</td>
<td>(T_A = 25°C)</td>
<td>5</td>
<td>8</td>
<td>5</td>
</tr>
<tr>
<td>Large Signal Voltage Gain (V_{OUT} = \pm 10V, R_L \geq 2 kΩ)</td>
<td>(T_A = 25°C, V_S = \pm 15V)</td>
<td>50</td>
<td>200</td>
<td>25</td>
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<tr>
<td>Slew Rate (\text{V}/\mu\text{s})</td>
<td>(T_A = 25°C, V_S = \pm 15V, A_V = 1)</td>
<td>50</td>
<td>70</td>
<td>50</td>
</tr>
<tr>
<td>Small Signal Bandwidth</td>
<td>(T_A = 25°C, V_S = \pm 15V)</td>
<td>15</td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td></td>
<td>6</td>
<td></td>
<td>15</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td></td>
<td>100</td>
<td></td>
<td>300</td>
</tr>
</tbody>
</table>

\(^{(1)}\) These specifications apply for \(\pm 5V \leq V_S \leq \pm 20V\) and \(−55°C \leq T_A \leq +125°C\) (lm118-n), \(−25°C \leq T_A \leq +85°C\) (LM218-N), and \(0°C \leq T_A \leq +70°C\) (LM318-N). Also, power supplies must be bypassed with 0.1 \(\mu\)F disc capacitors.

\(^{(2)}\) Slew rate is tested with \(V_S = \pm 15V\). The lm118-n is in a unity-gain non-inverting configuration. \(V_{IN}\) is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and specified to exceed 50V/\(\mu\)s.
### Electrical Characteristics *(f)* (continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LM118-N/LM218-N</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Bias Current</td>
<td></td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500</td>
<td></td>
</tr>
<tr>
<td>Supply Current</td>
<td>$T_A = 125^\circ C$</td>
<td>4.5</td>
<td>7</td>
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<tr>
<td>Large Signal Voltage Gain</td>
<td>$V_S = \pm 15V, V_{OUT} = \pm 10V$</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_L \geq 2 , k\Omega$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td>$V_S = \pm 15V, R_L = 2 , k\Omega$</td>
<td>$\pm 12$</td>
<td>$\pm 13$</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>$V_S = \pm 15V$</td>
<td>$\pm 11.5$</td>
<td>$\pm 11.5$</td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td></td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>Supply Voltage Rejection Ratio</td>
<td></td>
<td>70</td>
<td>80</td>
</tr>
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</table>

*(f)* Values are for $-40^\circ C$ to $125^\circ C$ unless otherwise noted.
TYPICAL PERFORMANCE CHARACTERISTICS
LM118-N, LM218-N

Input Current

![Input Current Graph](image)

Voltage Gain

![Voltage Gain Graph](image)

Power Supply Rejection

![Power Supply Rejection Graph](image)

Input Noise Voltage

![Input Noise Voltage Graph](image)

Common Mode Rejection

![Common Mode Rejection Graph](image)

Supply Current

![Supply Current Graph](image)
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

Closed Loop Output Impedance

\[ V_S = \pm 15V \]
\[ T_A = 25^\circ C \]
\[ A_V = 1000 \]
\[ A_V = 1 \]

FREQUENCY (Hz)

Figure 7.

Current Limiting

\[ V_S = \pm 15V \]
\[ T_A = 25^\circ C \]
\[ T_A = 125^\circ C \]

OUTPUT CURRENT (mA)

Figure 8.

Input Current

\[ T_A = 25^\circ C \]

DIFFERENTIAL INPUT (V)

Figure 9.

Unity Gain Bandwidth

\[ V_S = \pm 20V \]
\[ V_S = \pm 15V \]
\[ V_S = \pm 10V \]
\[ V_S = \pm 5V \]

TEMPERATURE (°C)

Figure 10.

Voltage Follower Slew Rate

\[ V_S = \pm 15V \]
\[ R_S = R_f = 10 \, k\Omega \]
\[ C_f = 5 \, pF \]

TEMPERATURE (°C)

Figure 11.

Inverter Settling Time

\[ V_S = \pm 15V \]
\[ T_A = 25^\circ C \]
\[ R_S = 5 \, k\Omega \]
\[ R_f = 5 \, k\Omega \]
\[ C_f = 10 \, pF \]
\[ C_o = 0.1 \, \mu F \]

TIME (μs)

Figure 12.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

Large Signal Frequency Response

![Large Signal Frequency Response Graph](image1)

Open Loop Frequency Response

![Open Loop Frequency Response Graph](image2)

Voltage Follower Pulse Response

![Voltage Follower Pulse Response Graph](image3)

Inverter Pulse Response

![Inverter Pulse Response Graph](image4)
Typical Performance Characteristics

LM318-N

Input Current

Voltage Gain

Power Supply Rejection

Input Noise Voltage

Common Mode Rejection

Supply Current
Typical Performance Characteristics (continued)

LM318-N

Closed Loop Output Impedance

![Closed Loop Output Impedance Graph](image)

Current Limiting

![Current Limiting Graph](image)

Input Current

![Input Current Graph](image)

Unity Gain Bandwidth

![Unity Gain Bandwidth Graph](image)

Voltage Follower Slew Rate

![Voltage Follower Slew Rate Graph](image)

Inverter Settling Time

![Inverter Settling Time Graph](image)
Typical Performance Characteristics (continued)

**LM318-N**

![Large Signal Frequency Response](image1)

- Frequency: 0.5M to 50M Hz
- **TA = 25°C**
- **VS = ±15V**

![Open Loop Frequency Response](image2)

- Frequency: 10 to 10000000 Hz
- **TA = 25°C**
- **VS = ±15V**

**Voltage Follower Pulse Response**

- Time (μs): 0.2 to 1.8
- **VS = ±15V**
- **TA = 25°C**

![Open Loop Frequency Response](image3)

- Frequency: 10 to 10000000 Hz
- **TA = 25°C**
- **VS = ±15V**

**Large Signal Frequency Response**

- Frequency: 0.5M to 50M Hz
- **TA = 25°C**
- **VS = ±15V**

![Open Loop Frequency Response](image4)

- Frequency: 10 to 10000000 Hz
- **TA = 25°C**
- **VS = ±15V**

**Inverter Pulse Response**

- Time (μs): 0.1 to 0.9
- **VS = ±15V**
- **TA = 25°C**
**AUXILIARY CIRCUITS**

*Balance circuit necessary for increased slew.
Slew rate typically 150V/µs.

**Figure 37. Feedforward Compensation for Greater Inverting Slew Rate**

Slew and settling time to 0.1% for a 10V step change is 800 ns.

**Figure 38. Compensation for Minimum Settling Time**

**Figure 39. Offset Balancing**

**Figure 40. Isolating Large Capacitive Loads**

**Figure 41. Overcompensation**
TYPICAL APPLICATIONS

Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

Figure 42. Fast Voltage Follower

\[ C_F = \text{Large} \quad (C_F \geq 50 \text{ pF}) \]

*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

Figure 43.

Figure 44. Fast Summing Amplifier

Figure 45. Differential Amplifier
Figure 46. Fast Sample and Hold

Figure 47. D/A Converter Using Ladder Network

*Optional—Reduces settling time.
ΔOutput zero.

* "Y" zero
+ "X" zero
‡ Full scale adjust.

Figure 48. Four Quadrant Multiplier

*Optional—Reduces settling time.

Figure 49. D/A Converter Using Binary Weighted Network
Figure 50. Fast Summing Amplifier with Low Input Current

Figure 51. Wein Bridge Sine Wave Oscillator

Figure 52. Instrumentation Amplifier

*Gain ≥ $\frac{200K}{R_g}$ for $1.5K \leq R_g \leq 200K$
Pin Diagram

Dual-In-Line Package (Top View)
See Package Number J (R-GDIP-T14)

Dual-In-Line Package (Top View)
See Package Number NAB008A, D (R-PDSO-G8), or P (R-PDIP-T8)

TO-99 Package (Top View)
See Package Number LMC (O-MBCY-W8)

Pin connections shown on schematic diagram and typical applications are for TO-99 package.
## REVISION HISTORY

<table>
<thead>
<tr>
<th>Changes from Revision B (March 2013) to Revision C</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed layout of National Data Sheet to TI format</td>
<td>16</td>
</tr>
</tbody>
</table>
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM118H</td>
<td>ACTIVE</td>
<td>TO-99</td>
<td>LMC</td>
<td>8</td>
<td>500</td>
<td>TBD</td>
<td>Call Ti</td>
<td>Call Ti</td>
<td>-55 to 125</td>
<td>(LM118H ~ LM118H)</td>
<td></td>
</tr>
<tr>
<td>LM118H/NOPB</td>
<td>ACTIVE</td>
<td>TO-99</td>
<td>LMC</td>
<td>8</td>
<td>500</td>
<td>TBD</td>
<td>Call Ti</td>
<td>Call Ti</td>
<td>-55 to 125</td>
<td>(LM118H ~ LM118H)</td>
<td></td>
</tr>
<tr>
<td>LM318M</td>
<td>NRND</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
<td>TBD</td>
<td>Call Ti</td>
<td>Call Ti</td>
<td>0 to 70</td>
<td>LM318M</td>
<td></td>
</tr>
<tr>
<td>LM318M/NOPB</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LM318M</td>
<td></td>
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<tr>
<td>LM318MX/NOPB</td>
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<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
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<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LM318M</td>
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<tr>
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<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
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<td>Level-1-NA-UNLIM</td>
<td>0 to 70</td>
<td>LM318N</td>
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</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **Eco Plan** - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD**: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# TAPE AND REEL INFORMATION

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM318MX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.5</td>
<td>5.4</td>
<td>2.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**REEL DIMENSIONS**

- **Reel Diameter**
- **Reel Width (W1)**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Q1, Q2, Q3, Q4**: Pocket Quadrants
- **Sprocket Holes**: User Direction of Feed
## TAPE AND REEL BOX DIMENSIONS

![Diagram of tape and reel box dimensions](image)

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
<tbody>
<tr>
<td>LM318MX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
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</table>
NOTES:
A. All linear dimensions are in inches (mmillimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0.25) R Ø MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Fits within JEDEC MO-002/T0-99.
P (R-PDIP-T8)  PLASTIC DUAL-IN-LINE PACKAGE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
MECHANICAL DATA

D (R-PDSO-G8) PLASTIC SMALL OUTLINE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[\text{Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.}\]
\[\text{Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.}\]
E. Reference JEDEC MS-012 variation AA.

4040047–3/M  06/11

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