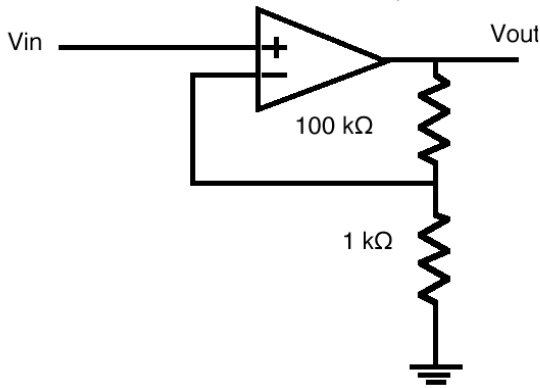
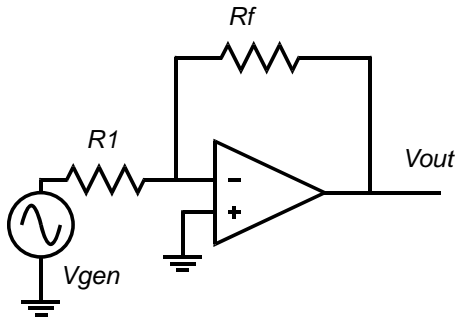


ECE137B Problem set #6,



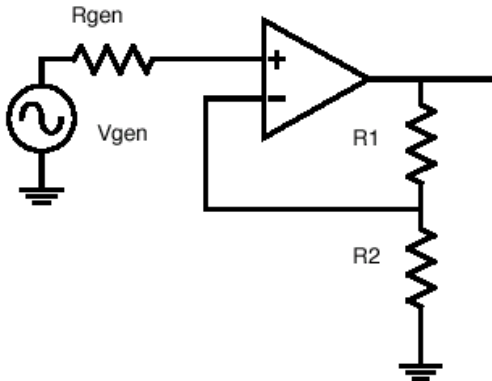
Problem 1

- a) The operational amplifier has infinite input impedance, zero output impedance, infinite common-mode rejection ratio, and a differential gain of  $A_{diff}=10,000$ . Find the gain  $V_{out}/V_{in}$ . (b) Now suppose that the op-amp has a differential input impedance of  $10\text{ k}\Omega$ . Find the closed-loop input impedance. (c) the differential amplifier has an output impedance of  $100\text{ }\Omega$ . Find the closed-loop output impedance.



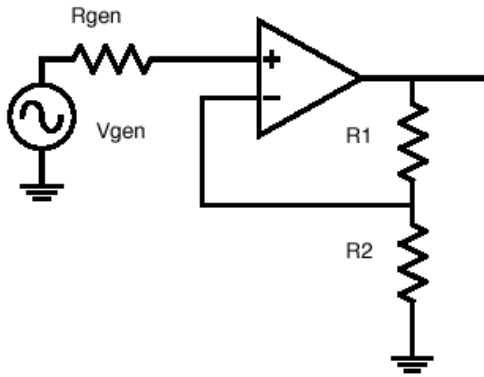
Problem 2

The operational amplifier shown above has zero output impedance, infinite common-mode rejection ratio, and a differential gain of  $A_{diff}=1000$ .  $R_f=1\text{ M}\Omega$ ,  $R_1=10\text{ k}\Omega$ . The amplifier input impedance, however, is only  $100\text{ }\Omega$ . Find the gain  $V_{out}/V_{gen}$ .



Problem 3. Feedback amplifier stability analysis by the Bode method. The operational amplifier has a differential gain of  $1,000,000$ . Its differential gain has three significant poles, one at  $1\text{ kHz}$ , one at  $1\text{ GHz}$ , and one at  $5\text{ GHz}$ . The amplifier is otherwise ideal.  $R_{gen}=0$ . We will consider 2 cases: a)  $R_1=0$  and  $R_2=1\text{ k}\Omega$  b)  $R_1=9\text{ k}\Omega$  and  $R_2=1\text{ k}\Omega$ . In each of cases a), and b) do the following:

- Draw Bode plots (Magnitude and phase) of  $A_d(f)$  and  $\beta(f)$
- Find the loop bandwidth and estimate from this the bandwidth of  $V_{out}/V_{gen}$ .
- Find the gain margin and the phase margin of the feedback loop. Is the amplifier stable ?



**Problem 4**

Stability analysis: the Root Locus  
 The operational amplifier has a differential gain of 1,000,000. Its differential gain has **two** significant poles, one at 1 Hz, and one at 1 MHz. The amplifier is otherwise ideal.  $R_{gen}=0$ . Consider 2 cases: a)  $R1=0$  and  $R2=1k\Omega$  b)  $R1=99k\Omega$  and  $R2=1k\Omega$ . In each of cases a), and b) do the following:

Solve mathematically for  $V_{out}(s)/V_{gen}(s)$   
 Find the natural frequency, the damped frequency, and the damping factor  
 Draw to scale the location of the poles of  $V_{out}(s)/V_{gen}(s)$  on the S-plane.

Graph the (amplitude) of  $V_{out}(j\omega)/V_{gen}(j\omega)$

Graph the step response of the amplifier {  $V_{out}(t)$  given  $V_{in}(t)=1V*U(t)$  }

**Problem 5 :** The transistors are modeled by the small signal model below left, and have  $g_m = v_{sat} c_{ox} W_g = 1 \text{ mS} / \mu\text{m} * W_g$ ,

$$C_{gs} = 1.5 \text{ fF} / \mu\text{m} * W_g$$

$C_{gd} = 0.3 \text{ fF} / \mu\text{m} * W_g$ , and have a 0.3 volt threshold. The supplies are +/- 3 volts.  $\lambda = 0$ .  $Q_{1,2,4,5,6,7,9}$  are to be biased at 0.3 mA. Find  $R_{bias}$ .

$R_{gen} = R_{in}/10 = 1 \text{ k}\Omega$ .  $W_g = 2 \text{ microns}$  for  $Q_{1,2,4,5,6}$ . You need to find  $W_g$  for the other FETs.  $R_{f2} = 100 \text{ k}\Omega$ ,  $R_{f1} = 1 \text{ M}\Omega$ . (a) Find all DC bias conditions (b) At low frequencies, find the loop gain  $T$ ,  $A_{\infty}$ , and the closed loop gain  $A_{cl} = V_{out}/V_{gen}$ . (c) Using your preferred method of analysis, find the location of all significant poles in the loop transmission. c) Draw a Bode plot of the magnitude of  $T(j\omega)$ . Find the phase margin of the feedback loop.

