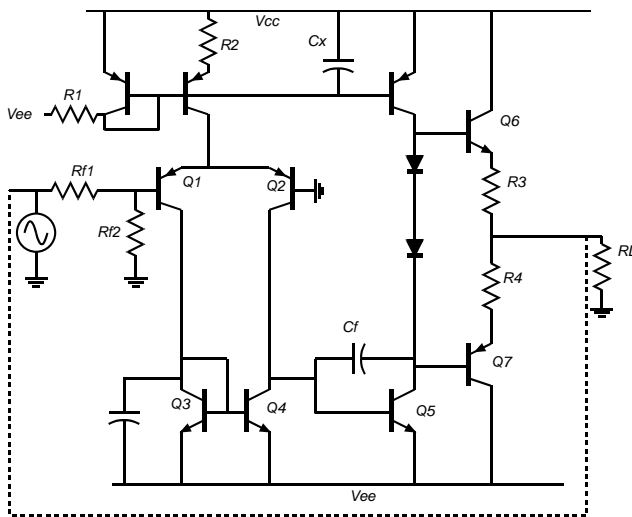


**Problem 1.** All transistors except the output transistors have  $C_{je}=25$  fF,  $C_{cb}=50$  fF and  $\tau_f=1$  ps. The push pull output transistors have  $C_{je}=250$  fF,  $C_{cb}=500$  fF and  $\tau_f=1$  ps. All transistors have infinite beta, and infinite  $V_a$ , EXCEPT Q4 and Q5, giving them infinite beta but  $V_a=100$  Volts. The 2 diodes are matched to the 2 output transistors. The load resistance is 500 Ohm.  $C_x$  is infinity. The supplies are + and - 3.3 volts. Q6 and Q7 are biased at 5 mA. All transistors are matched in  $I_s$ . Choose R1 so that Q5 is biased at 10 mA emitter current. Choose R2 so that Q1 and Q2 are biased at 1 mA each.  $R_{f1}=900$  Ohm,  $R_{f2}=100$  Ohm. a) Find the DC bias conditions. Find the open-loop (Differential) gain of the operational amplifier. Choose  $C_f$  so that the closed-loop bandwidth is 1 GHz.



b) High Frequency analysis. Assume Q7 is on and Q6 is off. With an infinite capacitor shorting C3, use the MOTC to find  $a_1$  and  $a_2$  associated with Q1 and Q2's input. (the high frequency analysis splits at Q2, because it is operating as a common base stage). Then, using the approximation that the time constant associated with  $(C_{cb5}+C_f)$  is much larger than other time constants in the Q4/Q5/Q7 signal path, find  $a_1$  and  $a_2$  associated with this part of the circuit. Find the overall transfer function of the form

- Draw Bode plots (Magnitude and phase) of  $A_d(f)$  and  $\beta(f)$
- Find the loop bandwidth and estimate from this the bandwidth of  $V_{out}/V_{gen}$ .
- Find the gain margin and the phase margin of the feedback loop. Is the amplifier stable? (Note that there is a second signal path through the amplifier, as illustrated at left. This is somewhat beyond the scope of the class...we will simply assume in 137b that the 2 paths have similar time constants.)

