Both the NMOS and PMOS FETs have 0.8 nm oxide thickness, 16 nm gate length, and a 0.25 V threshold. Mobility is 400 cm²/(V·s), injection velocity is 1E7 cm/s, and 1/lambda=infinity. The gate capacitance $C_{gs}$ is $\varepsilon_r\varepsilon_0L_gW_g/T_o+(0.5fF/\mu m)\cdot W_g$
while $C_{gd}$ is $(0.5fF/\mu m)\cdot W_g$

**Problem 1:**
We will choose all FET widths such that $|V_{gs}|=0.3$ V.
The supplies are +/- 1.0 volts
Q8,7,6 are to be biased at 50 $\mu$A

Find Rbias.
RL=500 kOhm. Rgen=Rin/10=10 kOhm.

To simplify the problem, the indicated capacitors are AC short circuits (do not treat these as capacitors in an MOTC analysis) (a) Find all DC bias conditions (b) find all device capacitances (c) find the circuit gain and (d) Find the all significant poles in the transfer function Vout/Vin

**Problem 2**
A simple operational amplifier. The power supplies are ±5 volts. Pick R1 so that Q1 and Q2 are biased at 0.25 mA. Pick R2 so that Q5 is biased at 5 mA. Pick R3=R4 so that the ouptut transistors are biased at 1 mA.

Assume feedback forces Vout to zero volts DC. All transistors have the same emitter saturation current, have $\tau_f=0.5$ ps, $C_{je}=5$ fF, $C_{cb}=10$ fF for the NPN and $\tau_f=3$ ps, $C_{je}=20$ fF, $C_{cb}=50$ fF for the PNP. $\beta=50$, $V_A=\infty$. The load resistance is 2 kΩ. $C_f$ is 10 pF. In the circuit connection shown (Rf1=9Kohm and Rf2=1kOhm represent the feedback network), we are calculating the gain around the feedback loop. This is represented by the dotted line, which you should not treat as a connection. Find the gain Vout/Vgen. Using MOTC, find the 2 dominant poles in the transfer function.

MAJOR COMMENT. There is a difficulty in that the Q1-Q4 stage has 2 paths from input-output. To simplify this problem, I have added Cx, a
Problem 3.
Q1 and Q2 have $\beta=50$ and $V_A=\infty$. $C_{je}=200 \, fF$, $C_{eb}=200 \, fF$ and the forward transit time is 1 pS. $V_{cc} = -V_{ee}=3.3 \, Volts$. $R_{load}=100 \, Ohms$, $R_{gen}=500 \, OHms$, $R_{in}=500 \, Ohm$. Q2 is to be biased at 250 mA and Q1 is to be biased at 50 mA.
a) Find the DC bias conditions and the voltage gain $V_{out}/V_{gen}$.
b) Use the method of time constants to find the 2 dominant pole frequencies of the circuit.
d) Draw Bode plots for parts b) and c).