ECE ECE145A (undergrad) and ECE218A (graduate)

Final Exam. Tuesday, December 8, 12-3 p.m.

Do not open exam until instructed to.
Open notes, open books, etc. You have 3 hrs.
Use all reasonable approximations (5% accuracy is fine.) ,
AFTER STATING and justifying THEM.
<u>Think before doing complex calculations.</u> Sometimes there is an easier way.

Problem	Points Received	Points Possible
1a		5
1b		7
2a		7
2b		5
3a		5
3b		7
3c		8
3d		5
3e		5
3f		5
4a		5
4b		7
4c		5
4d		5
5a		6
5b		5
5c		8
total		100

Name: ________________________

$$G_T = \frac{|S_{21}|^2 (1-|\Gamma_s|^2)(1-|\Gamma_L|^2)}{|(1-\Gamma_s S_{11})(1-\Gamma_L S_{22}) - S_{21}S_{12}\Gamma_s\Gamma_L|^2} \qquad G_P = \frac{1}{1-||\Gamma_{in}||^2}\cdot|S_{21}|^2\cdot\frac{1-|\Gamma_L|^2}{|1-\Gamma_L S_{22}|^2}$$

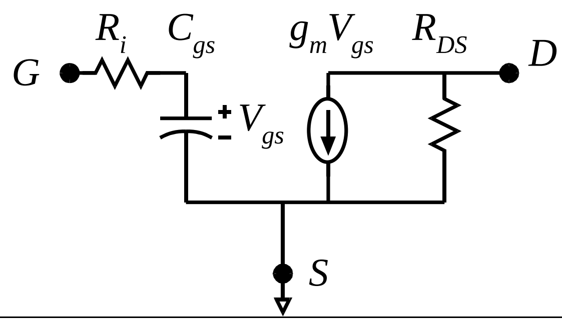
$$G_a = \frac{1-|\Gamma_S|^2}{|1-\Gamma_S S_{11}|^2}\cdot|S_{21}|^2\cdot\frac{1}{1-||\Gamma_{out}||^2} \qquad G_{\max} = \frac{|S_{21}|}{|S_{12}|}\cdot\left[K-\sqrt{K^2-1}\right] \text{if } K>1$$

$$G_{MS} = \frac{|S_{21}|}{|S_{12}|}\cdot \text{if } K<1 \qquad K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|} \quad \text{where } \Delta = \det[S]$$

Unconditionally stable if : (1) K>1 **and** (2) $||\det[S]||<1$

Problem 1, 12 points
Two-port properties, Gain relationships

<u>part a, 5 points</u>

Transistor cutoff frequencies C_{gs} =100 fF, g_m =100 mS. R_{ds} =100 Ohms, R_i =10 Ohms, Find f_τ and $f_{\mathbf{max}}$.	

part b, 7 points

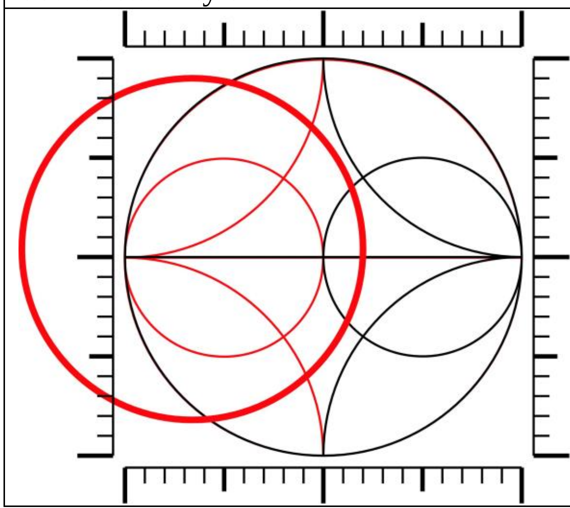
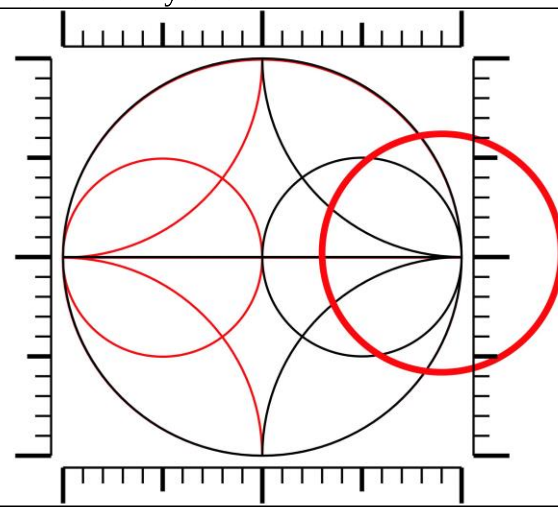
Find the short-circuit current gain and the maximum available power gain at 60 GHz

Problem 2, 12 points

Potentially unstable amplifier design

part a, 7 points

At a design frequency of 1 GHz, a common-source FET has source and load stability circles as below

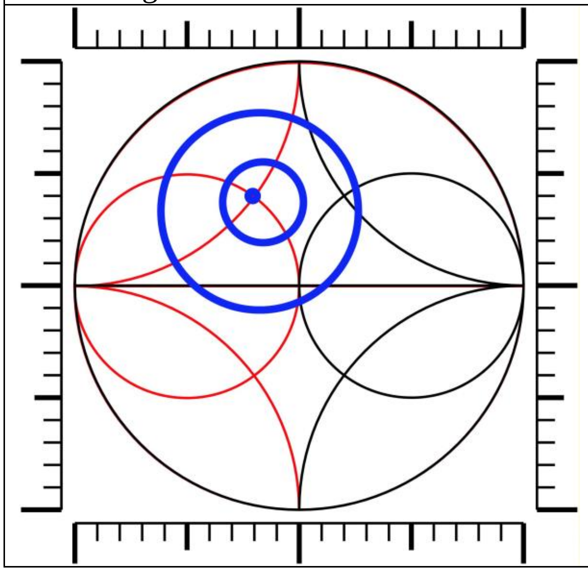
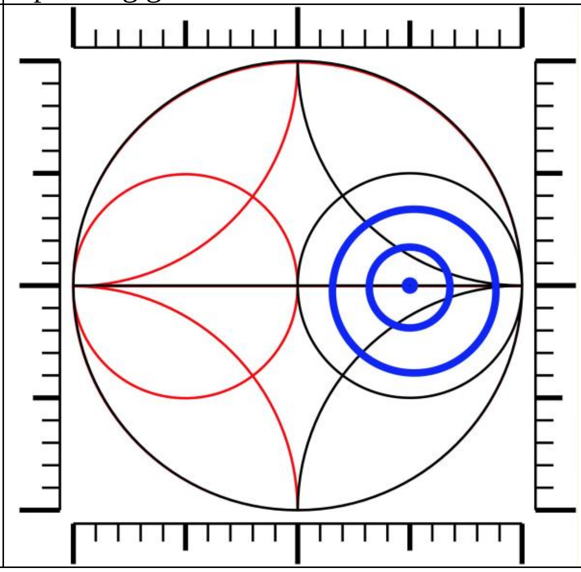
Source stability circle	load stability circle
	

Given that S11=0.5 and S22=1.1 at 1GHz, draw two stabilization circuits in the boxes below, giving element values

Solution 1	Solution 2

part b, 5 points

A FET has available and operating gain circles as below at 1 GHz.

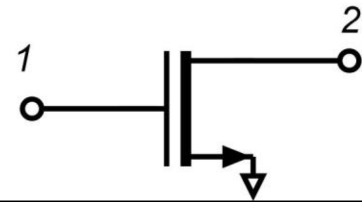
available gain	operating gain
	

Assuming a 50Ohm impedance normalization, what are the optimum generator and load impedances ?

$Z_{gen,opt}$ =______________________ $Z_{l,opt}$ = _____________________________

Problem 3, 35 points

Power gains and stability

The transistor has S11=0, S12=0.1, S21=8, S22=0.5	

part a, 5 points

If the load impedance is an open-circuit, what is the input reflection coefficient?

Γ_{in} =______________________

part b, 7 points

Is it necessary to stabilize the device before simultaneous input and output matching to it ? Assuming that you have stabilized, if necessary, or have not stabilized (if not necessary), what power gain will you obtain after matching on both input and output ?

Unconditionally Stable ? __________

Power gain after simultaneous matching=_________________________

part c, 8 points

(hard thinking, ok math): Can you determine from the S-parameters above what values of source reflection coefficient would lead to potential instability ? Can you determine the necessary value of parallel input stabilization resistance ?

part d, 5 points

Without stabilizing the FET, the FET is connected to a 100 Ohm generator, with 1mW available power, and a 100 Ohm load. Find the power in the load

$P_L =$ ____________________

part e, 5 points

Without stabilizing the FET, the FET is connected to a 50 Ohm generator, with 1mW available power, and a 50 Ohm load. Find the power in the load

$P_L =$ ____________________

part f, 5 points

Without stabilizing the device, the generator, with 1mW available power, is impedance-matched to the FET input, and is then connected directly to a 100 Ohm load. Find the power in the load

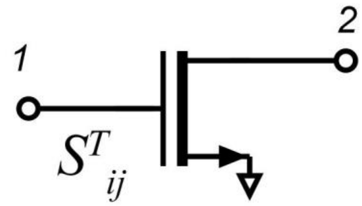
$P_L =$ ____________________

Problem 4, 22 points

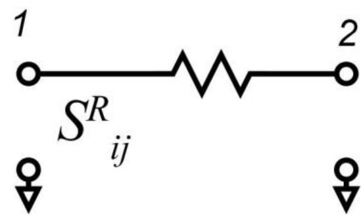
S parameters and Signal flow graphs

A transistor has the following s-parameters:

S11=0.5
S22=0.25
S12=0.5
S21=5



A second two-port consists of a 25 Ohm resistor between its input and output ports



part a, 5 points

Using a 50 Ohm impedance standard, compute the four S-parameters of the resistor network.

S11=______________ S12=______________ S21=_______________
S22=_____________

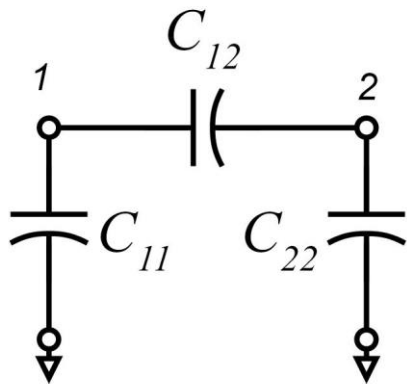
part b, 7 points

The resistor network is connected between to the FET input. Compute the four S-parameters of the combined network.

S11=______________   S12=______________ S21=_______________
S22=_____________

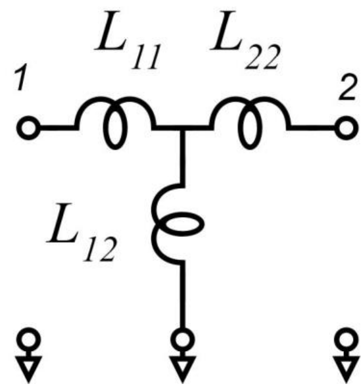
part c, 5 points

Y-parameters

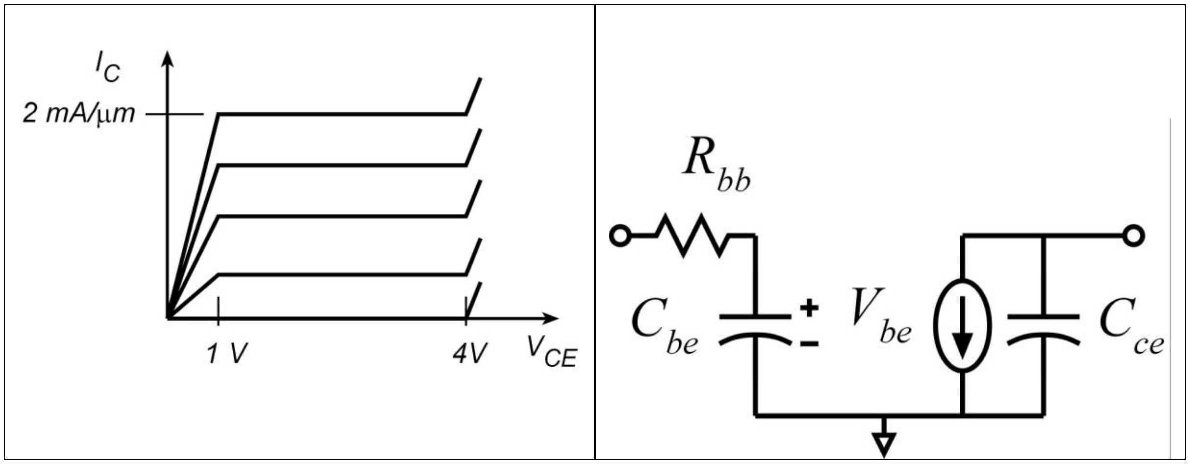
Compute the Y-parameters of this network	

<u>part d, 5 points</u>

Z-parameters

Compute the Z-parameters of this network	

Problem 5, 19 points
Power amplifier design



An HBT has the output characteristics as shown, with a maximum 2mA/micron collector current. The (somewhat contrived) device model is to the right, with $g_m = 20.0mS/\mu m \cdot L_E$ $R_{bb} = 20\Omega - \mu m / L_E$ $C_{be} = g_m \tau_f$, where $\tau_f = 0.5$ ps, $C_{CE} = 2\,fF/\mu m \cdot L_E$

<u>part a, 6 points</u>

The optimum load *admittance* is parallel combination of a conductance G and an inductive susceptance. Setting G to 40 milliSiemens, and setting the signal frequency to 100GHz, find (1) the appropriate HBT emitter length Le and (2) the required parallel load inductance L.

part b, 5 points

What is the maximum saturated output power ? What is the correct collector bias voltage and collector bias current ?

part c, 8 points

After impedance-matching on the amplifier input and output, what is the amplifier power gain ?