**ECE 145a /218A problem set 6a**
**Power amplifiers**

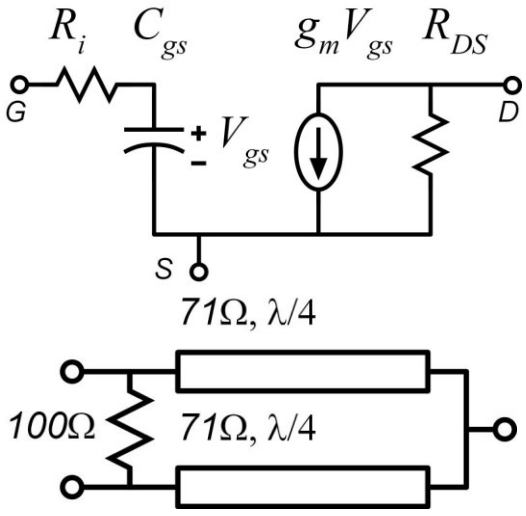
Problem 1:
The FET has a small-signal parameters as below, and large-signal parameters as given to the right.

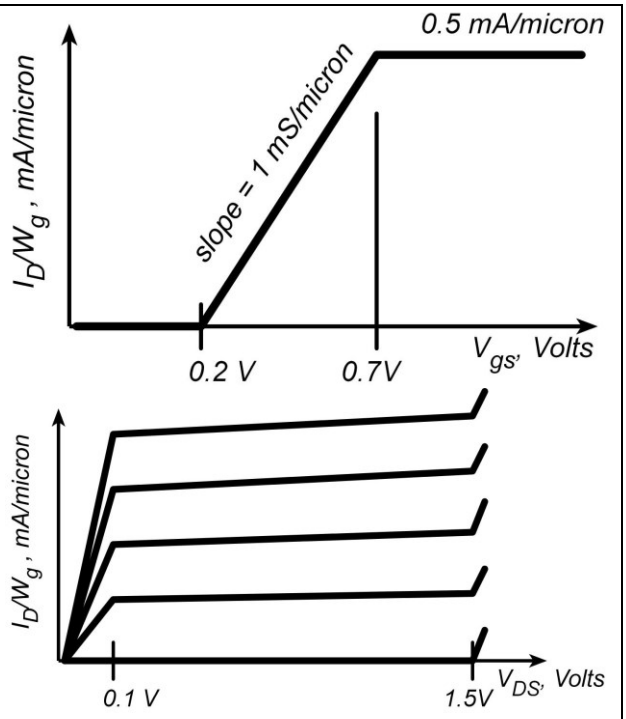
$g_m = 1.0mS/\mu m \cdot W_g \quad R_i = 1.0/g_m$

$C_{gd} = 0.0\,fF/\mu m \cdot W_g$

$C_{gs} = 1.5\,fF/\mu m \cdot W_g$

$G_{ds} = 0.1mS/\mu m \cdot W_g$




The maximum safe drain-source voltage is 1.1 Volts, and the maximum drain current is 1.5mA per micron of gate width Wg. The maximum gate width *for an individual FET finger* is 2 microns, if we wish to maintain the low input resistance Ri given above.

a) If we construct a multi-finger FET with *100* such fingers, each of 2 microns width, in parallel, find the overall gm, Ri, Cgs, Rds, of the device. What is the maximum drain current ? What are $f_\tau$ and $f_{\mathbf{max}}$ ?

b) For this 100-finger device, what is the optimum load impedance for maximum saturated output power ? Caution: you should *not* include the parallel loading of RDS in this calculation; this is a subtle point which arises because, in real FETs, RDS is bias-dependent and becomes infinite at zero drain current.

c) Ignoring RDS (setting it to infinity), and choosing a design frequency of $f_{\mathbf{max}}/10$, design a lumped LC matching network to match the input to 50 Ohms. Design a simple quarter-wave microstrip network to load the transistor with the optimum impedance

d) Under the above conditions, calculate by hand the maximum amplifier output power and its power gain. Hint: it is not necessary to know the element values of the matching network to do this.

e) Using Wilkinson Power-combiners, shown above, and *four* power amplifiers from

part (c), above, draw the schematic for a 4:1 corporate power-combined power amplifier. What would the total maximum saturated output power now ?