ECE145a / 218A lab project #4

Reactively Tuned Amplifier .
Mark Rodwell, 2009.

Your assignment is to design and construct a reactively tuned amplifier as diagramed in Figure 1. The transistor is to be an Avago AT-42035; I suggest biasing the device at Vce=8 Volts and Ic=10 mA. Please note that Avago is a recent spin-off of Agilent, in turn a spin-off of Hewlett-Packard; the part appears in the parts library of the 2009 version of ADS as a pb_HP_AT42035_19920721.

In Figure 1, resistors Rf, Rcc, and Rbx set the transistor DC bias current and DC collector-emitter voltage. Rbx and Rcc are isolated at RF using quarter-wave chokes. Rf is present for DC bias, but will degrade the transistor high-frequency gain, hence this resistor should be large (1 kOhm or more); more on this later. Reduction of the transistor gain by Rf can be avoided by isolating the resistor from the RF signal path (Figure 2). For this bias arrangement, the 2 supplies should be +15V and - 15 V. Clearly, if the matching networks use shunt lines to ground, the blocking capacitors must be placed between the transistor and the matching network.

The design sequence is as follows. The transistor must be DC-biased. From the S-parameters, the device stability at the design frequency is determined. One then adds resistive stabilization at the design frequency, in the form of either a series or shunt resistor at either the input or the output. Alternatively, a moderate-to-low value of Rf can provide this stabilization. Having stabilized the device, the input and output are matched to obtain the device maximum available gain.

The network analyzer, sampling oscilloscope, and spectrum analyzer all cost well above $20k, and all have easily-damaged inputs. To project these, you *must* use the input and output DC blocking capacitors, with a maximum value of 100 pF for each.

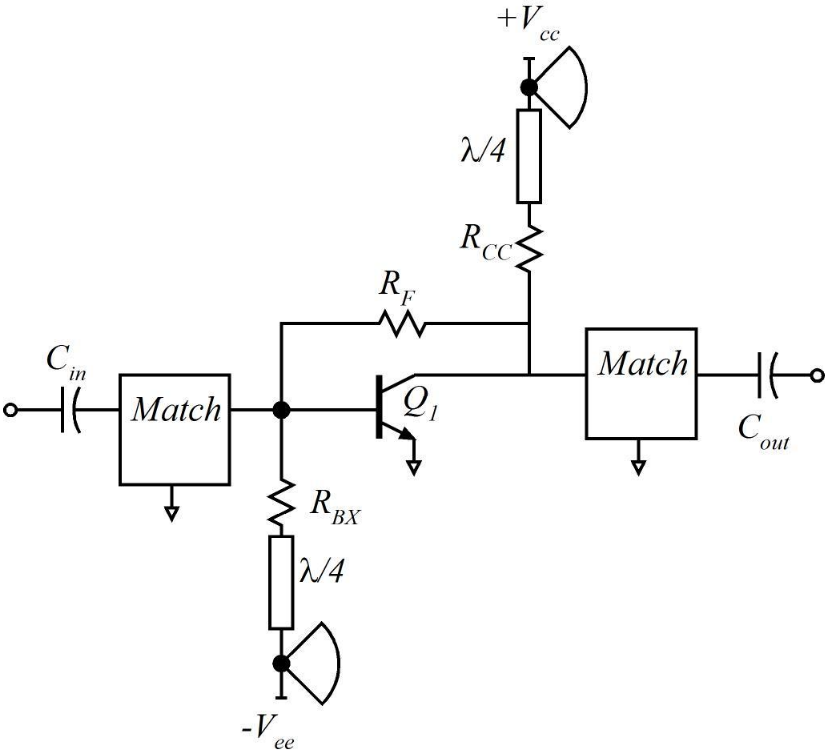

Figure 1: Common-emitter reactively-tuned amplifier (145a)

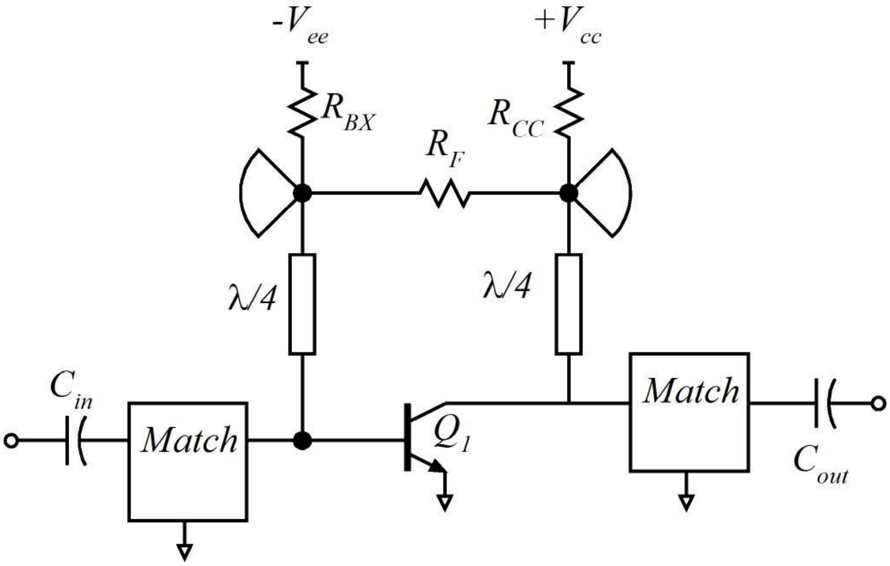

Figure 2: Alternate DC bias form avoiding RF loading of the transistor.

Assignment

Please do the following:

1) By hand design the DC bias circuit to force the desired combination of Ic and Vce in the transistor(s).

2) Enter the core circuit into Agilent ADS, without matching or stabilization and simulate the 4 S-parameters. Be sure to include all wires explicitly as microstrip elements. Examine the stability parameters K and B1, and the MAG/MSG. Picking a design frequency at or above 4 GHz, examine the stability circles at that frequency. Be warned that we have found more than one Model in ADS for the transistor, and that one of these does not work; please check with the TA.

3) From the stability circles, add resistive stabilization to over-stabilize the amplifier at the design frequency. Determine the maximum available gain after stabilization. Examine the Ga and Gp circles and from these determine the impedances to which the amplifier input and output must be tuned.

4) Design matching networks to tune the amplifier input and output. Add these to the circuit file.

5) Simulate the S-parameters from DC to 8 GHz and determine the frequencies at which the amplifier is potentially unstable. Add additional low-frequency stabilization to the circuit. Steps 3-4-5 may need to be iterated, particularly if your out-of-band stabilization reduces the in-band gain.

5a) Optional; 218A only. Simulate the noise figure circles and tune the input for best compromise between gain and noise figure.

6) Construct the amplifier on Duriod. Use *LEAD FREE* solder. Soldering to the ground plane will require a high-power iron, while the other components would be best soldered with a low-power unit. Measure the S parameters on the network analyzer. Make sure that the output power level from the network analyzer is not driving the amplifier into compression during this measurement[*]. Record and include in your report.

6) Adjust your matching networks as appropriate and re-measure.

7) Gain compression: Plot the Pout vs. Pin characteristic of the amplifier at the design frequency, and determine the input available power level at which the amplifier gain compresses by 1 dB. This is called the P_{1dB} input power and is a standard index for gain compression. You may use the network analyzer power sweep to do this, or use a frequency synthesizer (generator) as the signal source and a spectrum analyzer or power meter as the detector. If you use the generator and spectrum analyzer, first calibrate your measurement setup by evaluating the loss in the cables without the amplifier in the signal path. Then, you can correct your measured amplifier data for cable losses. Calculate by

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[*] Set the NA source power to around - 20 dBm. To do this: Menu --> Power --> use buttons/knob to set to - 20 dBm

hand the expected gain compression point (clipping limits being breakdown, saturation, and cutoff).

8) Optional: 218a only: Measure the noise figure using the noise source and spectrum analyzer.