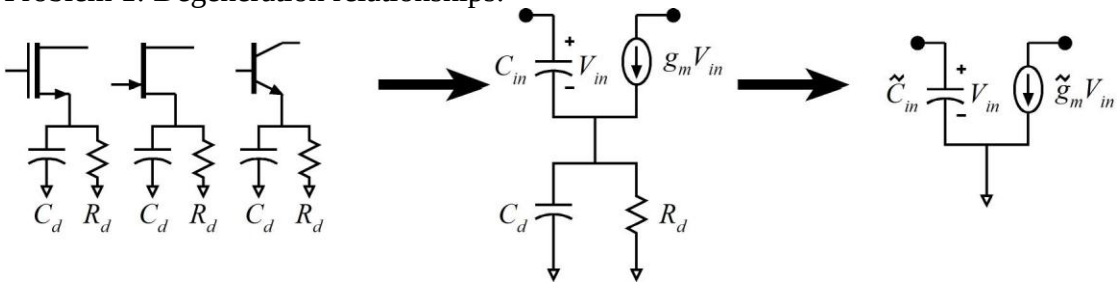
ECE 145a /218A problem set: resistive feedback amplifiers, device figures of merit, device power gains and cutoff frequencies.

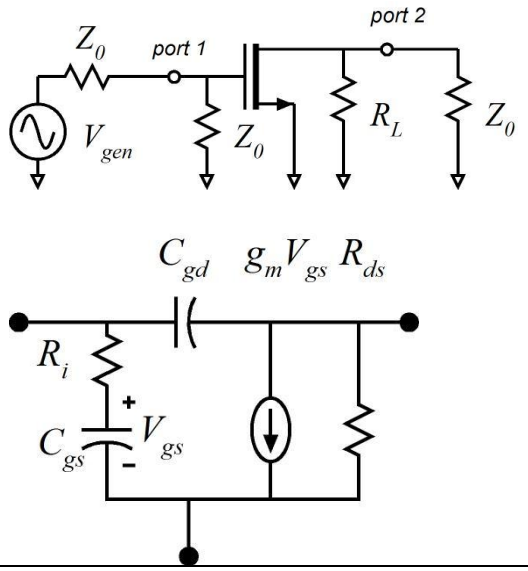
Problem 1: Degeneration relationships.



RC parallel emitter or source degeneration is used to reduce by equal amounts the device input capacitance and transconductance. Assuming that $C_d R_d = C_{in} / g_m$, compute the Y-parameters of the circuit in the center and the circuit to the right, showing that the 2 networks are equivalent if $\tilde{C}_{in} = C_{in} /(1 + g_m R_d)$ and $\tilde{g}_m = g_m /(1 + g_m R_d)$

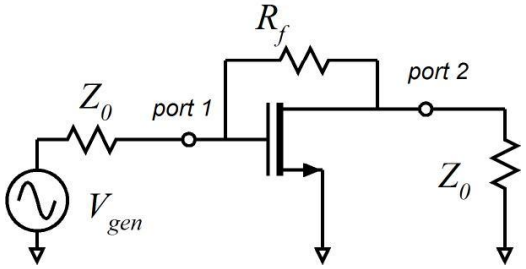
Problem 2: Analysis a simple resistively-loaded amplifier.
The device has the following parameters:
$g_m = 1mS / \mu m \cdot W_g \quad R_i = 0.5 / g_m$
$g_m R_{ds} = 25 \quad C_{gd} = 0\,\text{fF} \quad f_\tau$ =300 GHz.
In a 50 Ohm system, at low frequencies the amplifier is to have 10 dB insertion gain S21, and zero S11 and S22. Find the FET gate width W_g, and find R_L.

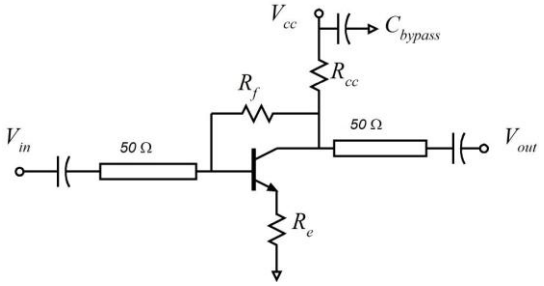
Find the -3 dB amplifier bandwidth



Problem 3: (218a only) compute the power-gain cutoff frequency of the transistor of problem 2. Even though we have not yet formally derived the quantity, you using elementary power-transfer concepts, you should be able to compute the maximum available power gain of the transistor at f=50 GHz.

Problem 4: Continuing to use the device model of problem 2. Determine the values of R_f and of W_g necessary for 10 dB insertion gain S21, and zero S11 at low frequencies. Neglect the effect of R_{ds} in your hand analysis. The compute the -3 dB bandwidth of S21. Hand analysis will be difficult unless you are



expert with MOTC or unless you neglect the effect of R_i ...please do so.	
Problem 5: Please enter the designs of Problems 2 and 4 on ADS, simulate, and generate dB magnitude plots of the S-parameters vs. frequency. Compare with hand analysis. Enter the elementary device model of problem 2 into ADS and plot the device maximum available gain and determine the power-gain cutoff frequency.	
Problem 6 (218a only). You will design and lay out a 50 Ohm, 10 dB amplifier block. Start with the design kit transistor of 0.5 by 8 microns emitter feature size. Using a 10 V supply, pick R_f from the feedback amplifier relationships, pick R_{cc} to bias the transistor at 2 mA. Add R_e as necessary to meet the amplifier design relationships. Simulate the 4 S-parameters.	 Generate a mask layout using the design kit. Unfortunately, the input/output blocking capacitors are not available in the design kit, so they cannot be included in the layout