

ECE 145a /218A problem set : Reactively matched amplifiers: mostly unilateral design.

<p>Background: Unilateral Device model. We will assume a highly simplified device model as to the right, with $g_m = 2mS / \mu m \cdot W_g$ $R_i = 1.0 / g_m$ $C_{gd} = 0 \text{ fF}$ $C_{gs} = 0.5 \text{ fF} / \mu m \cdot W_g$ $G_{ds} = 0.1mS / \mu m \cdot W_g$ Note that because of numerical problems in ADS, it may be necessary to add a nonzero C_{gd}; keep it small enough to not change the simulations !</p>	
<p>Background: Bilateral Device model. $g_m = 2mS / \mu m \cdot W_g$ $R_i = 1.0 / g_m$ $C_{gd} = 0.1 \text{ fF} / \mu m \cdot W_g$ $C_{gs} = 0.5 \text{ fF} / \mu m \cdot W_g$ $G_{ds} = 0.1mS / \mu m \cdot W_g$</p>	
<p>Problem 1: For the unilateral device model, compute by hand the maximum available power gain and the short-circuit current gain as a function of frequency.</p>	
<p>Problem 2: For a 50 Ohm generator and load, at a frequency of 50 GHz, and taking $W_g = 100$ microns for the unilateral device model, calculate the following by hand: insertion power gain, operating power gain, available power gain, maximum available power gain. Simulate these in ADS and compare with hand calculations.</p>	
<p>Problem 3: Using ideal L-C matching networks, design an amplifier for operation at 10 GHz signal frequency. Use ADS. Give dB plots of all 4 s-parameters vs. Frequency. Make a plot comparing the transistor MAG to the amplifier S21</p>	
<p>Problem 4: Take the bilateral device at 100 microns gate width. Calculate by hand ft and fmax. Plot the device MAG/MSG, U, and H21 vs frequency and compare the device fmax to hand calculations.</p>	
<p>Problem 5: Plot the stability factor K and B1 for the device of problem 4 vs frequency. At what frequencies is the device unconditionally stable ? At a design frequency of 50 GHz, what is the maximum stable gain ? Calculate this by hand and then simulate in ADS.</p>	
<p>Problem 6: Plot the device source and load stability circles at 100 GHz. What value of series resistance on the input would stabilize the device ? What parallel input resistance ? Repeat for the output.</p>	

Problem 7: Add series stabilization on the input so that the stabilized MAG is 2 dB less than the transistor MSG at 50 GHz. Plot the input and output Ga and Gp circles at 50 GHz. Design matching networks at 50 GHz. Plot all 4 S-parameters vs frequency, and compare the peak S21 obtained to the transistor MSG.