

**ECE 145a /218A problem set:**

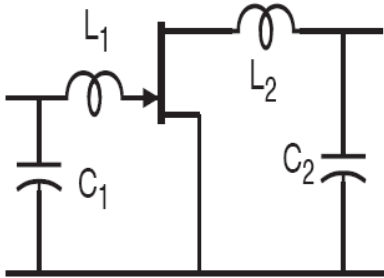
**Reactively matched amplifiers: mostly bilateral design.**

<p>Background: Unilateral Device model.          We will assume a highly simplified device model as to the right, with  <math>g_m = 2mS / \mu m \cdot W_g</math>   <math>R_i = 1.0 / g_m</math>  <math>C_{gd} = 0 \text{ fF}</math>  <math>C_{gs} = 0.5 \text{ fF} / \mu m \cdot W_g</math>  <math>G_{ds} = 0.1mS / \mu m \cdot W_g</math></p>	
<p>Background: Bilateral Device model.  <math>g_m = 2mS / \mu m \cdot W_g</math>   <math>R_i = 1.0 / g_m</math>  <math>C_{gd} = 0.1 \text{ fF} / \mu m \cdot W_g</math>  <math>C_{gs} = 0.5 \text{ fF} / \mu m \cdot W_g</math>  <math>G_{ds} = 0.1mS / \mu m \cdot W_g</math></p>	
<p>Problem 1a: Taking <math>W_g = 100</math> microns for the bilateral device model, Plot the MAG/MSG stability factor K and B1 for the device of problem 1 vs frequency. At what frequencies is the device unconditionally stable ? At a design frequency of 50 GHz, what is the maximum stable gain ? Calculate this by hand (!) and then compare to the ADS simulation.</p>	
<p>Problem 1b: Plot the device source and load stability circles at 50 GHz. What value of series resistance on the input would stabilize the device ? What parallel input resistance ? Repeat for the output.</p>	
<p>Problem 1c: Add series stabilization on the input so that the stabilized MAG is 2 dB less than the transistor MSG at 50 GHz. Plot the input and output Ga and Gp circles at 50 GHz. Design matching networks at 50 GHz. Plot all 4 S-parameters vs frequency, and compare the peak S21 obtained to the transistor MSG.</p>	
<p>Problem 2a: At a design frequency of 10 GHz, a transistor has  <math>S_{11}=0.5</math>, <math>S_{21}=4</math> <math>S_{22}=0.8</math> <math>S_{12}=0</math>          All defined for a reference 50 Ohm system impedance.          Find the transistor's maximum available gain at this frequency.</p>	
<p>Problem 2 b: The generator impedance is 10 Ohm , while the load impedance is 100 Ohm. Find the following: the transducer power gain Gt, the available power gain Ga, the operating power gain Gp</p>	
<p>Problem 2 c: The generator impedance is 10½, while the load impedance is 100½.</p>	

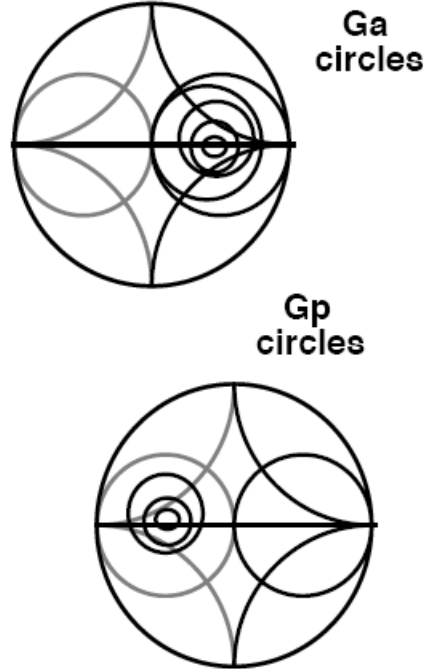
If the power available from the generator is 1 mW, what is the load power?	
Problem 2 d: If we placed an impedance-matching network between the generator and the transistor, but not between the transistor and the load, what would the load power be?	
Problem 2e: If the generator and load were instead both 50 Ohms, there were no matching networks, and there was 1 mW available from the generator, what would the load power be?	
<p>Problem 3a:  <math> S_{11}  &lt; 1</math>, <math> S_{22}  &lt; 1</math>          Above are shown the stability circles for a common-source-connected FET at 10 GHz. The transistor can be stabilized by either shunt or series stabilization at either the Input or the output.          Draw circuit diagrams, with exact component values given, for 2 stabilization methods.</p>	
Problem 3b: It so happens that the transistor itself has $S_{21} = 3 + j4$ , and $S_{12} = 0.7 + j0.7$ . The transistor $S_{11}$ and $S_{22}$ are not given, but the transistor is potentially unstable. After stabilization, and impedance matching on input and output, what is the transducer power gain obtained from the (stabilized and matched) transistor?	
<p>Problem 4: Here are <math>G_A</math> and <math>G_P</math> circles for a transistor, at 1 dB increments in Gain (50 Ohms impedance standard for the impedance charts). The transistor maximum available gain is 10 dB. If the input is impedance matched to the transistor, but the load impedance is 50 Ohm, what is the transistor transducer power gain?</p>	<p>(the solid black dots are the impedances for maximum gain, not 1-dB contours)</p>
<p>Problem 6: An amplifier (<math>S_a</math>) has <math>S_{a11} = 0.2</math>, <math>S_{a22} = 0.3</math>, <math>S_{a21} = 5</math>, <math>S_{a12} = 0.1</math>. 50 Ohm resistors are connected to ground on the input and output, thus. Find <math>S_{b21}</math> of the overall network.</p>	

**Problem 7:**

Ga and Gp circles for the transistor are shown at left (10 GHz). The center of the Ga circles is  $G=+0.5$ , and the center of the Gp circles is  $G=-0.25$ .



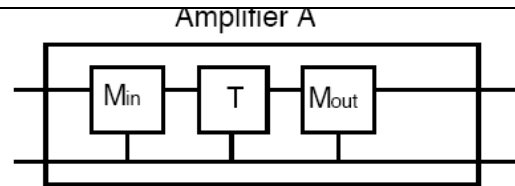
Using the Smith chart, find the values of the components required to Match the amplifier to a  $50\Omega$  system at 5 GHz.



**Problem 8:**

An transistor (St) has  $S_{11}=0.5$ ,  $S_{22}=0.25$ ,  $S_{21}=10$ ,  $S_{12}=0$ , given a 50 ohm impedance definition. The generator is 25 ohms, the load is 75 ohms. Impedance-matching networks are connected to the amplifier input and output, creating an amplifier A.

a) Find the MAGNITUDES of the 4 S-parameters of the amplifier A

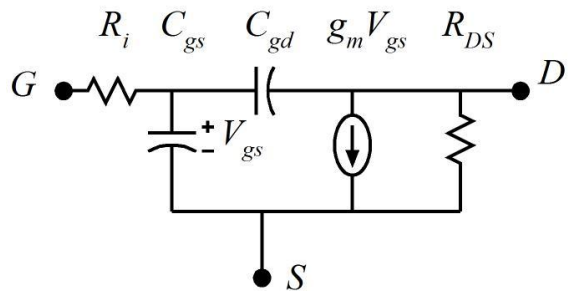


b) Find the transducer power gain of the amplifier given that the generator is 25 ohms and the load is 75 ohms.

c) Find the transducer power gain of the amplifier if connected to a 50 Ohm generator and load.

**Problem 9:** The transistor at right has 1000 mS/mm transconductance,  $R_i=1/g_m$ ,  $C_{gd}=0$  fF, a 160 GHz current gain cutoff frequency and a 250 GHz power gain cutoff frequency. The parameters above are obtained with  $V_{ds}=0.5$  V and  $V_{gs}=0.5$  Volts.

It is desired to have an amplifier with 15 dB gain and 100 GHz bandwidth at the 3-dB-point. You will use resistive feedback amplifiers, probably several cascaded stages



. Design such a amplifier, showing your calculations for all relevant parameters, and give a full circuit diagram.