

ECE145a/218a:

Exercise in Running the Simulation Tools and Introductory Circuits

The exercises below are designed to **complement** your running the ADS tutorials (in ADS documentation), which are highly recommended.

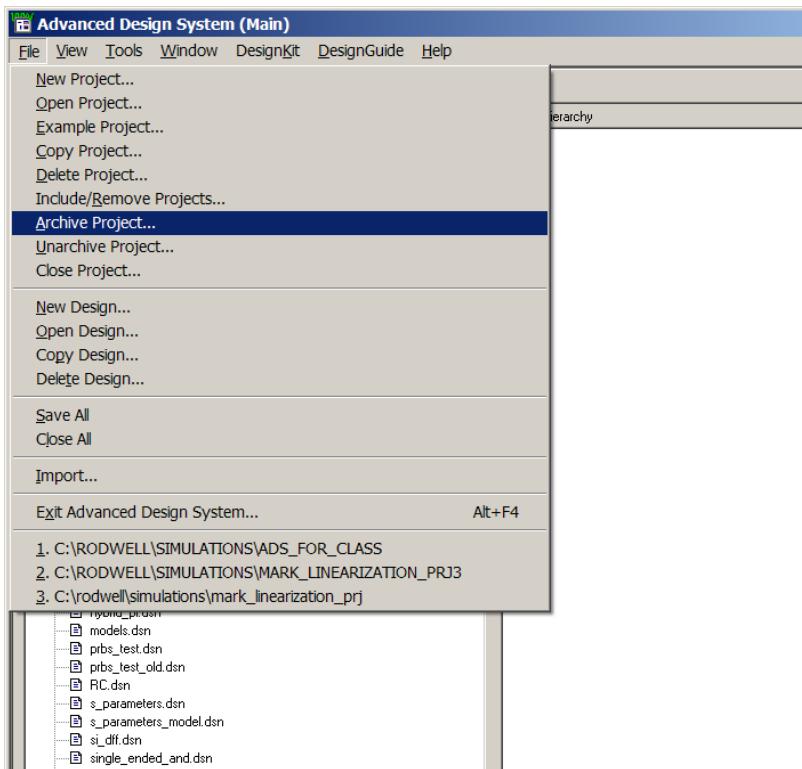
FIRST: MECHANICS OF ACCESSING THE PROGRAM.....	2
DOWNLOADING THE ADS PROJECT DIRECTORY	2
EXAMPLES OF ADS SIMULATIONS:.....	2
BASIC S-PARAMETER SIMULATION	5
MODELING BIPOLAR TRANSISTORS:	15
SPICE MODEL.....	15
SUBCIRCUIT MODEL WITH SPICE MODEL WITHIN.....	15
S-PARAMETER DATA FILE	22
SMALL-SIGNAL MODELS	22
INTERCONNECTS	24
UCSB HBT IC PROCESS CROSS-SECTION	24
INTERCONNECT MODELS (ROUGHLY).....	25
COMMENT: ADS MOMENTUM	27

First: Mechanics of Accessing the program.

I have set up some example ADS directories to aid in getting the tools running quickly.

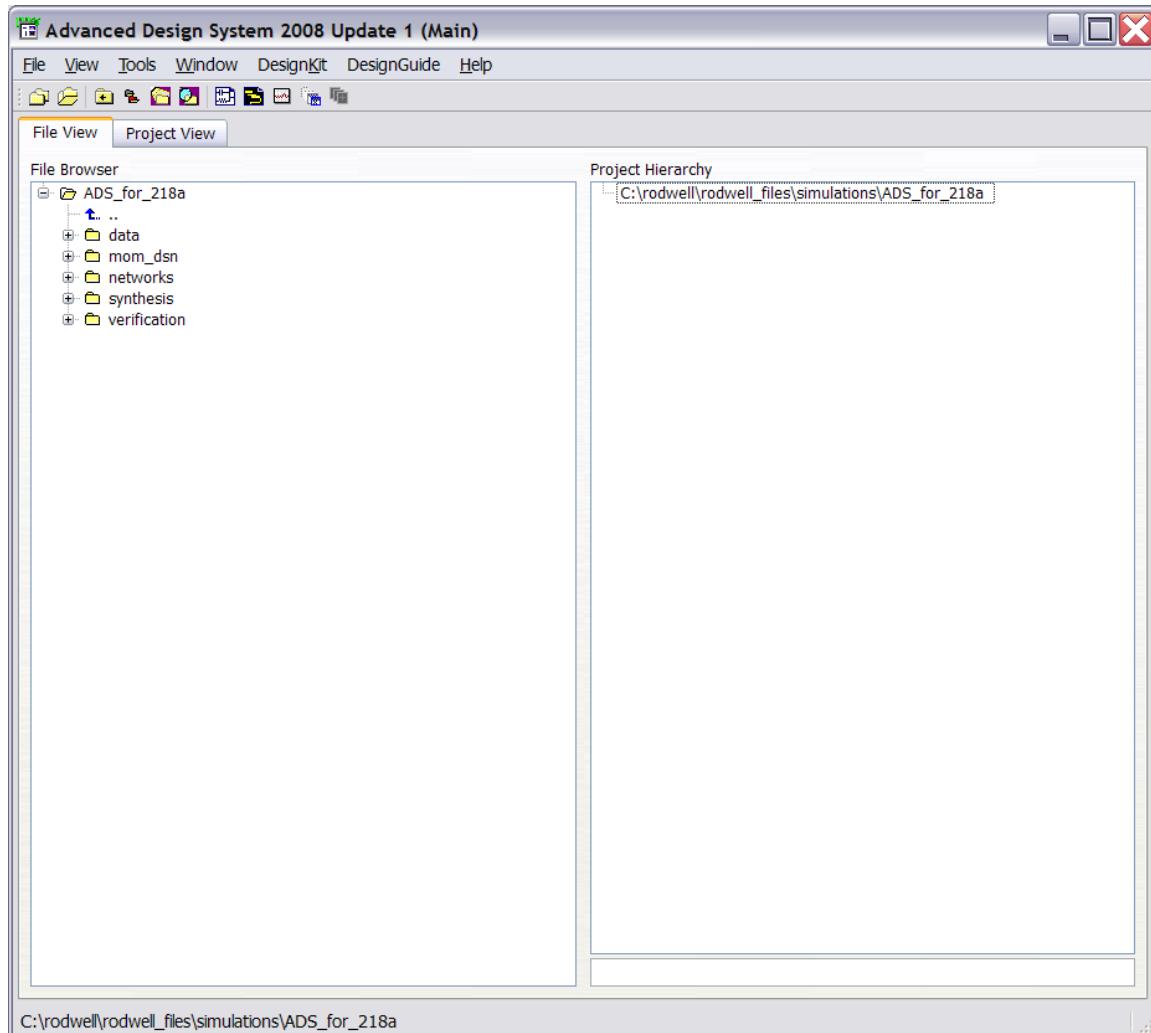
Downloading the ADS project directory

On my web page will be a compressed ADS project directory. This is in a ZAPPED format, which sounds like, but is not, a Zipped format. Download it using a web browser (save to disc) and then *unarchive project* to decompress it:



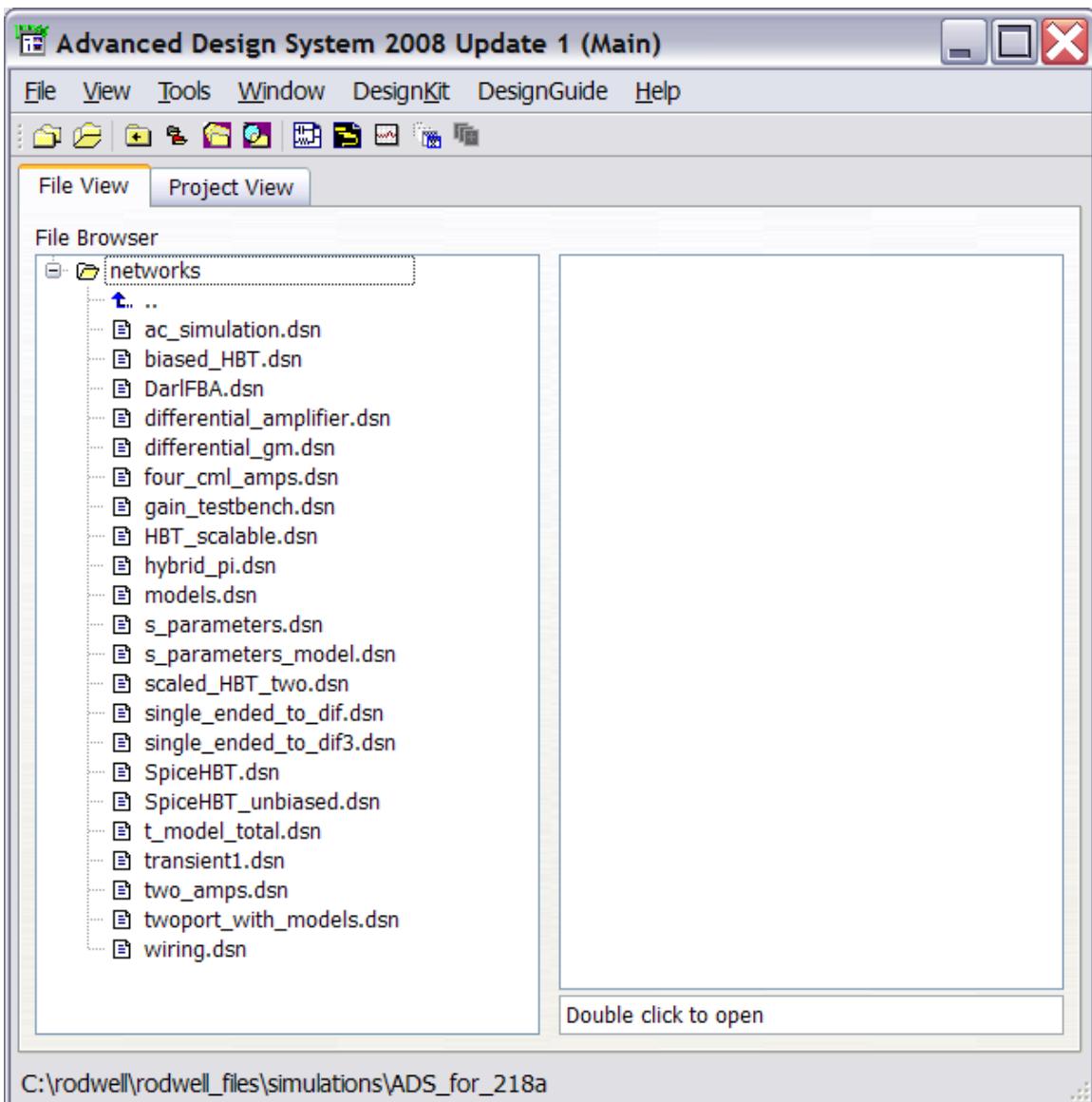
Examples of ADS simulations:

Download the project, Unarchive it as illustrated above, and open it. You should then see the following:



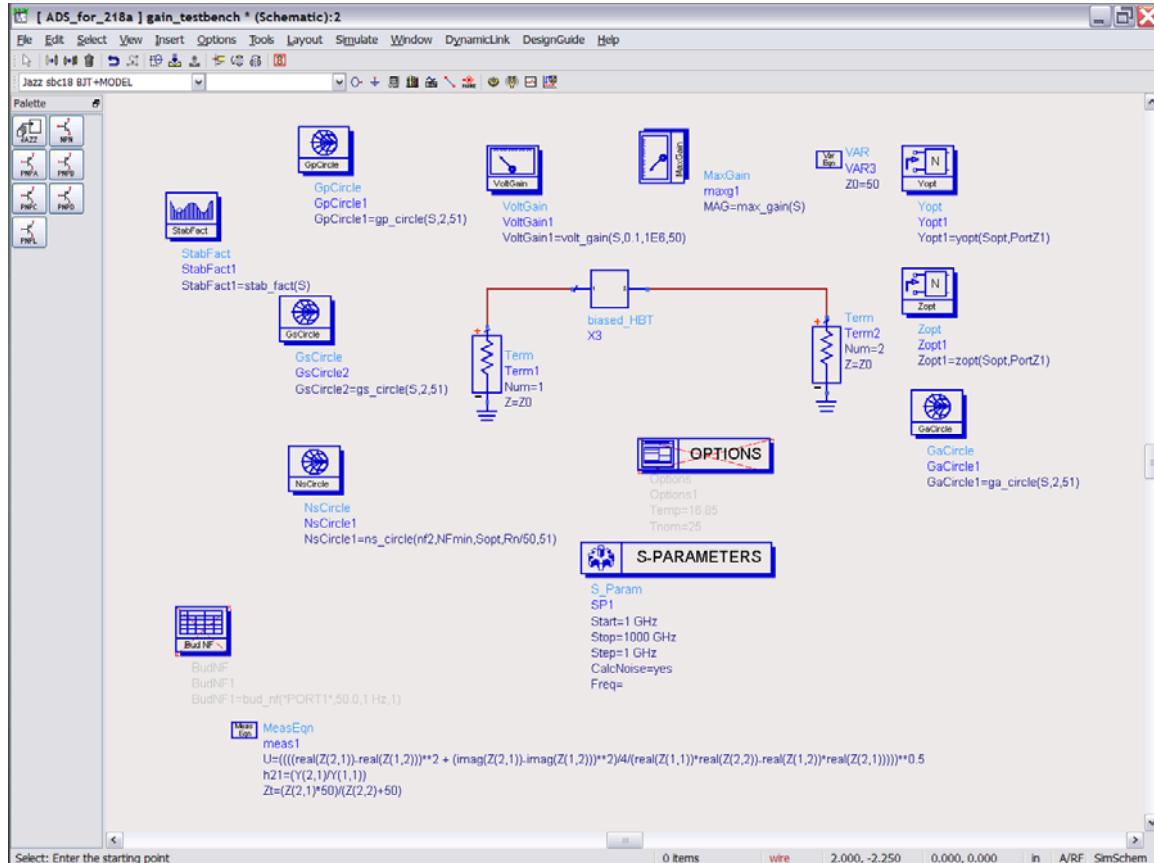
...you can open schematic editor window, by clicking on the button which looks like a schematic....but you may not need to: often the program opens itself in the state it was last saved.

You can expand the file browser window to see available circuits (I have given you lots):



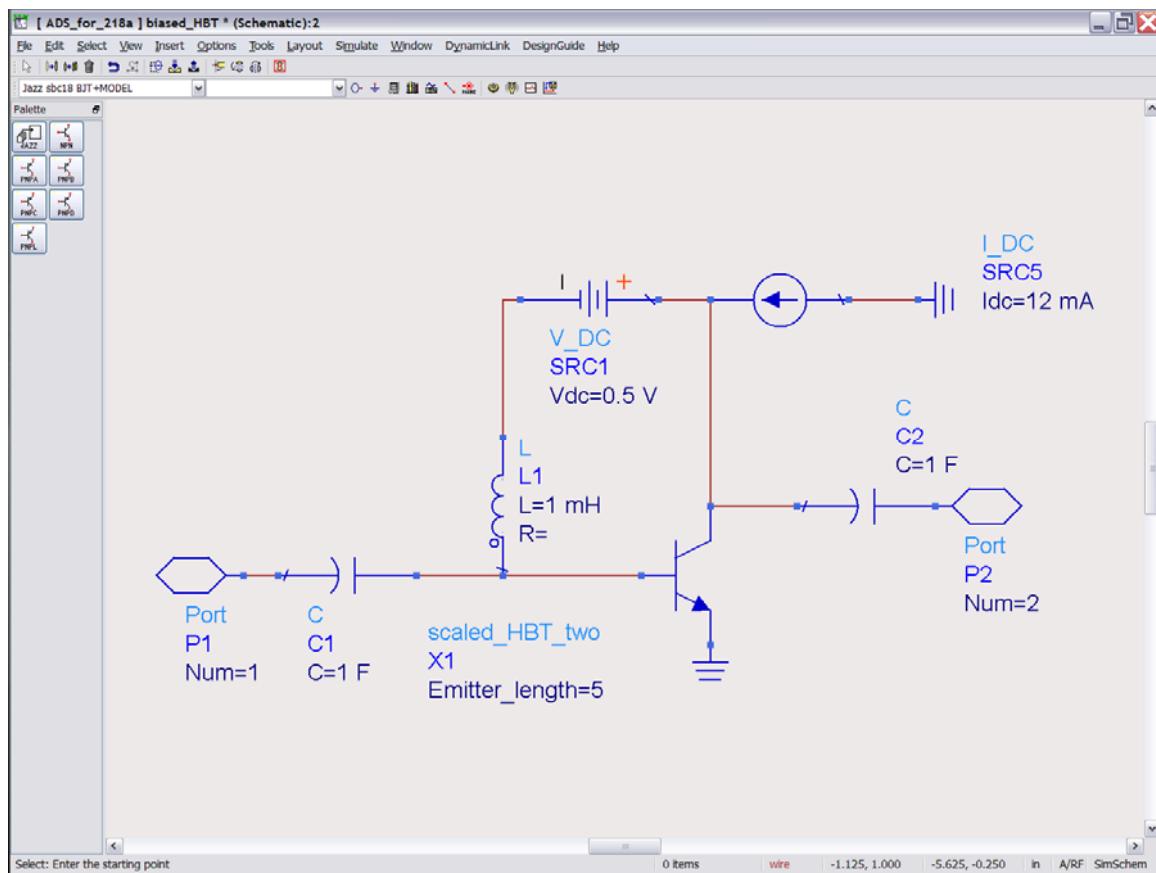
Basic S-parameter Simulation with bias-dependent model

Open up the file gain_testbench which I have created to calculate S-parameters:

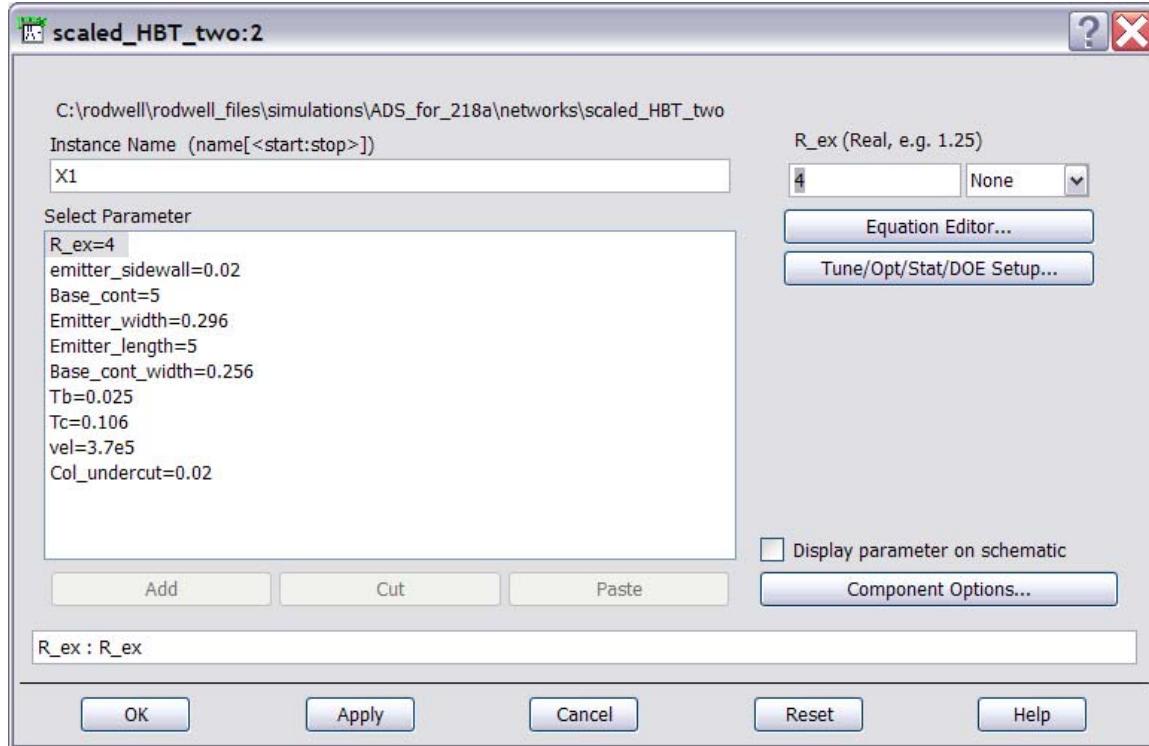


This will test for S-parameters of the subcircuit "biased_HBT". You can type the name of other subcircuits there to test them instead.

You will see a "down arrow" button which is used to pop into the network hierarchy. Click on it, then on the subcircuit to move into the hierarchy.



IMPORTANT: select the transistor, and double click on it and make sure that the following model parameters are set for *all* devices which you use in your circuit (only the emitter length should change):



In this list

Rex = 4 Ohm-micron² is the parasitic emitter resistance per unit area

emitter_sidewall=0.02 micron is the emitter sidewall thickness

base_cont= 5 Ohm-micron² is the base contact resistance per unit base contact area

emitter width=0.296 is the emitter junction width*

*the physical emitter junction width is $0.296 - 2 \times (\text{emitter sidewall}) = 0.256$ um
emitter length, the emitter length in microns.

base_cont_width=0.256 micron is the base contact width

Tb=0.025 is the base thickness in microns

Tc=0.106 is the collector depletion layer thickness in microns

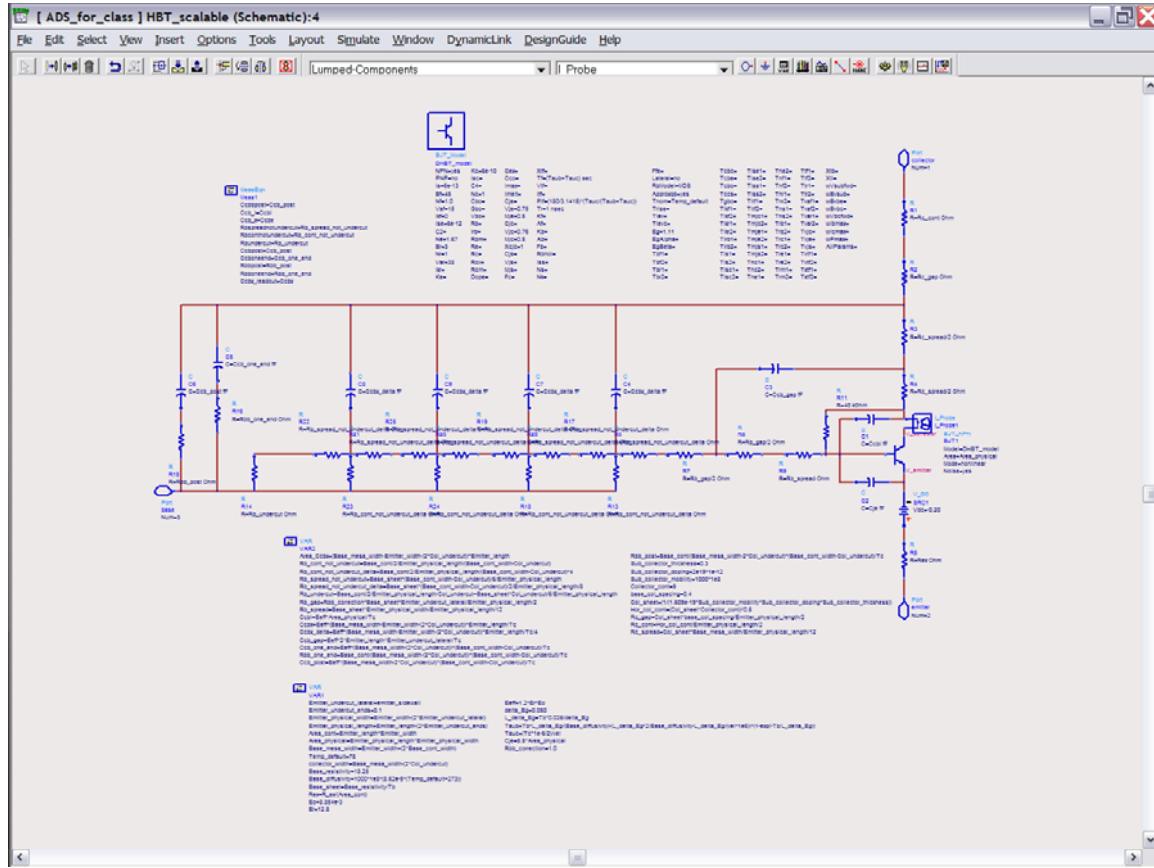
vel=3.7e5 is the collector electron saturation drift velocity in m/s

Col_underscoreut =0.02 micron is the base-collector junction undercut
 the width of the base-collector

In all of your circuits, **all** of the parameters should be set to the above values, except the emitter length Le, which you may set to 1, 2 , 4, or 8 microns. For convenience, and clarity in the circuit diagram, only the emitter length is shown by default. This has the danger that you may be inadvertently setting these transistor parameters to undesired values !

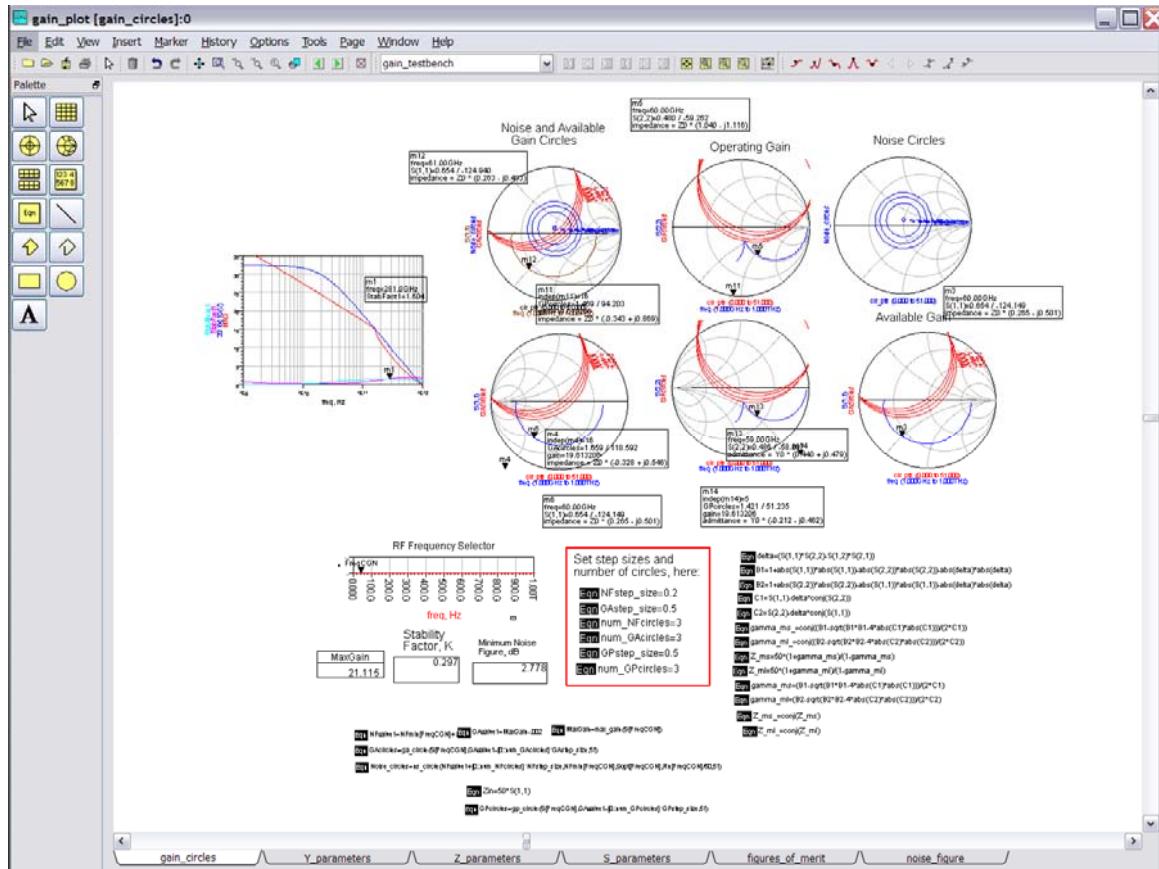
*The device has a maximum operating current of $\sim 3\text{mA}/\text{micron} * Le$, and a maximum power dissipation of about $4 \text{mW}/\text{micron} * Le$*

If you pop into the transistor:



The transistor is defined as a SPICE model (DHBT model), with external parasitic resistances and capacitances which we have defined through equations from the transistor geometry. We do this at UCSB because it allows us to make fairly accurate predictions of performance of future transistors which we may not yet have built.

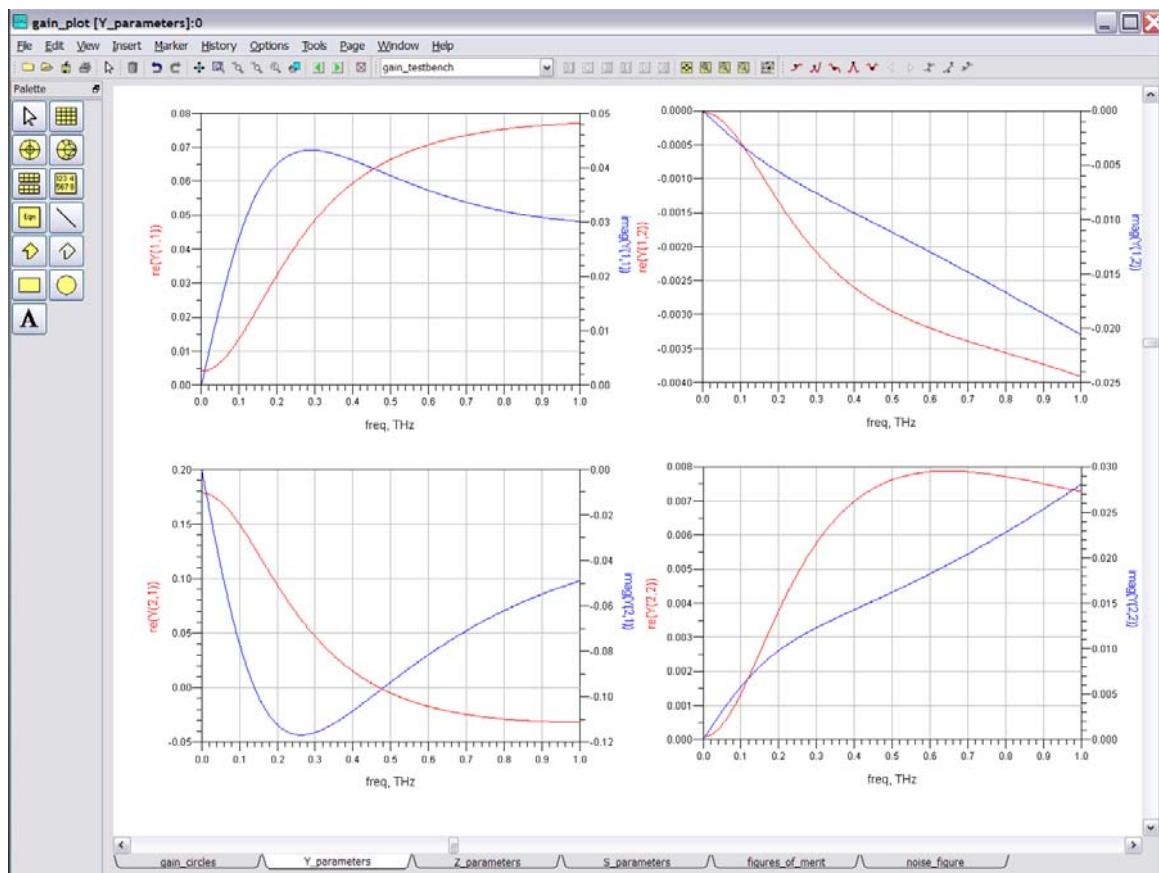
Now pop back up to the top level in the hierarchy and then "Simulate" , and (if it does not happen automatically), open up a plot of results (window→open data display→ "gain_testbench") to open up a set of plots I have pre-created:

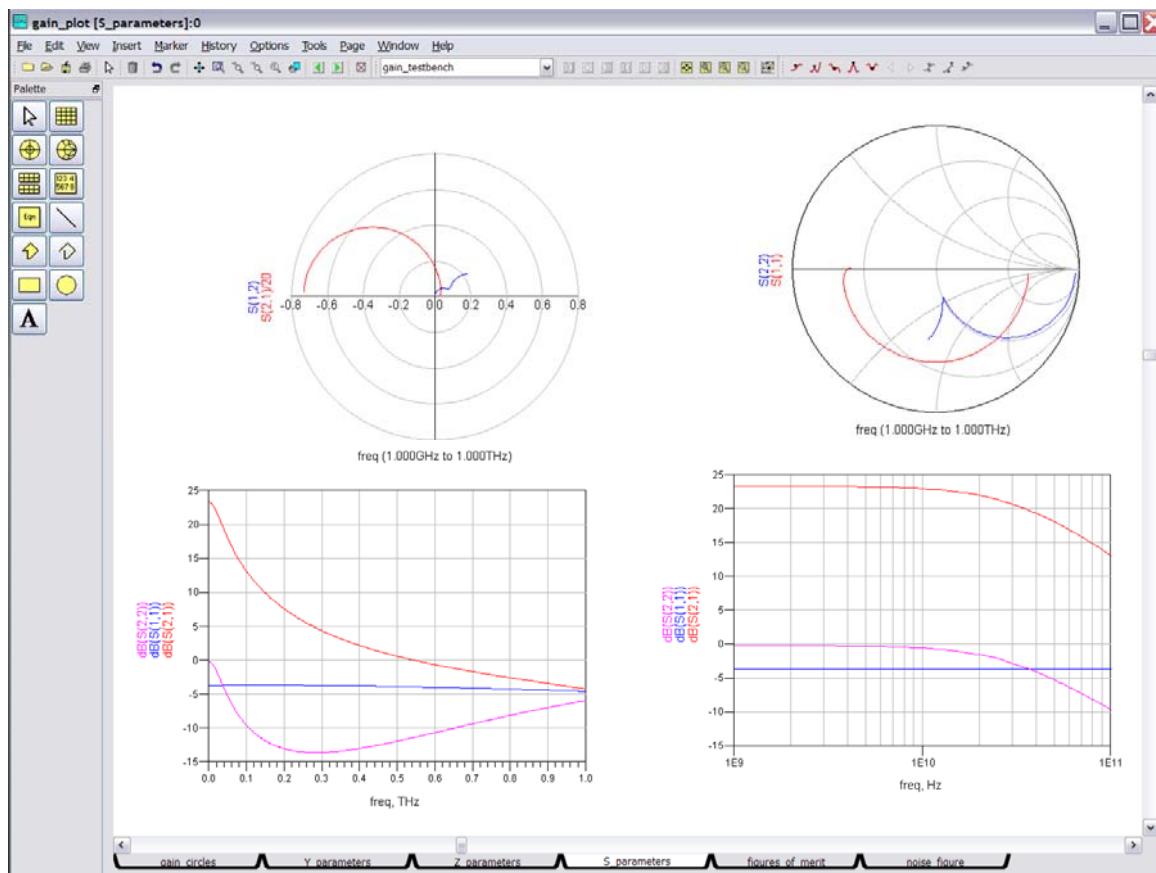


Note the series of tabs across the bottom. Which allows you to change views:

The gain circles plots we will use in detail (later) to design tuned amplifiers.

There are dB and polar plots of S-parameters, and plots of H21 and U (relevant for transistors, no relevant for the IC). There are also noise figure circles and gain circles, which are relevant to microwave tuned amplifier design. There are also plots of Y and Z and S parameters, and plots of open-circuit voltage gains, etc.

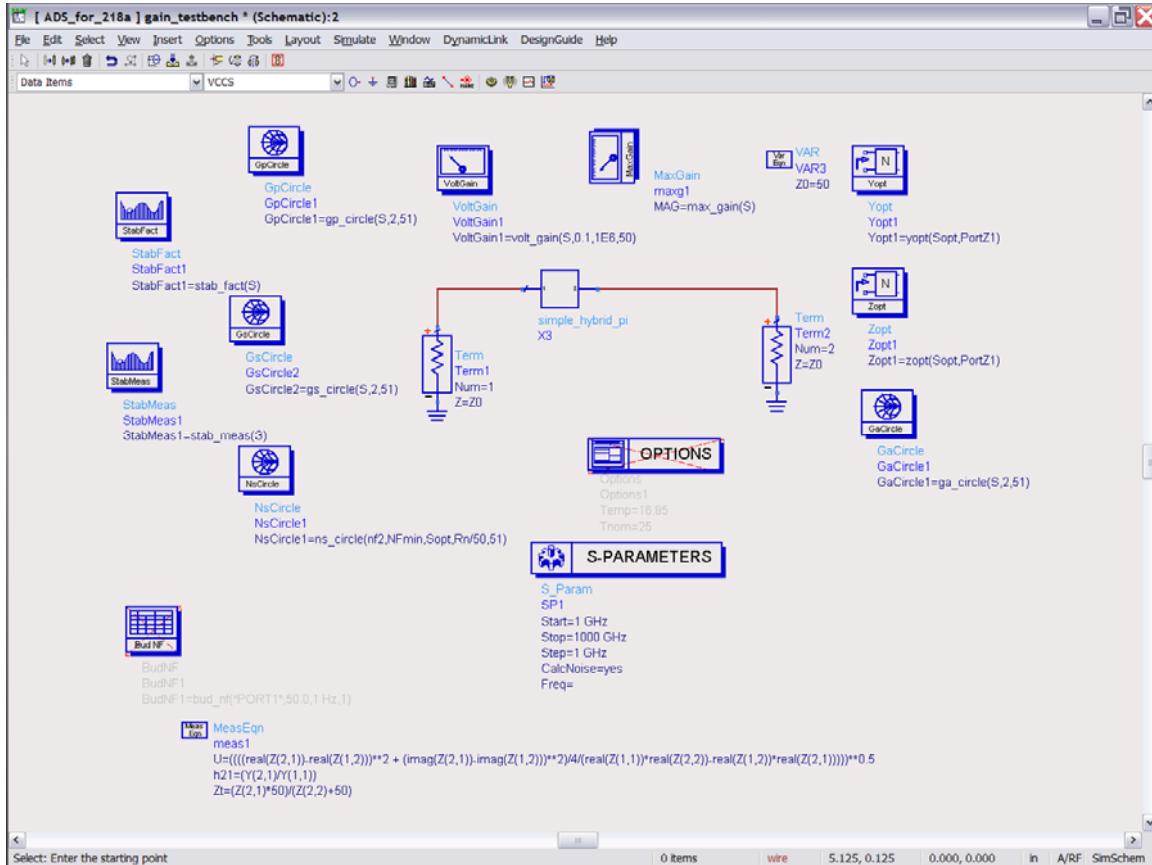




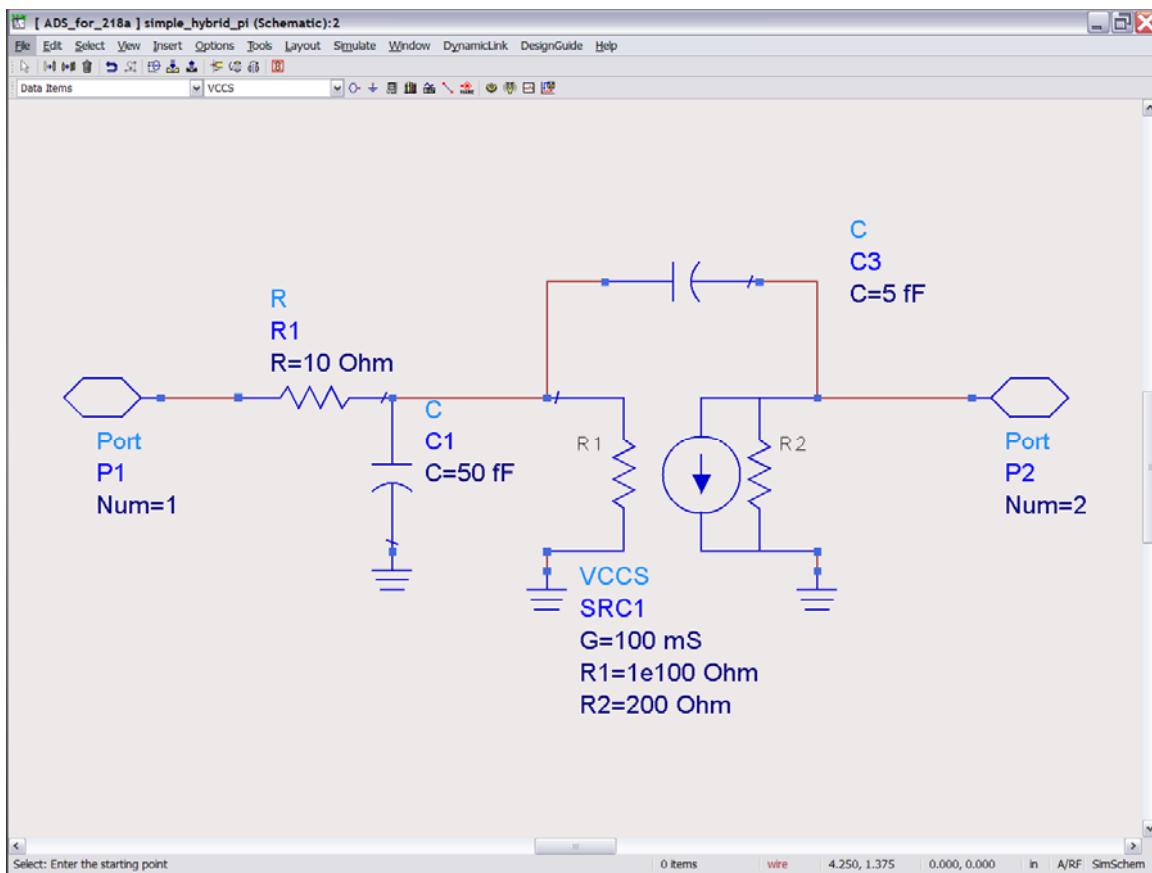
Click on the toolbar on the left-hand side, and you can add other plots.

Simulation with a hybrid_pi model

change the name of the DUT to simple_hybrid_pi



click into the circuit to take a look:



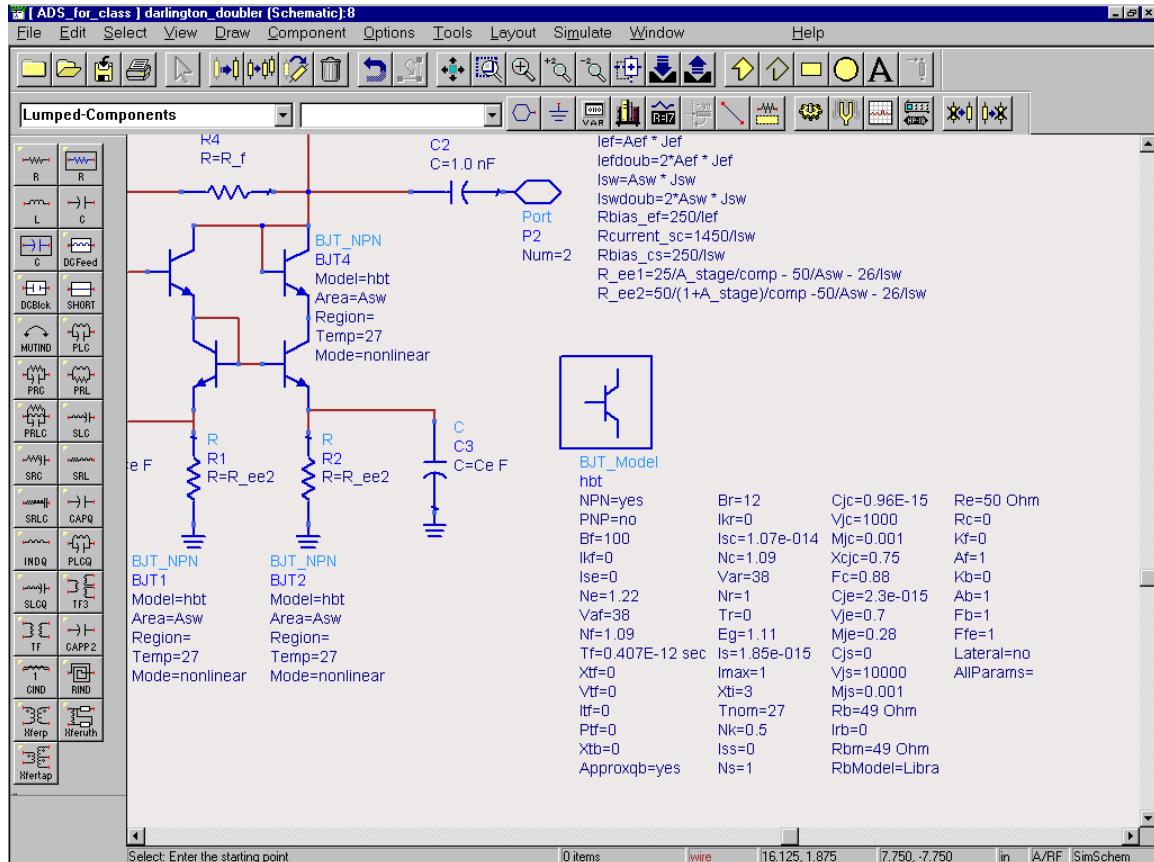
This is a simple hybrid pi model of a bipolar or field effect transistor.

Pop back out of the hierarchy and you can simulate to compute its S and Y parameters and other relevant network parameters.

Modeling Bipolar Transistors:

We can do this several ways:

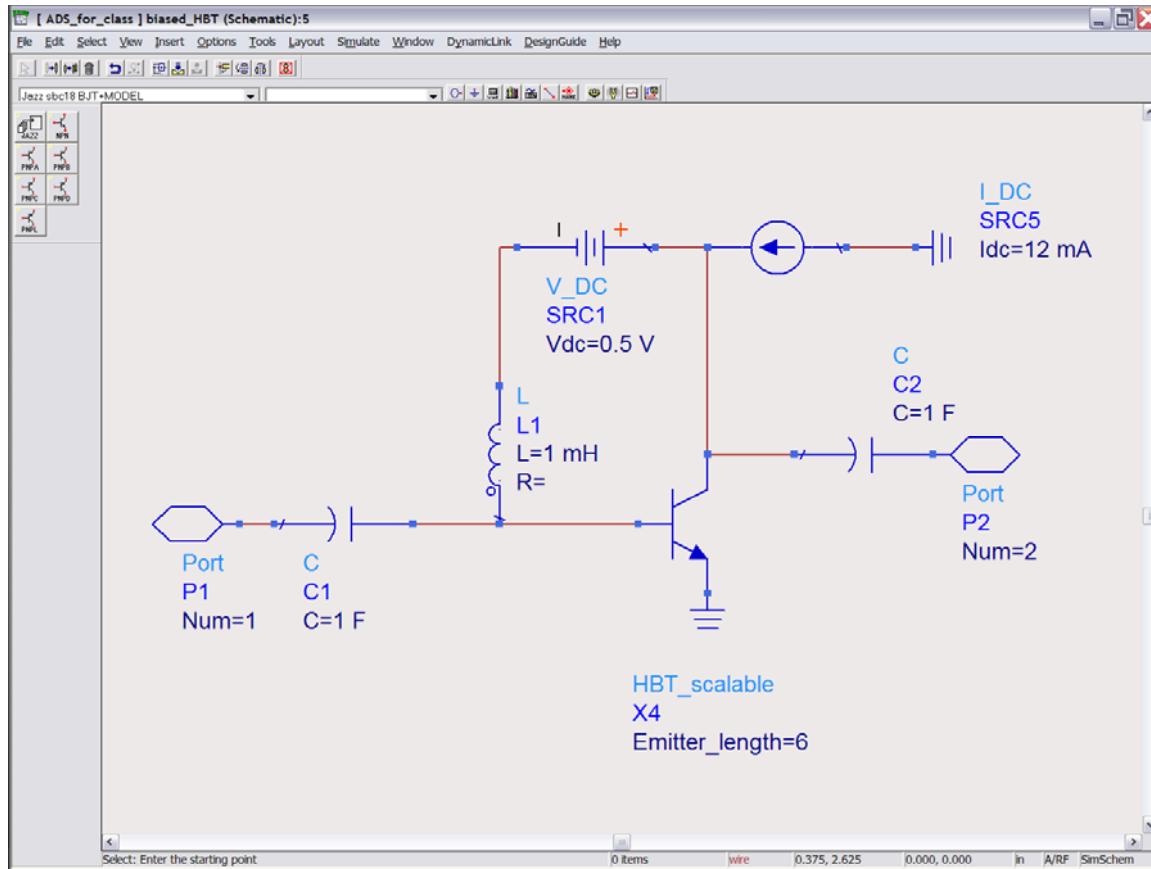
Spice MODEL



We have a model file, BJT_MODEL, which we then invoke with an area statement. This is a large signal model which defaults to a small signal model (with bias-dependent parameters) when we do a S-parameter simulation.

Subcircuit model with SPICE MODEL within

Here is a circuit (HBT under test)



HBT_scalable is a subcircuit with PASSED parameters

Rex is the emitter resistance per unit area,

base_cont is the base contact resistivity in ohm-micron²,

emitter width and emitter length are the length and width of the emitter in microns,

base_cont_width is the base contact width in microns

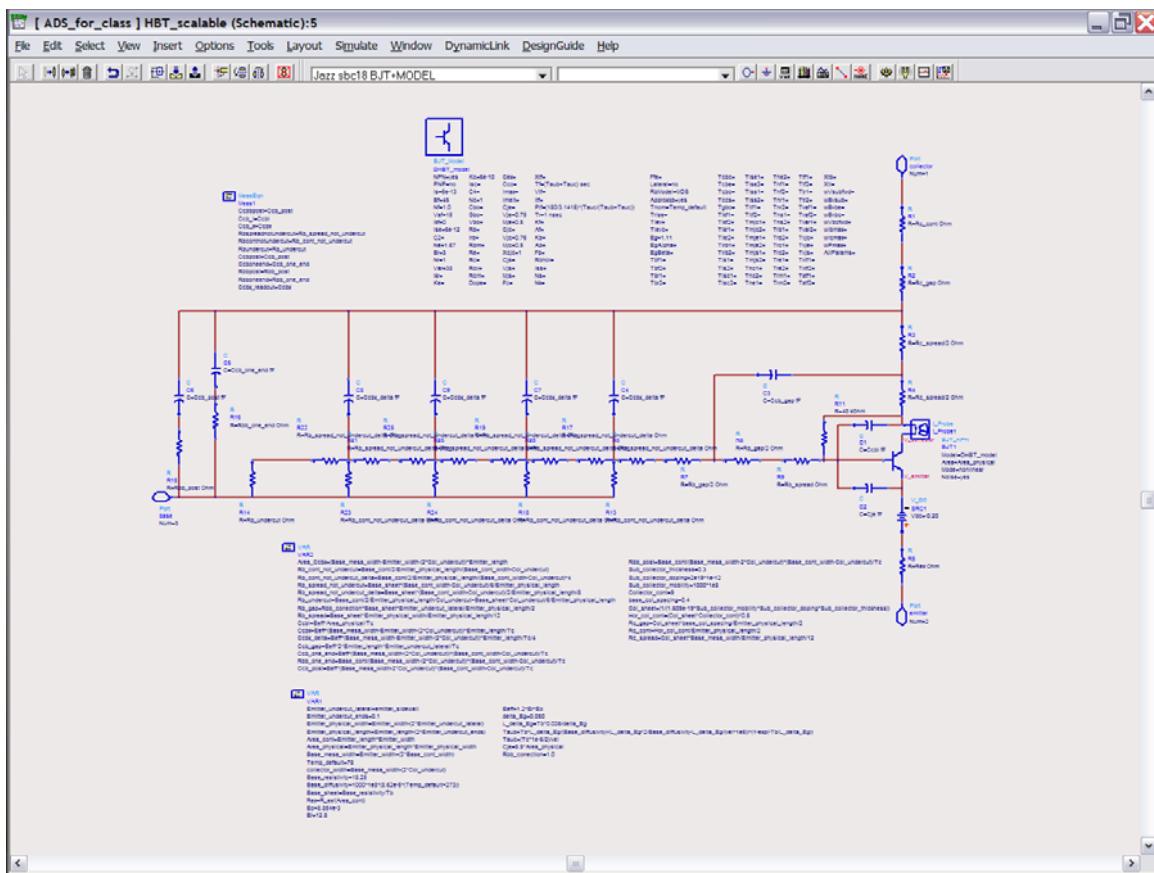
Tb is the base thickness in microns

Tc is the collector thickness in microns.

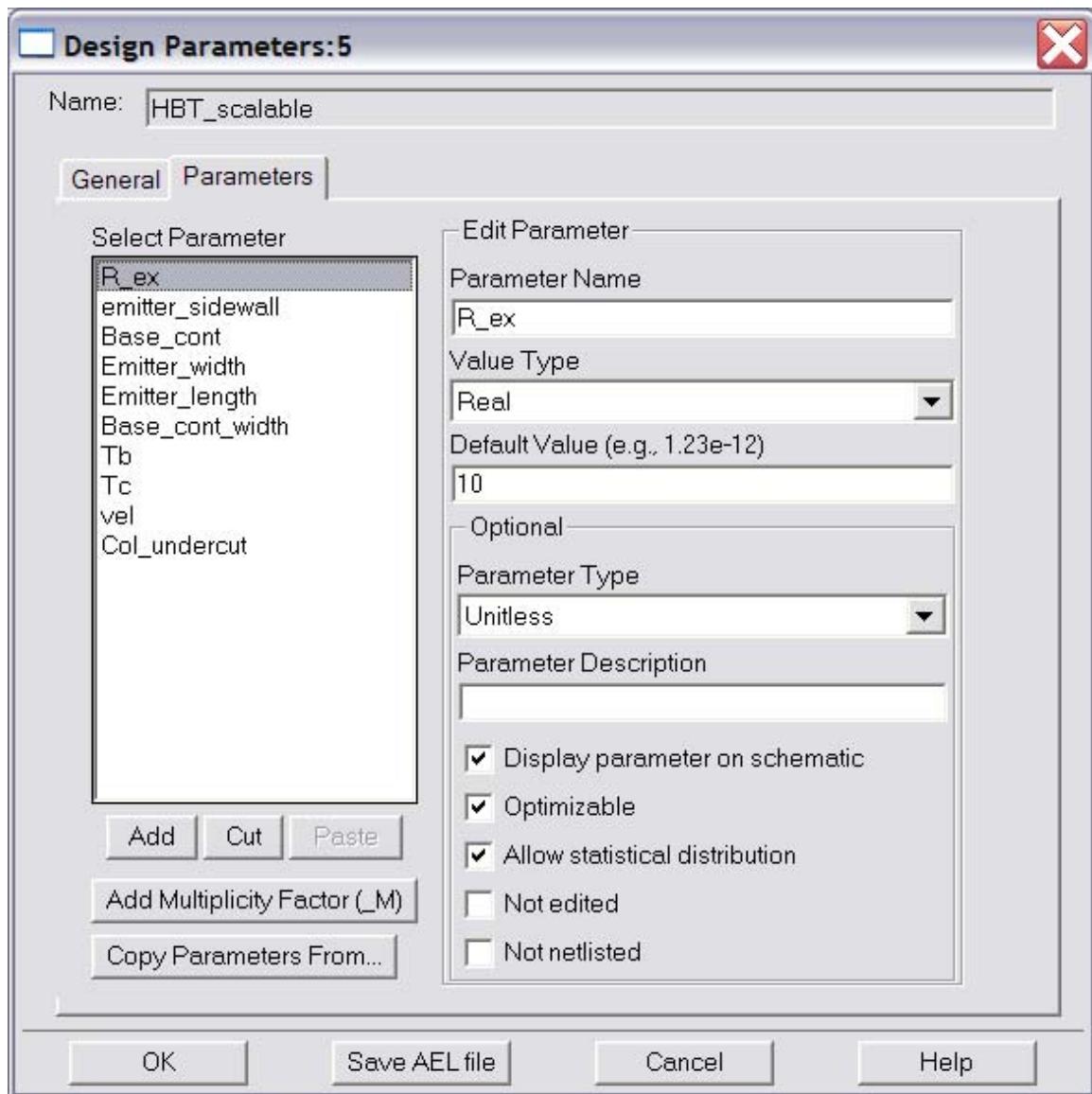
vel is the collector electron velocity

col_underscore is the undercut under the base contacts.

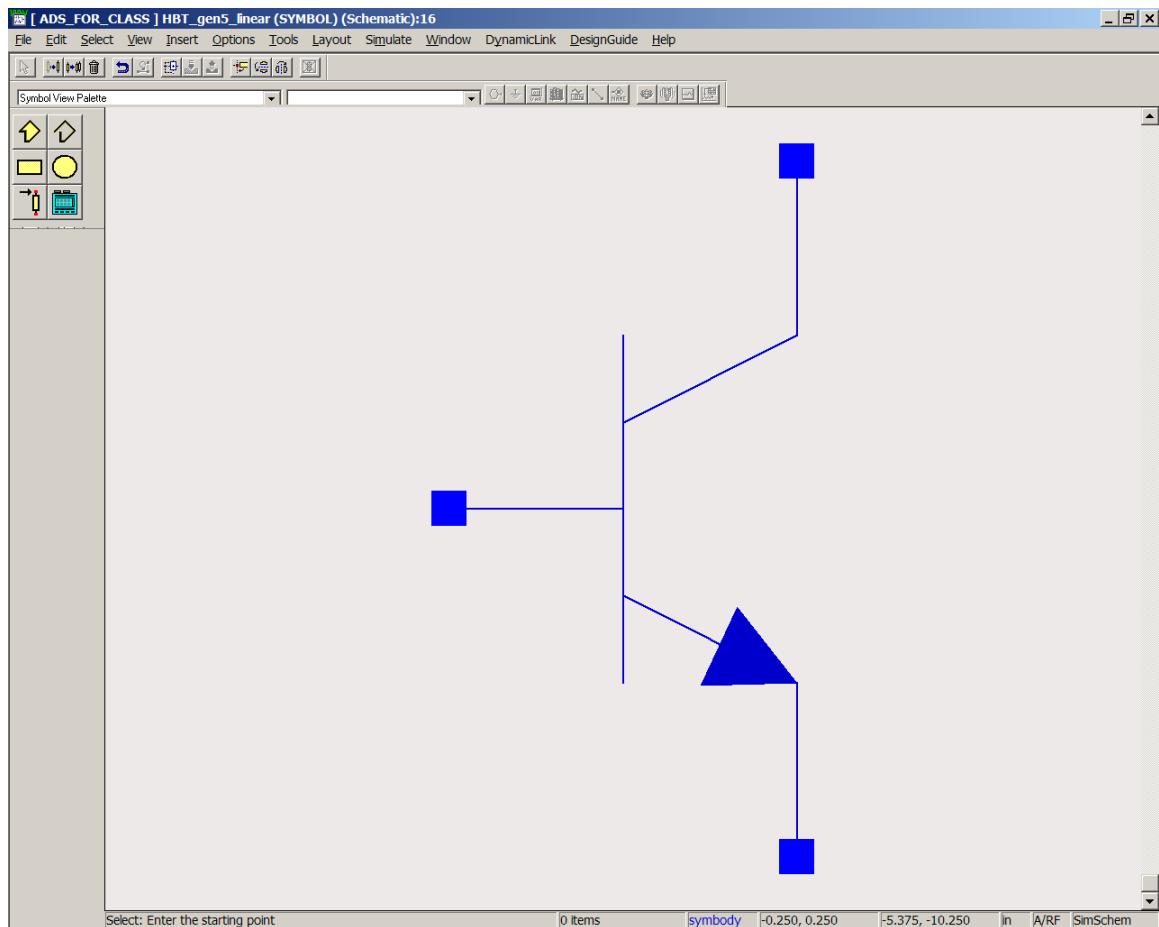
Popping into this model, as we did earlier, and you see the underlying definition based upon a SPICE model, with some additional parasitics and most of the device R's C's, and tau's defined in terms of the device physical dimensions:



Go to file→design parameters, and you will see how the passed parameters are defined (you should not need to play with this)

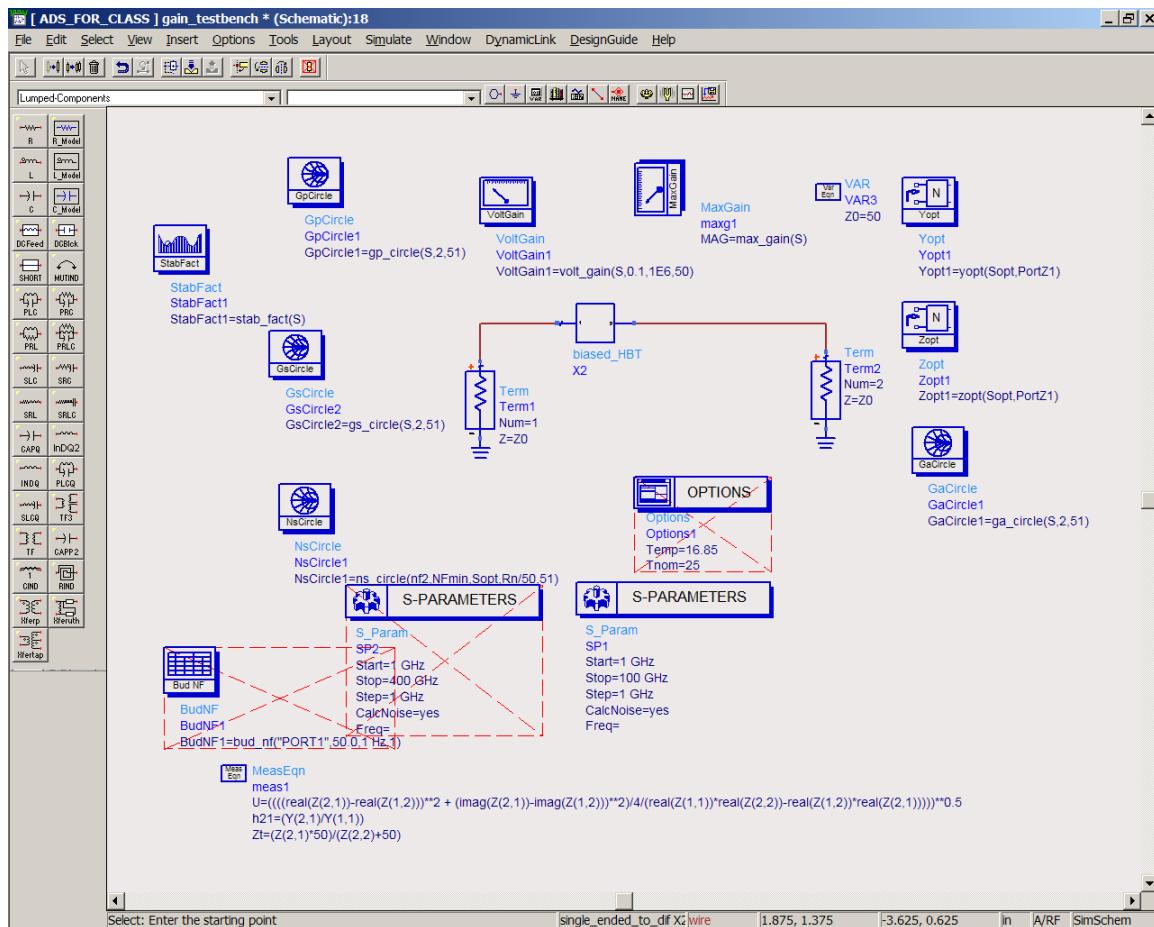


Go to view→ create/edit Schematic symbol and you will see how the subcircuit is given a pretty symbol:

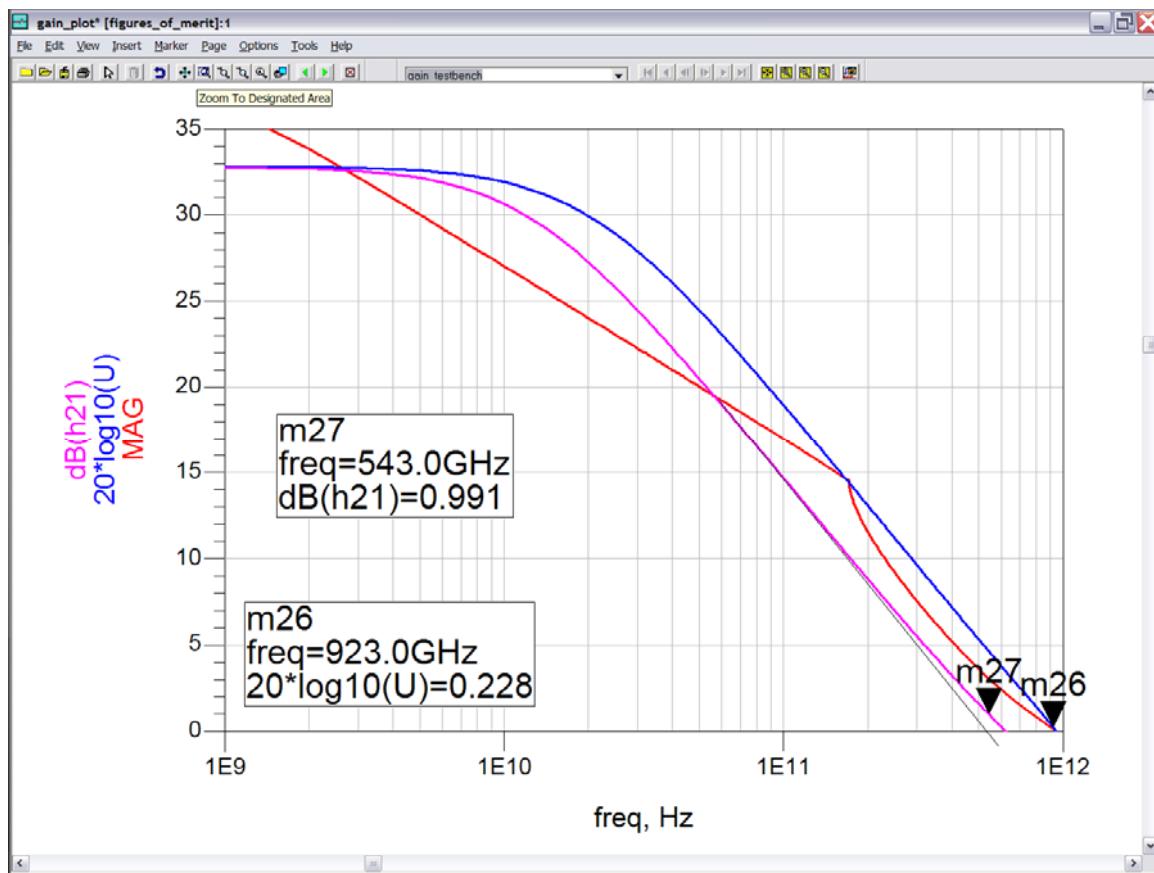


You can edit such symbols, but do so for a backed-up file first, as the editor is somewhat hard to use.

Pop back out to biased_HBT, then open the circuit gain_testbench, and change the DUT to biased_HBT:



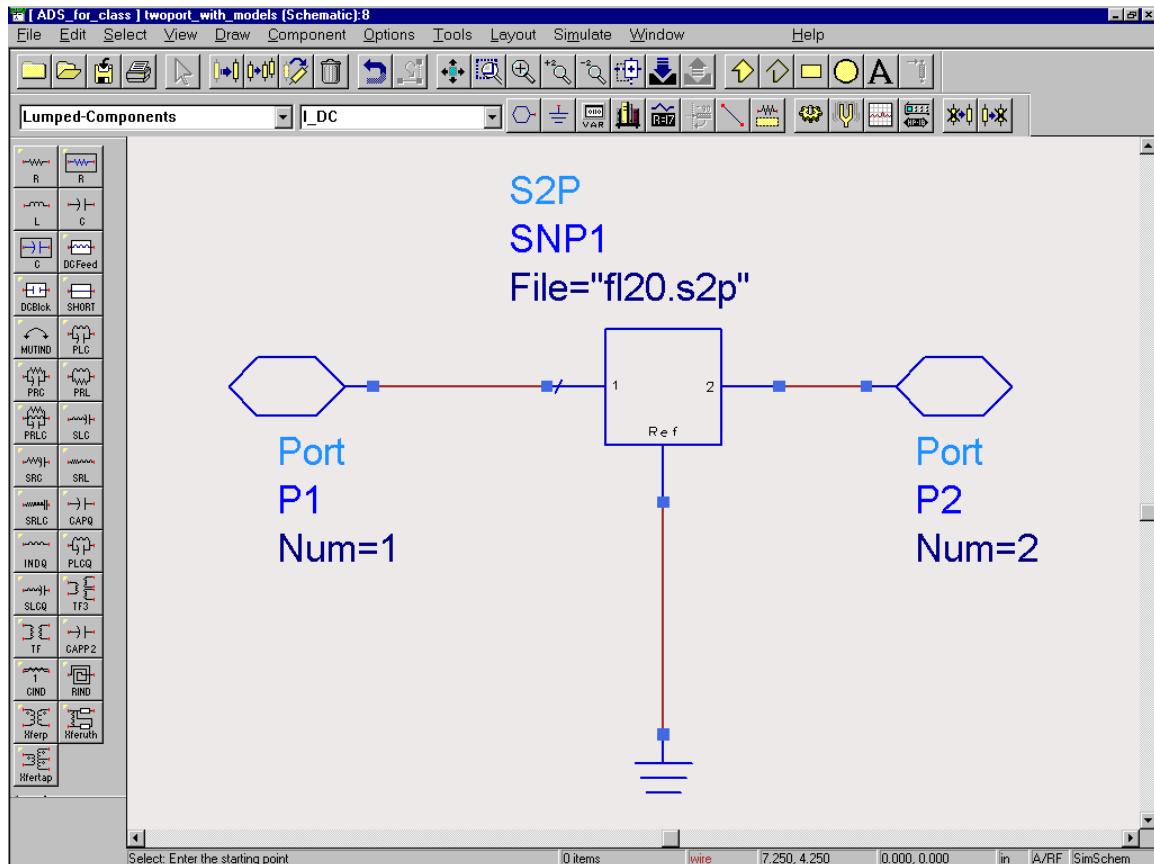
I have increased the frequency range to 1-1000 GHz, and on the figures_of_merit page of the gain plot we can now see the transistor high-frequency gains:



The device has an ft around 540 GHz and an fmax around 900 GHz.

S-parameter Data File

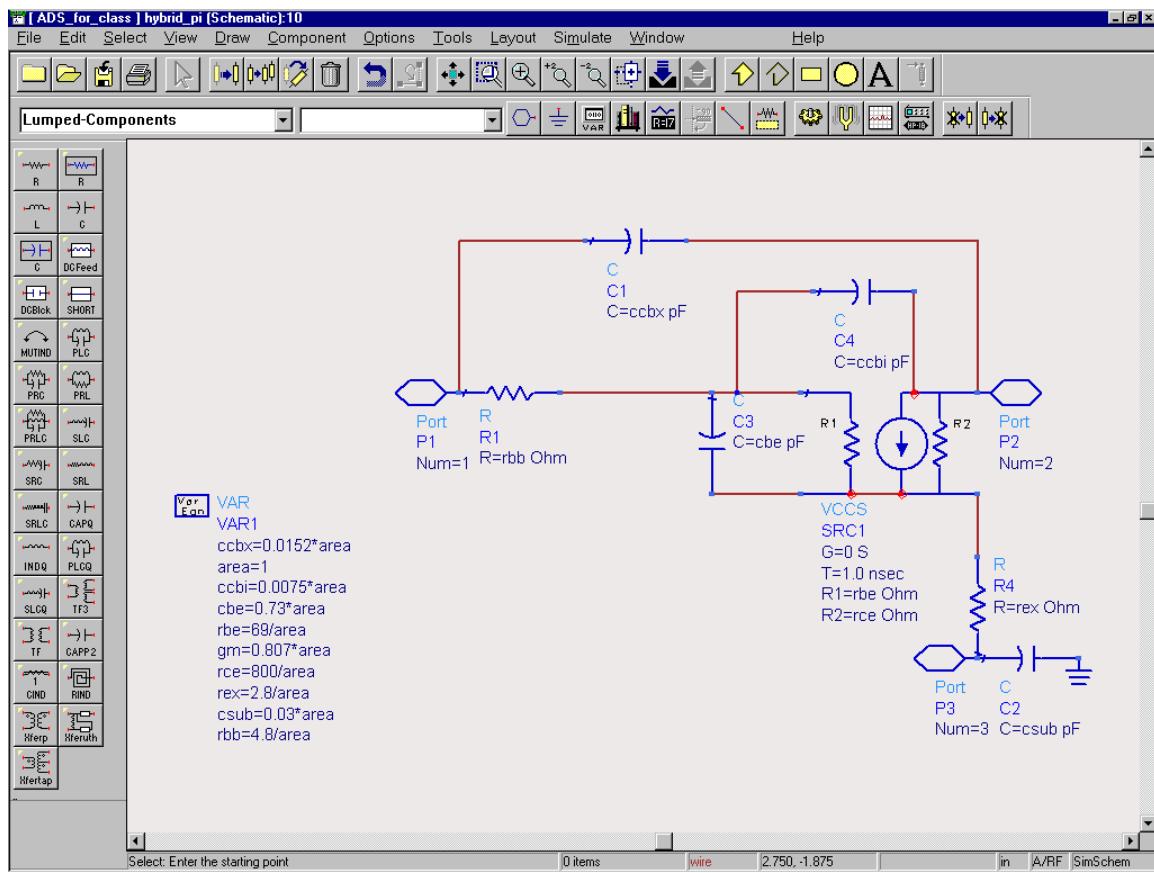
If you have measured data in tabular S parameter form, you can simulate from that



this is FYI only: I have not provided any such data set for you to use.

Small-Signal Models

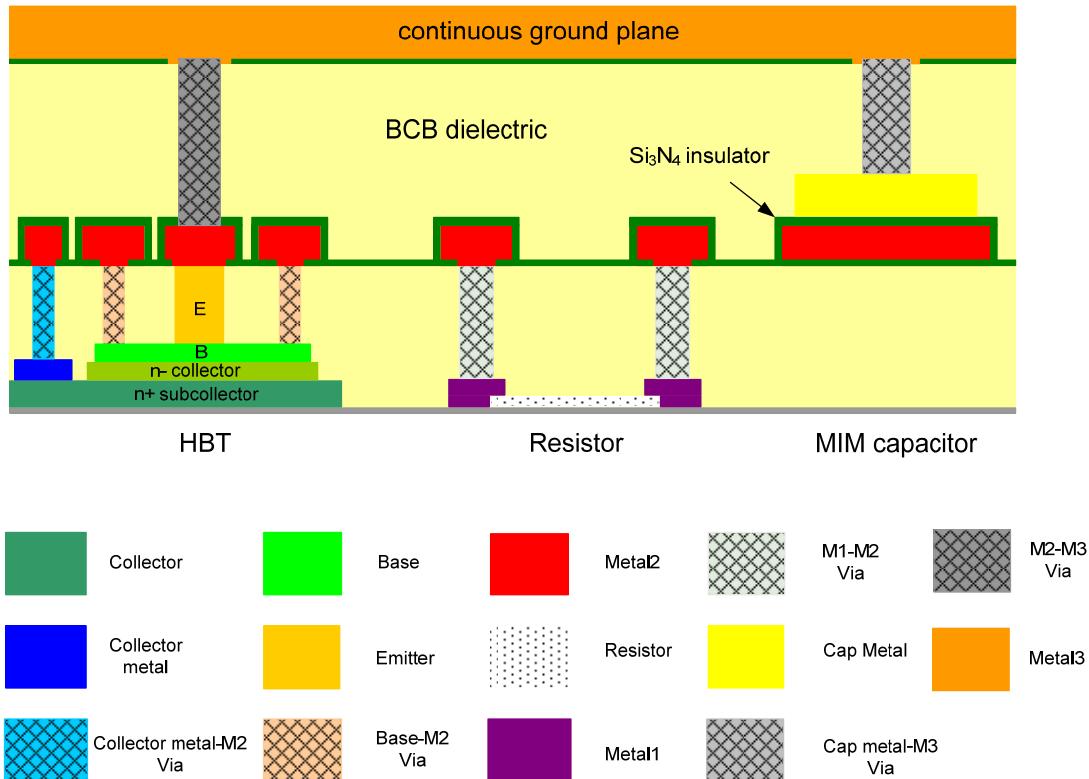
You can directly create hybrid pi models by method. Of course, there is no DC information being carried in this simulation model.



Interconnects

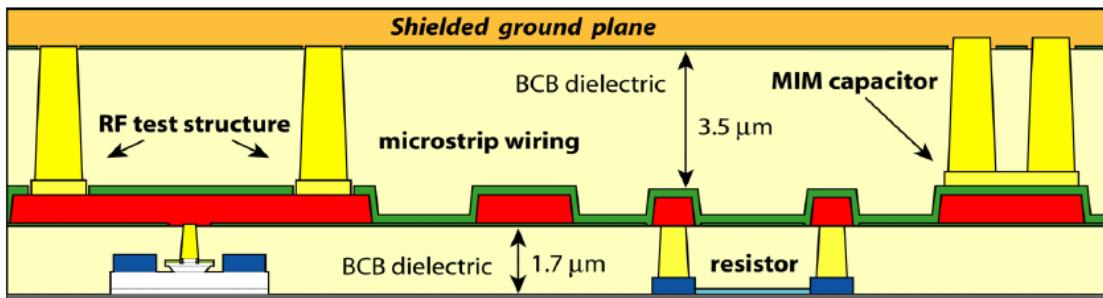
UCSB HBT IC Process cross-section

Let us use a UCSB research process as an introduction to the topic.



The process provides three metal layers, M1, M2, and M3. Normally, M3 will be used as a ground plane and M1 or M2 as signal lines.

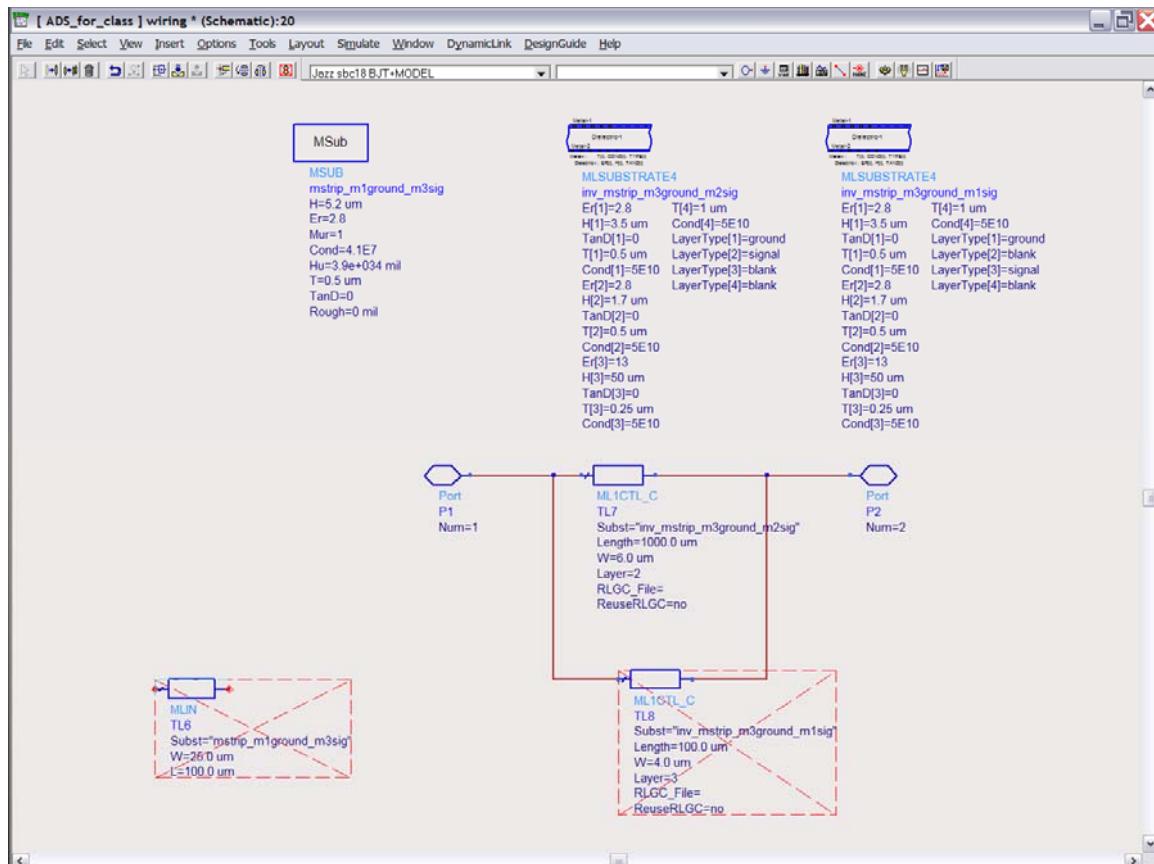
The cross-section below may also be helpful:



Note the thicknesses of the two BCB layers, and note that BCB has a dielectric constant of 3.8. Below the plane of the HBT subcollector, and below the resistors and metal 1, lies the semi-insulating InP substrate, having a dielectric constant of 13. We will approximate that M1 and M2 are each 1/2 micron thick.

Interconnect models (roughly)

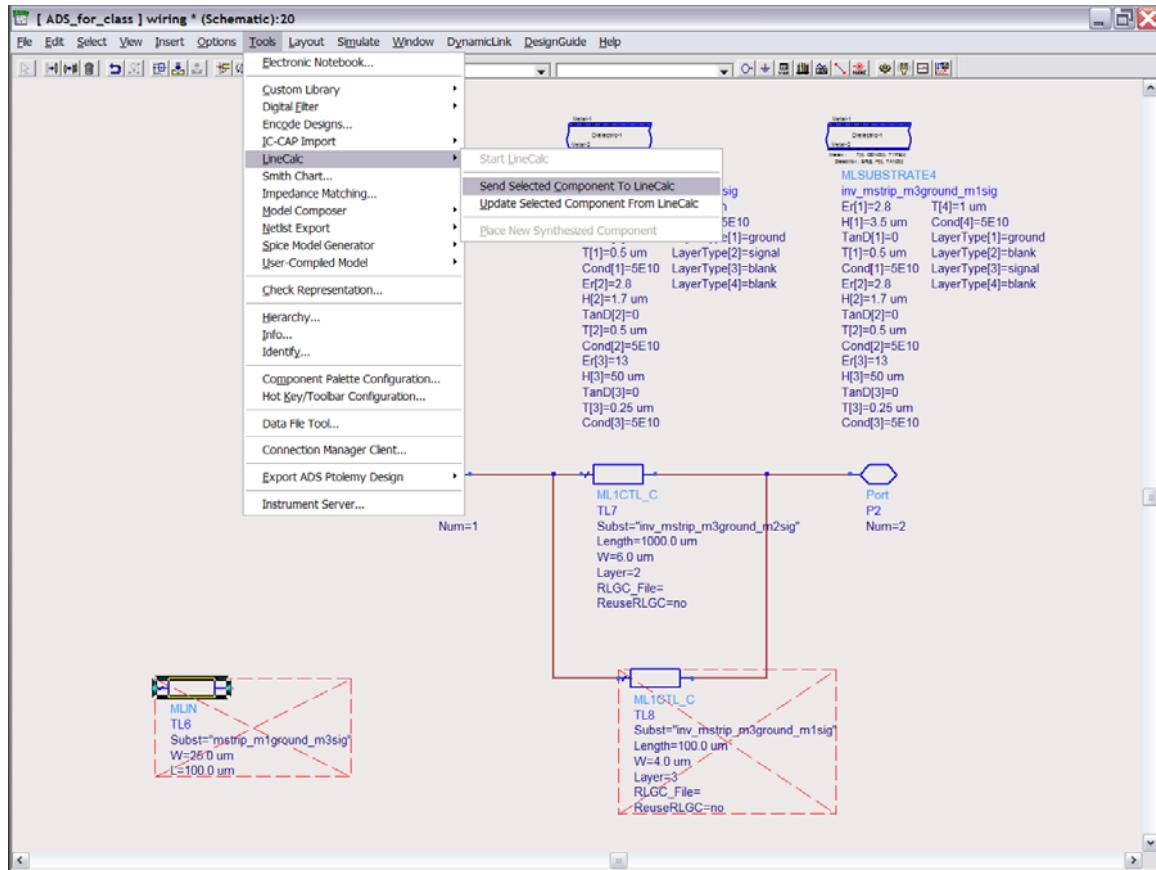
These interconnects can be ***roughly*** modeled as below:



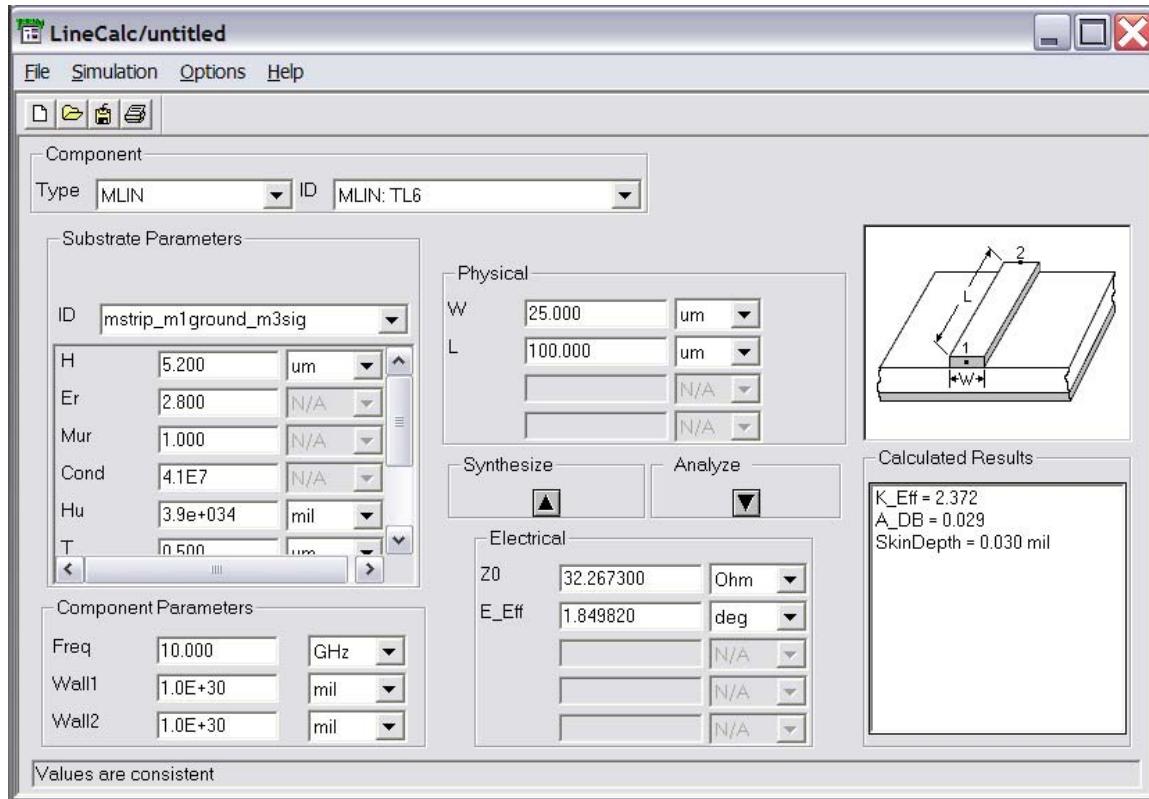
The model "inv_mstrip_m3ground_m2sig" is used for lines with an M3 ground plane and M2 signal line. The model "inv_mstrip_m3ground_m1sig" is used for lines with an M3 ground plane and M1 signal line. There are limitations for this modeling strategy:

- I can't seem to make these models calculate metal line resistance correctly, so I have set the resistance to zero. This will be a serious error for long wires.
- the associated substrate models are not supported by LINECALC. More on linecalc below.

The model "mstrip_m1ground_m3_sig" is a good and fairly accurate model for lines using metal 1 as the ground plane and m3 as the signal line. There are problems in using such lines; see the class notes. For lines of this type, we can select it, and then send its parameters to LINECALC:



...which allows very quick determination of line Z_0 , delay, and attenuation.



Comment: ADS MOMENTUM

In reality, we use ADS MOMENTUM to model a short section of line, and from this determine its inductance, capacitance, and resistance per unit length. From this we usually can fit lines of a specified geometry to a ADS TLINP model. MOMENTUM is a fast, accurate, and powerful tool, but there is not time to learn it in this class.

