LMC6482
CMOS Dual Rail-To-Rail Input and Output Operational Amplifier

General Description
The LMC6482 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6482 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC272 and TLC277.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6482’s rail-to-rail output swing. The LMC6482’s rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6482 especially well-suited for battery-operated systems.

LMC6482 is also available in MSOP package which is almost half the size of a SO-8 device.

See the LMC6484 data sheet for a Quad CMOS operational amplifier with these same features.

Features
(Typical unless otherwise noted)
- Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)
- Guaranteed 3V, 5V and 15V Performance
- Excellent CMRR and PSRR: 82 dB
- Ultra Low Input Current: 20 fA
- High Voltage Gain (R_L = 500 kΩ): 130 dB
- Specified for 2 kΩ and 600Ω loads
- Available in MSOP Package

Applications
- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC272, TLC277

3V Single Supply Buffer Circuit

Connection Diagram

© 2001 National Semiconductor Corporation DS011713 www.national.com
### Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LMC6482AI Limit</th>
<th>LMC6482I Limit</th>
<th>LMC6482M Limit</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD Tolerance (Note 2)</td>
<td>1.5 kV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>± Supply Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage at Input/Output Pin</td>
<td>(V+) +0.3V, (V−) −0.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage (V+ – V−)</td>
<td>16V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current at Input Pin (Note 12)</td>
<td>±5 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current at Output Pin (Notes 3, 8)</td>
<td>±30 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current at Power Supply Pin</td>
<td>40 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec.)</td>
<td>260˚C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Operating Ratings

Supply Voltage: 3.0V ≤ V+ ≤ 15.5V

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LMC6482AM Limit</th>
<th>LMC6482AI, LMC6482I Limit</th>
<th>LMC6482M Limit</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current at Input Pin (Note 13)</td>
<td>0.02</td>
<td>4.0</td>
<td>10.0</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>Input Current (Note 13)</td>
<td></td>
<td>0.01</td>
<td>2.0</td>
<td>5.0</td>
<td>pA</td>
</tr>
<tr>
<td>Common-Mode Input Capacitance</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Input Resistance</td>
<td>&gt;10</td>
<td></td>
<td></td>
<td></td>
<td>TeraΩ</td>
</tr>
<tr>
<td>CMRR Common Mode Rejection Ratio</td>
<td>82</td>
<td>67</td>
<td>65</td>
<td>60</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>0V ≤ V_CM ≤ 15.0V, V+ = 15V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0V ≤ V_CM ≤ 5.0V, V+ = 5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR Positive Power Supply Rejection Ratio</td>
<td>82</td>
<td>67</td>
<td>65</td>
<td>60</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>5V ≤ V+ ≤ 15V, V− = 0V, V_O = 2.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR Negative Power Supply Rejection Ratio</td>
<td>82</td>
<td>67</td>
<td>65</td>
<td>60</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>−5V ≤ V− ≤ −15V, V+ = 0V, V_O = −2.5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMRR Voltage Range</td>
<td>V+ = 5V and 15V For CMRR ≥ 50 dB</td>
<td>V+ − 0.3</td>
<td>−0.25</td>
<td>−0.25</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V+ + 0.3V</td>
<td>V+ + 0.25 V+</td>
<td>V+ + 0.25 V+</td>
<td>V+ + 0.25 V+</td>
<td>V</td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>R_L = 2 kΩ (Notes 7, 13)</td>
<td>Sourcing</td>
<td>666</td>
<td>140</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>75</td>
<td>35</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td>R_L = 600Ω (Notes 7, 13)</td>
<td>Sourcing</td>
<td>300</td>
<td>80</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>35</td>
<td>20</td>
<td>15</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V+ = 5V, V− = 0V, V_CM = V_O = V+/2 and R_L > 1M. **Boldface** limits apply at the temperature extremes.
### DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (Note 5)</th>
<th>LMC6482AI Limit (Note 6)</th>
<th>LMC6482I Limit (Note 6)</th>
<th>LMC6482M Limit (Note 6)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_O$</td>
<td>Output Swing</td>
<td>$V^+ = 5V$ $R_L = 2 , k\Omega$ to $V^+/2$</td>
<td>4.9</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$</td>
<td>4.7</td>
<td>4.5</td>
<td>4.5</td>
<td>4.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^+ = 15V$ $R_L = 2 , k\Omega$ to $V^+/2$</td>
<td>14.7</td>
<td>14.4</td>
<td>14.4</td>
<td>14.4</td>
<td>V</td>
</tr>
<tr>
<td>ISC</td>
<td>Output Short Circuit Current</td>
<td>Sourcing, $V_O = 0V$</td>
<td>20</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking, $V_O = 5V$</td>
<td>15</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>mA</td>
</tr>
<tr>
<td>ISC</td>
<td>Output Short Circuit Current</td>
<td>Sourcing, $V_O = 0V$</td>
<td>30</td>
<td>28</td>
<td>28</td>
<td>28</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking, $V_O = 12V$</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current</td>
<td>Both Amplifiers</td>
<td>1.0</td>
<td>1.4</td>
<td>1.4</td>
<td>1.4</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Both Amplifiers</td>
<td>1.3</td>
<td>1.6</td>
<td>1.6</td>
<td>1.6</td>
<td>mA</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2$, and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (Note 5)</th>
<th>LMC6482AI Limit (Note 6)</th>
<th>LMC6482I Limit (Note 6)</th>
<th>LMC6482M Limit (Note 6)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>(Note 9)</td>
<td>1.3</td>
<td>1.0</td>
<td>0.9</td>
<td>0.9</td>
<td>V/$\mu$s</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td>$V^+ = 15V$</td>
<td>1.5</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\phi_m$</td>
<td>Phase Margin</td>
<td>$V^+ = 15V$</td>
<td>50</td>
<td>Deg</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$G_m$</td>
<td>Gain Margin</td>
<td>$V^+ = 15V$</td>
<td>15</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{m}$</td>
<td>Amp-to-Amp Isolation</td>
<td>(Note 10)</td>
<td>150</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$e_n$</td>
<td>Input-Reflected Voltage Noise</td>
<td>$F = 1 , kHz$ $V_{cm} = 1V$</td>
<td>37</td>
<td>nV/$\sqrt{Hz}$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for \( T_J = 25^\circ C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+ /2 \), and \( R_L > 1M \). **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ. (Note 5)</th>
<th>LMC6482AI Limit (Note 6)</th>
<th>LMC6482I Limit (Note 6)</th>
<th>LMC6482M Limit (Note 6)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( i_n )</td>
<td>Input-Referred Current Noise</td>
<td>( F = 1 \ kHz )</td>
<td>0.03</td>
<td></td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
<tr>
<td>T.H.D.</td>
<td>Total Harmonic Distortion</td>
<td>( F = 10 \ kHz, A_V = -2 ) ( R_L = 10 \ k\Omega, V_O = 4.1 V_{PP} )</td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( F = 10 \ kHz, A_V = -2 ) ( R_L = 10 \ k\Omega, V_O = 8.5 V_{PP} ) ( V^+ = 10V )</td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

### DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for \( T_J = 25^\circ C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = V^+ /2 \) and \( R_L > 1M \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ. (Note 5)</th>
<th>LMC6482AI Limit (Note 6)</th>
<th>LMC6482I Limit (Note 6)</th>
<th>LMC6482M Limit (Note 6)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td></td>
<td>0.9</td>
<td>2.0</td>
<td>3.0</td>
<td>3.0</td>
<td>mV max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7</td>
<td>3.7</td>
<td>3.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( TCV_{OS} )</td>
<td>Input Offset Voltage Average Drift</td>
<td></td>
<td>2.0</td>
<td></td>
<td></td>
<td></td>
<td>μV/°C</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td></td>
<td>0.02</td>
<td></td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current</td>
<td></td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>( 0V \leq V_{CM} \leq 3V )</td>
<td>74</td>
<td>64</td>
<td>60</td>
<td>60</td>
<td>dB min</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>( 3V \leq V^- \leq 15V ), ( V^- = 0V )</td>
<td>80</td>
<td>68</td>
<td>60</td>
<td>60</td>
<td>dB min</td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Input Common-Mode Voltage Range</td>
<td>For CMRR \geq 50 dB</td>
<td>( V^- -0.25 )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( V^+ + 0.25 )</td>
<td>( V^- )</td>
<td>( V^+ )</td>
<td>( V^+ )</td>
<td>V min</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Swing</td>
<td>( R_L = 2 \ k\Omega ) to ( V^+ /2 )</td>
<td>2.8</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 600\Omega ) to ( V^+ /2 )</td>
<td>2.7</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>V min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.37</td>
<td>0.6</td>
<td>0.6</td>
<td>0.6</td>
<td>V max</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>Both Amplifiers</td>
<td>0.825</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
<td>mA max</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

Unless otherwise specified, \( V^+ = 3V, V^- = 0V, V_{CM} = V_O = V^+ /2 \) and \( R_L > 1M \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ. (Note 5)</th>
<th>LMC6482AI Limit (Note 6)</th>
<th>LMC6482I Limit (Note 6)</th>
<th>LMC6482M Limit (Note 6)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>(Note 11)</td>
<td>0.9</td>
<td>V/μs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td></td>
<td>1.0</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T.H.D.</td>
<td>Total Harmonic Distortion</td>
<td>( F = 10 \ kHz, A_V = -2 ) ( R_L = 10 \ k\Omega, V_O = 2 V_{PP} )</td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>
AC Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a Class 1 device rating.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of T J(max), R θJA, and T A. The maximum allowable power dissipation at any ambient temperature is P D = (T J(max) – T A)/R θJA. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V+ = 15V, V CM = 7.5V and R L connected to 7.5V. For Sourcing tests, 7.5V ≤ V O ≤ 11.5V. For Sinking tests, 3.5V ≤ V O ≤ 7.5V.

Note 8: Do not short circuit output to V+, when V+ is greater than 13V or reliability will be adversely affected.

Note 9: V+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, V+ = 15V and R L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V O = 12 V PP.

Note 11: Connected as voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature parameters see RETS6482X.

Typical Performance Characteristics  V S = +15V, Single Supply, T A = 25°C unless otherwise specified

Supply Current vs Supply Voltage

Input Current vs Temperature

Sourcing Current vs Output Voltage

Sourcing Current vs Output Voltage

Sinking Current vs Output Voltage
Typical Performance Characteristics  $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

- **Sinking Current vs Output Voltage**
  - $V_S = 3V$
  - Output Voltage Referenced to GND (V)

- **Output Voltage Swing vs Supply Voltage**
  - $R_L = 100\, \Omega$
  - Supply Voltage (V)

- **Input Voltage Noise vs Frequency**
  - $V_S = 15V$
  - Frequency (Hz)

- **Input Voltage Noise vs Input Voltage**
  - $V_S = 15V$
  - Common Mode Input Voltage (V)

- **Input Voltage Noise vs Input Voltage**
  - $V_S = 3V$
  - Common Mode Input Voltage (V)

- **Crosstalk Rejection vs Frequency**
  - $V_S = 15V$
  - Rejection (dB)
  - Frequency (kHz)
Typical Performance Characteristics  \( V_S = +15V, \) Single Supply, \( T_A = 25˚C \) unless otherwise specified (Continued)

**Crosstalk Rejection vs Frequency**

\[ V_S = 5V, \quad R_C = 5 \, k\Omega \]

-REJECTION (dB)
-\( \text{FREQUENCY (kHz)} \)

**Positive PSRR vs Frequency**

\[ V_S = 5V, \quad R_C = 5 \, k\Omega \]

-PSRR (dB)
-\( \text{FREQUENCY (Hz)} \)

**Negative PSRR vs Frequency**

\[ V_S = 5V, \quad R_C = 5 \, k\Omega \]

-PSRR (dB)
-\( \text{FREQUENCY (Hz)} \)

**CMRR vs Frequency**

\[ V_S = 1.5V, \quad R_C = 5 \, k\Omega \]

-CMRR (dB)
-\( \text{FREQUENCY (Hz)} \)

**CMRR vs Input Voltage**

\[ V_S = \pm 7.5V, \quad F = 10 \, kHz, \quad R_C = 5 \, k\Omega \]

-CMRR (dB)
-\( \text{INPUT VOLTAGE (V)} \)

**\( \Delta V_{OS} \) vs CMR**

\[ V_S = \pm 2.5V \]

-CHANGE IN \( V_{OS} \) (mV)
-\( \text{INPUT VOLTAGE (V)} \)

**\( \Delta V_{OS} \) vs CMR**

\[ V_S = \pm 1.5V \]

-CHANGE IN \( V_{OS} \) (mV)
-\( \text{INPUT VOLTAGE (V)} \)
Typical Performance Characteristics  $V_S = +15V$, Single Supply, $T_A = 25°C$ unless otherwise specified (Continued)
Typical Performance Characteristics  $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

Open Loop Output Impedance vs Frequency

Slew Rate vs Supply Voltage

Non-Inverting Large Signal Pulse Response

Non-Inverting Large Signal Pulse Response

Non-Inverting Small Signal Pulse Response

Non-Inverting Small Signal Pulse Response

Inverting Large Signal Pulse Response
Typical Performance Characteristics $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

**Inverting Large Signal Pulse Response**

- Time (1$\mu$s/Div)
- Input Signal (1V/Div)
- Output Signal (1V/Div)

**Inverting Small Signal Pulse Response**

- Time (1$\mu$s/Div)
- Input Signal (50mV/Div)
- Output Signal (50mV/Div)

**Stability vs Capacitive Load**

- Capacitive Load (10000)
- Voltage Output (V)

- Capacitive Load (1000)
- Voltage Output (V)

- Capacitive Load (100)
- Voltage Output (V)
Typical Performance Characteristics  $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

Application Information

1.0 Amplifier Topology

The LMC6482 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6482’s input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

2.0 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6482 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

3.0 Rail-To-Rail Output

The approximated output resistance of the LMC6482 is 180Ω sourcing and 130Ω sinking at $V_S = 3V$ and 110Ω sourcing and 80Ω sinking at $V_S = 5V$. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC6482 can typically directly drive a 100 pF load with $V_S = 15V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive
Application Information (Continued)

Loading reduces the phase margin of op-amps. The combination of the op-amp’s output impedance and the capacitive load induces phase lag. This results in either an under-damped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 4. This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.

\[
\begin{align*}
R_1 \cdot C_1 & \leq R_2 \cdot C_f \\
\end{align*}
\]

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for \(C_f\) may be different. The values of \(C_t\) should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)
6.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6482, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even through it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LM6482's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 9. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6482's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 10 for typical connections of guard rings for standard op-amp configurations.

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don’t insert the amplifier’s input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 11.
7.0 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in Figure 12. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with $V_{S} = \pm 5V$.

![FIGURE 12. Inverting Configuration Offset Voltage Adjustment](image1)

8.0 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6482’s features. The key benefit of designing in the LMC6482 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range. Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inversion or severe distortion.

9.0 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482 (Figure 14). Capable of using the full supply range, the LMC6482 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC4282 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.
10.0 Instrumentation Circuits

The LMC6482 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6482 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6482 an excellent choice of noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with $R_g$ to set the differential gain of the 3 op-amp instrumentation circuit in Figure 15. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

![FIGURE 15. Low Power 3 Op-Amp Instrumentation Amplifier](image-url)
Application Information (Continued)

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 16. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

![FIGURE 16. Low-Power Two-Op-Amp Instrumentation Amplifier](DS01713-30)

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

11.0 Spice Macromodel

A spice macromodel is available for the LMC6482. This model includes accurate simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions
- and many more characteristics as listed on the macromodel disk.

Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications

The circuit in Figure 17 uses a single supply to half wave rectify a sinusoid centered about ground. \( R_I \) limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in Figure 19.

![FIGURE 17. Half-Wave Rectifier with Input Current Protection (RI)](DS01713-31)

![FIGURE 18. Half-Wave Rectifier Waveform](DS01713-32)

![FIGURE 19. Full Wave Rectifier with Input Current Protection (RI)](DS01713-33)
In Figure 23 dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of \( C_{\text{H}} \) and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.

\[
I_{\text{OUT}} = \frac{(V^+ - V_{\text{IN}})}{R}
\]

FIGURE 23. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

In Figure 23 dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of \( C_{\text{H}} \) and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.
Typical Single-Supply Applications (Continued)

The LMC6482's high CMRR (82 dB) allows excellent accuracy throughout the circuit’s rail-to-rail dynamic capture range.

![Figure 24. Rail-to-Rail Sample and Hold](image)

R1 = R2, C1 = C2; f = \frac{1}{2\pi R1 C1}; DF = \frac{1}{2}\sqrt{\frac{C2}{C1}} \sqrt{\frac{R2}{R1}}

**FIGURE 25. Rail-to-Rail Single Supply Low Pass Filter**

The low pass filter circuit in Figure 25 can be used as an anti-aliasing filter with the same voltage supply as the A/D converter. Filter designs can also take advantage of the LMC6482 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

### Ordering Information

<table>
<thead>
<tr>
<th>Package</th>
<th>Temperature Range</th>
<th>NSC Drawing</th>
<th>Transport Media</th>
<th>Package Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Pin</td>
<td>Military: −55°C to +125°C, Industrial: −40°C to +85°C</td>
<td>LMC6482AIN, LMC6482IN</td>
<td>Rail</td>
<td>LMC6482MN, LMC6482AIN, LMC6482IN</td>
</tr>
<tr>
<td>Molded DIP</td>
<td></td>
<td>N08E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8-pin</td>
<td>LMC6482AIM, LMC6482AIMX, LMC6482IM, LMC6482IMX</td>
<td>M08A</td>
<td>Rail, Tape and Reel</td>
<td>LMC6482AIM, LMC6482IM</td>
</tr>
<tr>
<td>Small Outline</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ceramic DIP</td>
<td>LMC6482AMJ/883</td>
<td>J08A</td>
<td>Rail</td>
<td>LMC6482AMJ/883Q5962-9453401MPA</td>
</tr>
<tr>
<td>8-pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mini SO</td>
<td>LMC6482IM, LMC6482IMMX</td>
<td>MUA08A</td>
<td>Rail, Tape and Reel</td>
<td>A10</td>
</tr>
</tbody>
</table>

www.national.com 18
Physical Dimensions inches (millimeters) unless otherwise noted

8-Pin Ceramic Dual-In-Line Package
Order Number LMC6482AMJ/883
NS Package Number J08A

8-Pin Small Outline Package
Order Package Number LMC6482AIM, LMC6482AIMX, LMC6482IM or LMC6482IMX
NS Package Number M08A
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

8-Pin Molded Dual-In-Line Package
Order Package Number LMC6482AIN, LMC6482IN
NS Package Number N08E
LIFE SUPPORT POLICY

NATIONAL’S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.