1) **Intrinsic IIP3 of NMOS devices (20)**

   a. Simulate a 100um NMOS device (20 x 5 um x 0.18um) to verify the nonlinear short channel model and the high IIP3 bias condition in saturation (Vds = 1.8 V). Plot the $I_d$ versus $V_{gs}$ on one plot and three transconductance coefficients on another. (16)

   b. Find the $V_{gs}$ which gives infinite IIP3 and plot IIP3 as a function of gate voltage. If the $V_{gs}$ changes by +/-10 mV, what is the IIP3? (4)

2) **LNA IIP3.** Last quarter you designed an LNA. You used transient simulations to calculated the IIP3. Now let’s revisit your LNA design to look at the effect of cross modulation distortion.

   A triple-tone test is used to characterize the cross-modulation distortion (XMD). To start, we will demonstrate the triple-tone test with a transient simulation. Then, the waveform at the output will be transferred to the frequency spectrum using a discrete Fourier Transform (DFT). We can find the XMD tone with the frequency spectrum.

   a. Now take a resistive feedback LNA for example. (This is just for demonstration. For your practice, you might have a different LNA) Note that the port is defined at the input and output of the LNA.

   ![Diagram of LNA ports](image)

   b. Open ADE and load the setup. Run an S-parameter (small-signal) simulation of your LNA and generate a plot of $S_{21}$. Record the center of your LNA band. (10 pts)

   c. In the analysis, select the tran simulation and set F1, F2 and F3 are three frequencies and $P_1$, $P_2$ and $P_3$ are the respective powers in dBm for the triple tone test. For our purposes use F3 to be the center of your LNA band and F1 to
be 50 MHz below the receive band and F2 to be 60 MHz below the receive band. Use P1 of -40 dBm and P1/P2 of 0 dBm.

3) You have to calculate how long you should run for tran simulation. For example, If you use 895M, 905M and 995M, then the greatest common divisor is 5M. It means at least you have to run 1/5M = 200ns. Make sure all the options in the Output box are selected. Also, click the “RFout Frespec in dBm” in Output box.

4) In the Expression, the time slot you chose to do DFT should be appropriate for the time period of the beat frequency. In this example, the DFT is calculated from 200ns to 400ns. For the first 200ns, it is used to make sure the circuit goes into steady state. (depends on your architecture). Close setting Outputs box. Run the simulation.

5) When the simulation is done. A frequency spectrum will show up. Try to zoom in to the frequency range you are interested. For this case, three input tones are at 895M, 905M and 995MHz. The output IM3 tone is located at 995 + (905 - 895) = 1005MHz. Provide a plot of the FFT spectrum and calculate the IIP3 from your result. (20 pts)
6) The transient technique while effective is very time-consuming; particularly to make the IM3 versus PIN plot that is common in receiver characterization. A more common approach to do an IIP3 simulation is based on Harmonic Balance or Periodic Steady State (PSS) simulation. Rather than explain PSS here, please use the application note from Cadence (LNA Design Using SpectreRF) that explains how to setup a PSS simulation on page 37. The entire application note might be worth perusing if you are lost when you skip to page 37. For two tones separated by 10 MHz that fall in the center of your LNA band, sweep the power of the tones from -50 dBm to -10 dBm. Show a single plot of the IM3 and the fundamental tone versus input power and extrapolate IIP3 and P1dB. (20 pts)