Transistor Technologies for High Efficiency and Linearity
Transistor Technologies for Microwave Circuits

MOSFET

Source
Gate
Drain

HEMT
MESFET

S
G
D

Emitter
n⁺ InGaAs
n⁺ GaAs
n⁺ GaInP
p⁺ GaAs

Base
n⁻ GaAs
n⁻ GaAs

Collector

Semi-insulating GaAs substrate

GaAs HBT

SiGe HBT
RFMD POLARIS™ TOTAL RADIO™
Quad-Band GSM/EDGE Architecture (2.5G)

Technologies in multi-chip module

- GaAs HBT
- GaAs pHEMT
- HV CMOS
- Bulk CMOS
- SiGe BiCMOS
- LiTaO₃ SAW filters
- SMD capacitors
- Packaged XTAL

external XTAL
Requirements for Transistors in Power Amplifiers

High microwave gain
Low on-resistance & low “knee voltage”
High power density
High voltage capability
Linearity
Ease of matching
Ease of biasing
Adequate heatsinking
Low cost (high yield)
Reliability & ruggedness
Stability
Central Concern for Transistors in ECE265C

What is highest voltage that can be maintained?
What is highest current that can be delivered?
What is highest power that can be withstood?
Safe Operating Area for Transistors

$I_{\text{max}}$ depends on device size

*Maximum power dissipation* depends on size and duty cycle
- worse for CW tone than for high PAR signals
**Tradeoff of Breakdown Voltage and $ft$**

To avoid breakdown, generally must limit peak electric field to below a critical value, $\varepsilon_b$

To achieve high voltage, one can design the high field region to be long:

$$V_{bk} = \varepsilon_b \cdot wc$$

The large $wc$ tends to increase transit time for carriers, resulting in low $ft$:

$$T_{tr} > wc / v_{sat}, \quad Ft = 1 / (2\pi T_{tr})$$

The product of $V_{bk}$ and $ft$ tends to be independent of $wc$:

$$V_{bk} \cdot ft \leq \varepsilon_b \cdot v_{sat} / 2 \pi$$

CMOS scaling through Moore’s Law acts to drive up $ft$, but it drives down $V_{bk}$ at the same time.
Speed-Voltage Tradeoff in Transistors

Ft = \frac{1}{2\pi Ttr}

Ttr = \frac{Wc}{vsat} \quad \text{(or } \frac{1}{2} \frac{Wc}{vsat}\text{)}

BV = \frac{1}{2} \varepsilon_b Wc \quad \text{(or } \varepsilon_b Wc\text{)}

BV*ft = \frac{1}{2} \varepsilon_b Wc \times \frac{1}{2\pi} \frac{vsat}{Wc}

BV*ft \sim \frac{1}{2\pi} \varepsilon_b * vsat

\varepsilon_b: \text{breakdown electric field}

Source or base \quad \text{Channel or BC depletion region} \quad \text{Drain or collector}

Drain or collector

Source or base

Ttr

Wc

\varepsilon_b: \text{breakdown electric field}
Transistor Size

Need to pick device large enough to support $I_{\text{max}}$
Not necessarily well described in SPICE models

For bipolars: $I_c/A_{\text{emitter}} = J_c < 2-5 \text{ mA/um}^2$ for Si
< 0.5 mA/um$^2$ for GaAs

For FETs: $I_d/W_g < 0.3-0.8 \text{ A/mm}$ for CMOS
0.1 A/mm for LDMOS
0.2-1 A/mm for pHEMT
0.5-1.5 A/mm for GaN
Thermal Effects in Power Transistors

• Burnout (melting of portions of device, rapid diffusion of defects, excess stress, etc)
• Degradation
• Thermal runaway in bipolar transistors
• Decreased performance: reduced Iout, lower ft, etc
• Thermally induced distortion & memory effect
• Difference between cw and short-time ac characteristics
Negative Output Conductance due to heating
Basics of Thermal Circuits

\[ \Delta T_j = T_{\text{junction}} - T_{\text{heatsink}} = R_{\text{th}} \times P_{\text{dissipated}} \]

(C) \hspace{2cm} (C/W) \times W

Analog with standard electrical circuits

- \( V \)
- \( R \times I \)
Thermal Resistance of Transistor

Main contribution is often $R_{th}$ to back of chip

$$\Delta T = P_{diss} \cdot R_{th}$$

$$R_{th} \sim \frac{1}{K_{th}} \cdot \frac{L}{A} \quad \text{(rect. prism geometry)}$$

$K_{th}$:
- GaAs: 0.45
- Si: 1.5
- InP: 0.7

Heat spreads approximately at 45 degrees in substrate
Thermal Resistance Calculations Using 3D Structure Simulators (solve Laplace’s equation)

InP HBT
CMOS SOI

Ansys, comsol, sentaurus, etc
Thermal Resistance Estimate 1

Single stripe heat source (neglects heat sinking from leads)

Assume for simplicity that heat spreads at 45 degrees.
Calculate the resistance of each section of substrate by taking into account its area.

\[ R_{th} = \sum \Delta R \Delta z \Rightarrow \frac{1}{k_{th}} \int_0^h \frac{dz}{A(z)} \]

\[ R_{th} = \frac{1}{k_{th}} \int_0^h \frac{dz}{(w+2z)(L+2z)} \quad \text{for spreading in 2 dimensions} \]

\[ R_{th} = \frac{1}{2k_{th}} \cdot \frac{1}{L-w} \ln \left( \frac{w+2h}{L+2h} \cdot \frac{L}{w} \right) \]

(For \( w \approx L \), \( R_{th} \to \frac{1}{k_{th}} \cdot \frac{h}{L(L+2h)} \))

For \( L \) very long (\( L > h \)) spreading in one dimension

\[ R_{th} = \frac{1}{k_{th}} \int_0^h \frac{dz}{L(w+2z)} = \frac{1}{2k_{th}} \ln \frac{w+2h}{w} \]

\[ h \]

Rth for section near device is \( \gg \) Rth at bottom
Multiple stripes heat source

When heat flux from different transistors overlap, area available for heat flow from each is limited.

\[
R_{th} = \frac{1}{X_{th}} \int_{0}^{h} \frac{dz}{A(z)} = \frac{1}{X_{th}} \left[ \int_{0}^{s/2} \frac{dz}{(w+2z)(L+2z)} + \int_{s/2}^{h} \frac{dz}{(w+s)(L+2z)} \right]
\]

\[
R_{th} = \frac{1}{2X_{th}} \left[ \frac{1}{L-w} \ln \frac{w+s}{L+S} + \frac{1}{w+1} \ln \frac{1+2h}{L+S} \right]
\]
How To Decrease Thermal Resistance

- Thin substrates
- Thermal Vias
- Heat Spreaders
- Flip-chip bonding (sometimes)
FETs for Power Amplifiers

- Si
- GaAs
- InP
- GaN
- CMOS
- LDMOS (Laterally Diffused MOS)
- MESFET
- HEMT
- pHEMT
Different Flavors of FET

MOSFET

MESFET

HEMT

SOURCE GATE DRAIN

SOURCE GATE DRAIN

SOURCE GATE DRAIN

N-GaAs

N-GaAlAs

UNDOPED GaAs

SEMI-INSULATING GaAs

SEMI-INSULATING GaAs

P-Si

SEMIFET

MESFET

JFET
Limits in CMOS Transistors

• **Limits on \( I_{ds} \):** maximum channel charge is limited by gate oxide field: \( qN_{\text{max}} \sim \varepsilon_{\text{ox}} E_{\text{oxmax}} \)

• **Oxide breakdown:** typically occurs at 10MV/cm => 1V for every 10A of gate oxide
  Gate-channel breakdown will occur at source or drain, wherever field is highest.
  There are slow oxide “breakdown” mechanisms too (time-dependent dielectric breakdown)

• **Avalanche breakdown in channel at high \( V_{DS} \) values**

• **Oxide charging:** when operated at high \( V_{ds} \), electrons are injected into the gate oxide, creating trapped charge which shifts device threshold (hot carrier injection)
Hot Electron Generation

Electrons acquire energy from the electric field along the channel. Most electrons lose this energy ("thermalize") but some electrons don't.

Excess kinetic energy
High Voltage Breakdown Mechanism of MOS Transistor

Impact ionization at drain edge of gate

Source   Channel   Drain

Moderate electric field

High electric field

What happens to holes generated by impact ionization?
They flow to the substrate and to the source.
They cause some extra current due to body effect.
They can be measured as substrate or well current.
Hot Electron Effects

High electric fields → Energetic electrons → Impact ionization (E>1.5eV) → Avalanche breakdown
Substrate current
Parasitic bipolar
Snapback behavior

Charge injection into SiO2 (E>3eV) → Vt shifts
Transconductance degradation

Diagram:
- Forward injection
- Avalanche
- Substrate current
- Depletion-layer edge
- Substrate
CMOS Id-Vds curve (generic)
SOI effects

Parasitic bipolar transistor
Fed by impact ionization
Causes excess $I_d$, lower BV

"snapback"
Hot Electron Effect 2: Reliability problem from oxide charging

Causes increase in Vth as the device is operated (Current drops, device turns off)
Lightly Doped Drain Structure (LDD) To Minimize Hot Electron Effects

Minimize electric field near drain
Technique to improve CMOS PAs:

**Differential Topology**

- Double the available voltage swing
- Even-order harmonic suppression
- Double the frequency of current injection into substrate
  - Reduce the potential for LO-pulling
- The tail current source is removed from the standard differential pair (*this is a “quasi-differential” structure*)
  - DC current set by the biasing of input devices
  - Max. current set by the input voltage swing
- May require differential to single-ended output conversion (balun)
Technique to improve CMOS PAs:

**Cascode Structure**

- Generally used in Op-Amps and other analog designs
  - Increase the small-signal output resistance
  - Reduce the Miller effect
- In the case of RF PA, isolate the input and output nodes
  - Reduce the impact of oxide breakdown
- On the cascode device,
  - $V_{ox(max)} = V_{out(max)} - V_{bias}$
- On the bottom device,
  - $V_{ox(max)} = V_{casc} - V_{in} = V_{bias} - V_t - V_{in(min)}$
Id-Vds Characteristics of Cascode

**Id-Vds for Cascode:**
- Higher Ron
- Lower Idmax
- Body effect on top FET
- Higher Vmin decreases efficiency
Stacked-FET Structure

- All FETs are operating in the safe region
Stacked-FET Structure

- All FETs are operating in the safe region
Stacked-FET Structure

Tailor swing at each drain and gate by proper selection of gate capacitor

\[ Z_{s2} = R_{\text{opt}} \]

\[ Z_{s3} = 2R_{\text{opt}} \]

\[ 3R_{\text{opt}} \]

\[ C \]

\[ C_{gs} \]

\[ Z_{2s} \]

\[ C_{2} \]

\[ C_{3} \]

\[ R_{L} \]

\[ r_{o} \]

\[ g_{m} \]

\[ V_{gs} \]

\[ V_{t} \]

\[ i_{t} \]

\[ Id \sim g_{m} V_{gs} \]

\[ \sim g_{m} V_{t} C_{2}/(C_{2}+C_{gs}) \]

\[ Z_{s2} = \left( 1 + \frac{C_{gs}}{C_{2}} \right) \frac{1}{g_{m}} \]
Stacked FET Approach for CMOS PAs

*Works well at least up to 90GHz !!!*

In 45 nm CMOS SOI

50 mW Psat at 90GHz

*Jefy Jayamon (UCSD)*
Power Combining with Distributed Active Transformers

Aoki, Kee, Hajimiri and Rutledge (Caltech)
CMOS Amplifier with On-Chip Transformer

<table>
<thead>
<tr>
<th>Technology</th>
<th>Value</th>
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<tbody>
<tr>
<td>Technology</td>
<td>0.35 μm BiCMOS</td>
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<tr>
<td>Oxide thickness to top metal</td>
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<tr>
<td>Top metal sheet resistance</td>
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<td>Metal 2 sheet resistance</td>
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<tr>
<td>Top metal thickness</td>
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<tr>
<td>Metal 2 thickness</td>
<td>0.5 μm</td>
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<tr>
<td>Metal 1 thickness</td>
<td>0.5 μm</td>
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**SUMMARY OF MEASURED AND SIMULATED AMPLIFIER PERFORMANCE**

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<thead>
<tr>
<th></th>
<th>Pout (W)</th>
<th>η (%)</th>
<th>PAE (%)</th>
<th>Gain (dB)</th>
<th>η active (%)</th>
<th>η passive (%)</th>
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<td>48</td>
<td>43</td>
<td>10</td>
<td>67.5</td>
<td>70.5</td>
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THE PRO’s of using silicon

- **COST**
  
  CMOS ~ 1.5c/mm² - SiGe BiCMOS ~2.5c/mm²
  GaAs PHEMT ~ 4-7c/mm² - GaAs HBT ~5-10c/mm²

- **CAPACITY**
  
  Can use Si foundries are large, essentially ‘infinite’ capacity for needs of general PA’s, on a constant cost-cutting well established reduction curve.

- **INTEGRATION**
  
  Unlike III-V’s, allows the integration of digital, analog, power management with PA. Allows for the incorporation of self-test and calibration circuits.

- **ESD**
  
  Si technologies have well established ESD methodologies / structures.

- **THERMAL**
  
  Silicon has 3X better thermal conductivity than silicon, extremely important in PA reliability.
ISSUES in using silicon for PAs with respect to III-V technologies:

- **LOW BREAKDOWN**
  - BVDSS ~ 6-8V for CMOS (0.35-.5um),
  - BVCEO ~ 4-6V for SiGe HBTs
  (compare with 14-20V for III-V HBTs and PHEMTs)

- **RELIABILITY**
  - Relatively easy to show good performance on Si PA,
  - The hard task is to make it RELIABLE

- **HIGHER RON**
  - RON ~ 3 Ohm-mm for CMOS NFETs (0.35-0.5um)
  - RON ~ 1.5 Ohm-mm for PHEMT (0.35um)

- **LOWER GAIN/PAE**
  - 5-7% lower PAE at high band (1.8-2GHz)

- **INFERIOR PASSIVES**
  - Lossy silicon substrates creates significantly worse
  Inductor and Capacitor Q
LDMOS

Laterally-Diffused Metal Oxide Semiconductor

Offset drain provides much higher breakdown voltage than digital CMOS
(at cost of ft)

p+ contact at source avoids “hole” problem
can be used to ground source to backside
Laterally-Diffused Metal Oxide Semiconductor

Offset drain provides much higher breakdown voltage than digital CMOS (at cost of ft)

p+ contact at source avoids “hole” problem

can be used to ground source to backside

Lightly doped n-type
LDMOS Model: Approach 1

modelling approach: sub-circuit models

channel region
MM11

drift region
MM31

pro’s
• flexible
• charge partitioning channel / drift region

con’s
• uncontrolled node
• computation time / convergence

D. Klassen et al
LDMOS Transistors are current workhorses for Basestation PAs
LDMOS prices

Historically $1 / peak Watt
(Basestation PA 200W peak) => $200

With present heavy competition
$ 0.5 / peak Watt
GaAs MESFET

*GaAs-based Metal-Schottky FET*

- Low $R_{on}$, high $f_t$, high $BV$
- High $g_m$ compared with Si
- Microwave IC capability (S-I substrate)
- Typically depletion-mode (negative supply needed)
- $g_m$ varies with $V_{in}$
- $R_{out}$ moderate, varies with $f$ and $V_{ds}$
- Gate conducts at high bias, rectifies input signal

![GaAs MESFET Diagram]
If reverse bias on Schottky gate is increased, channel becomes more depleted, channel charge decreases.

Channel charge $Q \sim q \ N_d \ (a-w)$

$$w = \sqrt{\frac{2e(V+V_{bi})}{qNd}}$$

$\Rightarrow$ I-V curves similar to MOSFET
Gradual Channel Approx.

$$I_d = \frac{1}{2} C_{in} \mu W/L (V_{gs} - V_t)^2$$

in saturation region
Typically depletion mode
Ideosyncracies of GaAs and InP FETs

Gate forms a Schottky barrier with the channel *ie a diode!*
It conducts current if forward biased sufficiently
Generally about 0.7V is enough

Most FETs are n-channel and have $V_t < 0$
I.e they are on with $V_{gs} = 0$
$\Rightarrow$ Depletion mode devices

FETs with $V_t > 0$ can only operate with $V_t < V_{gs} < 0.7V$
which is not a large range!

Depletion-mode Power FETs have an annoying feature:
you must turn on the gate bias (to a negative value)
before turning on the drain bias. Otherwise they
can conduct a lot of current and can burn up!
DC vs Pulsed Id-Vds Characteristics of GaAs FET
Idealized Current Transient for III-V FET
How To Increase Breakdown Voltage in III-V FETs

Multiple gate recesses particularly on drain side
Just like "drain extension" MOSFET

Field plate
Modulates electric field at drain edge of gate
Just like LDMOS
HEMT

**GaAs-based High Electron Mobility FET**

Low Ron, high ft, high BV

Very high gm

Microwave IC capability (S-l substrate)

Typically depletion-mode  
(negative supply needed)

gm varies only slightly with Vin

Rout high, can be controlled

Gate conducts at high bias  
rectifies input signal
Channel Charge in HFETs Is like that of MOSFETs

Except:
1) The barrier layer is doped
2) There is a maximum charge - because of carrier spillover (finite barrier effects)
3) Quantum effects are important
GaAs Pseudomorphic HEMT (pHEMT)

- \( \text{In}_x \text{Ga}_{1-x} \text{As} \) channel, with \( 0.15 \leq x \leq 0.33 \)
  - Enhanced electron transport
  - Increased conduction band discontinuity, allowing higher channel current
  - Quantum well channel provides improved carrier confinement

- Power devices typically use “double heterojunction” layer structure

- Material grown by MBE or MOCVD

- Used for power amplifiers from 0.9 to 94 GHz
Ultrahigh Speed Transistors

Pseudomorphic In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As HEMTs
With an Ultrahigh $f_T$ of 562 GHz

Yoshimi Yamashita, Akira Endoh, Keisuke Shinohara, Kohki Hikosaka, Toshiaki Matsui, Member, IEEE,
Satoshi Hiyamizu, Fellow, IEEE, and Takashi Mimura, Fellow, IEEE

• Gate length 25 nm
• InGaAs channel with 70% In on InP substrate
A Curtice 2 model is used, with the parameters listed. The transistor shown has a gate width of 1 mm. (You can make larger devices - with larger current handling capability- by changing the area factor in the model instance).

Voltage breakdown is not included in model. BVds=12V

Note that GaAs FETs can have gate current at high Vgs.
Based on fitting \( g_m \)
\( A_c \) vs \( D_c \) \( g_m \) can be different
"Self-heating" correction

\[
I_{ds} = \frac{I_{ds}^{comp}}{1 + \frac{P_{diss}}{P_{eff}}}
\]

**Gm vs VGS:** complicated!

**ID vs VDS:**

\[
g_m = g_m^{comp} (1 + Kappa \times V_{ds}) \tanh \left( \frac{3 \times V_{ds}}{V_{sat}} \right)
\]

\[
I_{ds} = I_{ds}^{comp} (1 + Kappa \times V_{ds}) \tanh \left( \frac{3 \times V_{ds}}{V_{sat}} \right)
\]
Applications of E-pHEMT Technology for Cellular Handset Power Amplifiers

Shyh-Liang Fu, Pin-Fan Chen, Harry Yu, and Dave Wu
Wireless Semiconductor Division
Agilent Technologies, San Jose, CA

Load-Pull for PAE Tuning

Gain (dB)
PAE (%)
Pout (dBm)
Heterojunction Bipolar Transistors

GaAs HBT

SiGe HBT
Pros

- High microwave gain
- High power density = small die size
- Straightforward fabrication
  (simple lithography
  no Vth control problems)
- Single power supply
- High efficiency
- Good linearity

Cons

- Thermal issues
  (including thermal runaway)
- Finite base current
- Saturation charge storage
GaAs HBT Power Amplifier Example

WCDMA

Fig. 6. Cross sectional view of the MCM.
Model for GaAs/GaInP HBT
Gummel-Poon

The transistor has overall emitter area 3200um² (40 fingers x 2um x 20um).
Absolute highest \( I_c = 1.9 \text{A} \) (0.6mA/um²).
\( Bv_{ce} = 10 \text{V}, \ Bv_{cb} = 20 \text{V} \). Model does not include these limits. Ballasting is not included in this model.

Larger devices can be made by changing area factor.
Model for GaAs/GaInP HBT VBIC

The transistor has overall emitter area 3200um² as for G-P model. Thermal sub-circuit is included, so DC self-heating effect on beta is observed.
Breakdown Voltage Definitions

BVceo: Breakdown voltage between C and E, with third terminal (base) open
BVces: Breakdown voltage between C and E, with third terminal (base) shorted to ground (E)
BVcbo: Breakdown voltage between C and B, with third terminal (emitter) open

\[ V_{ce} = V_{cb} + V_{be} \]
For BVces: base is shorted to emitter, so \( V_{be} = 0 \)
BVces is BV of BC diode with emitter tied to base

BVcbo is BV of BC diode with emitter open \( = \) BVces

Off-state breakdown: BV at zero bias current
On-state breakdown: BV at high bias current

\[ \text{BVceo} < \text{BVces} \]
On-state BV < Off-state BV
High Voltage Breakdown Mechanism of Bipolar Transistor

Impact ionization in BC depletion region

What happens to holes generated by impact ionization?
They flow to the base.
For short circuited base, they flow out of the base.
For open circuited base, they stick around in base!
To maximize breakdown voltage in bipolar transistors:

*When using common emitter configuration*
Drive base with a low impedance source not a current source

Or

Use common base configuration

Or

Use cascode connection
Gain vs Frequency

Common emitter

Common base

Common-base
Common-emitter
Cascode
Bias Circuit Considerations

Do not want to short out RF input signal
Want temperature independent bias

Often use current mirror
Use smaller device to set bias, to conserve power

Basic circuits:

- $V_{bias}$
- $V_{batt}$ or $V_{ref}$ (can be BG reference)
- $Q_{helper}$ supplies current to feed bases
- This provides low impedance near dc
- This provides low impedance at rf
Thermal Runaway in BJTs and HBTs

At high $V_{ce}$, dc behavior of $I_c$ vs $V_{be}$ shows increasing $gm$, then infinite $gm$, then negative $gm$

$\Rightarrow$ Multivalued $I_c$

Current splits between hot and cold fingers
Self-Heating Effects: Current Collapse

\[ T = T_{th} + R_{th} \cdot I_c \cdot V_{ce} \]

\[ I_c = \frac{g_D \cdot n^2_{ib}(T)}{p_{bw}} \cdot e^{\frac{q \cdot V_{be}}{kT}} \Rightarrow \left. \frac{\partial V_{be}}{\partial T} \right|_{I_c} = -1 \text{ to } -2 \frac{mV}{^\circ C} \]

\[ \frac{dV_{be}}{dI_c} = \left. \frac{\partial V_{be}}{\partial I_c} \right|_T + \left. \frac{\partial V_{be}}{\partial T} \right|_{I_c} \cdot \frac{dT}{dI_c} \]

\[ \frac{KT}{qI_c} + \frac{R e}{\alpha} + \frac{R B}{\beta} \approx 1 \Omega \]

\[ -1.5 \frac{mV}{^\circ C} \]

\[ R_{th} \cdot V_{ce} \]

\[ \text{Ex: } \frac{1^\circ C}{mW} \cdot 0.5V \]

\[ -1.5 \times 1 \times 5 = -7.5 \Omega \]

Produces current hogging by the hottest finger of a large HBT
Bipolar Ic-Vce Curves with Thermal Runaway

HBT

BJT
(no heterojunction)
Solution to thermal runaway

Include extra resistances in emitter fingers (ballast resistors) to keep gm finite

Costs in gain and efficiency

Can put ballast resistors in base input (use value Reballast*beta)

In principle ballast resistors can be shorted by capacitors to avoid drop in gain (but capacitors have to be very big and numerous)

Add extra Rb till

\[
\frac{R_E}{\alpha} + \frac{R_B}{\beta} + \frac{KT}{qI_C} > R_{th}V_{CE }\frac{\partial V_{BE}}{\partial T}\left|_{I_C}\right.
\]
How To Cope With Thermal Runaway

Emitter Ballast

Base Ballast

For higher microwave gain
Thermal Instability in Bias Circuits

Analogous to thermal runaway problem with multifingered bipolar transistors

Power transistor has high power dissipation: \( I_cV_{ce} \)

Then heats up. Then \( V_{be} \) is smaller for a given current

Want to include series \( R \) in emitter legs (or in base legs)  **but not too much**

Can use \( R \) in base legs to provide RF isolation too
Input Impedance of Bias Circuits

For "dc", the bias circuit can provide a current source, or a voltage source (or more generally, an arbitrary impedance) The impedance can be frequency dependent - with changing values over the baseband frequency response of the amplifier.

Choices made for the \( \text{Zin}(\omega) \) of the bias circuit can affect breakdown and linearity.

For breakdown considerations - recall that for bipolar transistors, \( Bvces \) (or \( Bvcb \)) is larger than \( Bvceo \) (since hole current created by avalanching can leak out of the base) So want a low dc resistance for the bias circuit.

Linearity effects are dominated by self-biasing.
In Power Amplifiers
For Heavy Lifting
Use Wide Bandgap Semiconductors
Wide Bandgap Material Properties

**Breakdown Electric Field (MV/cm)**
- GaN
- SiC 4H
- InP
- GaAs
- Si

**Thermal conductivity (W cm/K)**
- diamond
- sapphire
- GaN
- SiC 4H
- InP
- GaAs
- Si
Electron Transport Characteristics

Mobility
(FET channels - cm^2/Vs)

<table>
<thead>
<tr>
<th>Material</th>
<th>Mobility</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs FET</td>
<td>4500</td>
</tr>
<tr>
<td>GaAs PHEMT</td>
<td>6000</td>
</tr>
<tr>
<td>InP HEMT</td>
<td>10000</td>
</tr>
<tr>
<td>Si</td>
<td>500</td>
</tr>
<tr>
<td>SiC 4H</td>
<td>400</td>
</tr>
<tr>
<td>GaN HFET</td>
<td>1500</td>
</tr>
</tbody>
</table>
GaN Properties

- Wurtzite Crystal Structure
- $E_g = 3.4 \text{ eV}$
- $E_{br} = 3 \text{MV/cm}$
- $V_{sat} = 2.5 \times 10^7 \text{ cm/s}$
- Defect Density $10^8-10^{10}/\text{cm}^2$
Polarization in Nitride HFETs

Polarization in GaAs: \[ P = P_{\text{spont}} + P_{pz} \] all \( z \) directed

\[ P_{pz} = 2 d_{31} \sigma_{xx} \]

\[ \sigma_{xx} = \sigma_{yy} \]
\[ \sigma_{zz} = 0 \] (free surface)

Note strain \( \varepsilon_{xx} = \varepsilon_{yy} \), also have \( \varepsilon_{zz} = -\nu \varepsilon_{xx} \)

\[ P_{pz} = 2 e_{31} \varepsilon_{xx} + e_{33} \varepsilon_{zz} \]
ALGaN/GaN HFET structure

- 2DEG
- Field plate $L_{FP}$
- SiC substrate
- Metal
- GaN
- AlGaN
- $T_{SiNx}$
- Surface states
- $\sigma_{2DEG}$
- $\sigma_{surf states}$
- $\sigma_{sp} + \sigma_{pz}$
- $\sigma_{metal}$
Power Density Limits

\[ P_{\text{max}} = \frac{1}{8} \ V_{\text{max}} \ J_{\text{max}} \]

\[ V_{\text{max}} = E_b k \ wc \]
limited by breakdown

\[ J_{\text{max}} = q \ vsat \ N_d \]
limited by channel doping (HFET)
or by Kirk effect (HBT)

\[ N_d \sim \varepsilon \ E_b k / q \ wc \]

\[ \Rightarrow P_{\text{max}} \sim \varepsilon \ E_b k^2 \ v_{\text{sat}} \]

For GaN,
Pmax is 70x higher than for GaAs !!

For HBT, we=1um, Pmax= 200W/mm !!
Output Impedance and High Frequency Limits

Power from a single “transistor” limited by $R_{out} \sim 1 \text{ ohm}$ in order to match to 50 ohms with reasonable efficiency

$$P_{out} \sim \frac{V_{bk}^2}{R_{out\ min}}$$

50 x higher for GaN than for GaAs!!

Efficient power amplifier requires $ft > 3 f_{op}$

Johnson figure of merit:

$$BV \times ft \sim Ebk \times vsat$$

10x higher in GaN than in GaAs!!

Caution:
$BV$ and $ft$
need not be simultaneous
GaN on SiC: The Thermal Advantage

- SiC has a very high thermal conductivity of 4.9 W/cm-K
  - GaAs: 0.4, Si: 1.5, Sapphire: 0.4

- Gate pitch with Silicon

- Gate pitch with SiC

- Gate pitch with Silicon
  - Gate pitch with SiC

- SiC delivers higher power from given chip area => SiC has higher W/mm² => reduces $/W

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2. These I-V curves were measured from a commercial GaN transistor under DC (blue), pulsed with cold QP (green), and pulsed with hot QP (red) conditions.