ECE 145C/218C Homework #3

1) 18 pts. Consider the 2 stage amplifier shown below. The drain efficiency and gain for the driver amplifier are 20% and 12 dB, and for the power stage, they are 45% and 7 dB, respectively.
   a. Compute the power-added efficiency for each stage, and the drain efficiency and power-added efficiency of the combined circuit. (7)
   b. If the RF output power of the final stage is 0.5 W, how much power is dissipated as heat in the final stage? (5)
   c. Repeat a. and b. for the case where the gain of the output stage is 13 dB. (6)

2) 21 pts. Consider an amplifier needed for a wireless local area network (WLAN) using the 802.11g air interface standard. The associated OFDM signal has peak-to-average power ratio of 9 dB (after "de-cresting", a procedure of reducing the PAPR in a way that minimizes the signal distortion). The average output power of the amplifier must be 20 dBm, so the peak power must be 29 dBm. Assume that you are working with an FET technology where the maximum output voltage is limited to 3 V (due to breakdown and hot carrier effects), and the maximum output current per unit gate width is 350 mA/mm. You may select the power supply voltage to be anything you wish.
   a. What size device (ie what gate width) is needed to construct the amplifier assuming a simple Class A architecture? (5)
   b. What is the load resistance that must be used? (6)
   c. What is the power supply voltage that you should choose? (3)
   d. For initial computations you may assume that the Ron value is zero. Refine your computations (in approximate way) by assuming that the value of Vmin (="knee voltage" of the transistor) is 0.8 V. (7)
3) 42 pts. Imagine you are designing a power amplifier for a cellular handset operating at 1.9 GHz, and that the transistor used for the final stage has $I_d-V_{ds}$ characteristics such as given in the figure below (this a slightly idealized "plain vanilla" FET). Assume that the power supply voltage that you have to work with is 3.6V (this is the typical voltage for a Li ion battery).

![Id-Vds Characteristics](image)

a. Determine the maximum output power that you can expect to achieve from this device assuming class A operation (without overdriving the input or causing any clipping of the output). Note that you are not allowed to change the power supply or the width of the device (so the maximum current is fixed as stated in the figure). (6)

b. What is the load resistance that you would choose for the device to achieve maximum power? You may assume, for the moment, that there are no parasitic capacitances or inductances. (4)

c. What is the maximum efficiency that you could expect from the amplifier when operated in this condition of maximum power, if there were no losses in the impedance matching network in Class A? (5)

d. Suppose you have constructed the amplifier in the manner described by your answers to a, b, and c. Now you are told to operate the amplifier with a power supply voltage of 2.5V. If you do not change the amplifier (that is, the RL that you chose remains the same as above), what will be the maximum power that you can now achieve with the amplifier? (5)

e. What will be the efficiency if you do not change the RL value from the answer given in part b? (5)

f. What will be the maximum power if now you are allowed to change and optimize RL for this reduced Vdd value? (3)

g. What will be the efficiency if you do change the RL value to what is given in part f, at maximum power? (4)
h. Consider now that the device has some output capacitance $C_{ds}$. Suppose the value of capacitance is such that $1/\omega C_{ds} = RL$ as you calculated in part b (no matter what RL you got, just to make numerical calculations easy!). With a 3.6V power supply once again, if you do not change the matching from part a-b-c (that is, you have only a resistor RL) and use the same bias current, estimate what is the highest output power that you could expect to get without distortion from clipping or saturation. Repeat the estimation if you are allowed to use an appropriately configured matching network at the output that can account for $C_{ds}$ at your operating frequency. (6)

i. You are told that the device will be operated with an input signal that has a peak to average power ratio of 7dB, and that you must be able to amplify the peaks of the signal without clipping them. The average output power is thus 5x lower than the peak power. Estimate what the highest average efficiency of the power amplifier will be for this condition. You may assume the power supply of 3.6V, as described in part a-b-c, and Class A operation. (For this and for the following you may ignore the output capacitance $C_{ds}$). Note here you are not told what the probability density function of the signal is, so you are not expected to provide a highly accurate answer just an engineering approximation. (4)