ECE 2C, notes set 5: Fundamentals of Transistor Amplifiers (part II)

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Goals:

Practice DC bias analysis of transistor * circuits

Practice AC small - signal analysis of transistor * circuits

* or any nonlinear circuit element
(diode, Vacuum tube, tunnel junction, ...)

Comment (1): DC bias design in real circuits.

In developing our simple amplifier study, we have provided DC input bias with a battery.

Clearly not real. But OK for now.

Bias structures in real ICs: as shown

1950's style
RC biasing

Direct coupled (IC style)

LC biased (and tuned)
RF - IC style
Comment (2): bias design: DC-coupling.

Direct - Coupled amplifier/IC designs:
DC output voltage on one stage = DC input voltage of the next.
Need skill & creativity to fit together DC bias requirements of all stages
→ ECE137AB
Comment (3): bias design: AC/RC-coupling.

AC - Coupled amplifiers:
DC bias conditions set by resistors
Blocking capacitors isolate DC levels between stages.
Very low - frequency signals are not amplified.
We will *briefly* study such circuits
...mostly as an exercise in frequency response analysis.
Again, more detailed study in ECE137AB
Current Mirrors: First Treatment

Used in DC coupled circuits:
  to provide (to set) DC bias currents.
  as an active load (discuss later)

We now consider only basic operation
Current mirror DC bias analysis (1)

Example Parameters:

- **FET Q1:**
  \[
  (\mu c_{ox} W_g / 2L_g) = 1\text{mA/V}^2
  \]
  \[
  V_{th} = 0.3 \text{ V}
  \]
  \[
  1/ \lambda = 10\text{V}
  \]

- **FET Q1:**
  \[
  (\mu c_{ox} W_g / 2L_g) = 2\text{mA/V}^2
  \]
  \[
  V_{th} = 0.3 \text{ V}
  \]
  \[
  1/ \lambda = 10\text{V}
  \]

- **Circuit**
  \[
  V_{dd} = 2.5 \text{ V}
  \]
  \[
  R_L = 1.0 \text{ k}\Omega
  \]

Let us set \( I_{D1} = 0.1 \text{ mA} \).

**Analysis:**

\[
I_{D1} = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2(1 + \lambda V_{DS})
\]

\[0.1 \text{ mA} = (1 \text{ mA/V}^2)(V_{gs} - 0.3 \text{ V})^2(\lambda V_{DS} \text{ term neglected})\]

\[
(V_{gs} - 0.3 \text{ V}) = \sqrt{0.1 \text{ mA}/1 \text{ mA/V}^2} = 0.316 \text{ V}
\]

\[
V_{gs} = 0.616\text{ V}.
\]

\[
R_{ref} = (V_{DD} - V_{gs}) / I_{D1} = (2.5\text{ V} - 0.616\text{ V})/(0.1 \text{ mA})
\]

\[
R_{ref} = 18.8 \text{ k}\Omega.
\]

*we are again ignoring the \((1 + \lambda V_{DS})\) term in the bias analysis.

Doing this causes some significant error.

In ECE137A we will learn some tricks to calculate this quickly yet fairly accurately.

Do not ignore the \((1 + \lambda V_{DS})\) term in the small signal analysis.
Current mirror DC bias analysis (2)

Example Parameters:

FET Q1: $\mu c_{ox} W_g / 2L_g = 1\text{mA/V}^2$

FET Q1: $(\mu c_{ox} W_g / 2L_g) = 2\text{mA/V}^2$

$V_{th} = 0.3 \text{ V}$

$V_{th} = 0.3 \text{ V}$

$1/\lambda = 10\text{V}$

$1/\lambda = 10\text{V}$

Now find the current in the output branch.

Analysis:

$I_{D2} = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2(1 + \lambda V_{DS})$

$I_{D2} = (2 \text{mA/V}^2)(0.613\text{V} - 0.3\text{V})^2(\lambda V_{DS} \text{term neglected})$

$I_{D2} = 0.2 \text{mA}$

$V_{D2} = V_{DD} - I_{D2}R_L = 2.5\text{V} - (0.2 \text{mA})(1\text{k}\Omega)$

$V_{D2} = 2.3 \text{V}$

If $R_L$ is not large, $V_{DS}$ of Q2 will be more than the knee voltage and will provide 1mA to the load regardless of the value of $R_L$.

$\rightarrow$ constant - current source

*we are again ignoring the $(1 + \lambda V_{DS})$ term in the bias analysis.

Doing this causes some significant error.

In ECE137A we will learn some tricks to calculate this quickly yet fairly accurately.

Do not ignore the $(1 + \lambda V_{DS})$ term in the small signal analysis.
Current Mirrors: Constant-Current Source

If the \((1 + \lambda V_{DS})\) term is small, mirror provides nearly constant current over a wide range of load resistances, i.e. over a wide range of voltages.

The \((1 + \lambda V_{DS})\) term causes a significant variation of load current as the output voltage (or the load resistance) is varied.
Differential Amplifiers

Amplifies the difference between two input voltages $V_{in}^+$ and $V_{in}^-$. Also makes DC-coupled IC design easier. Widely used.

Current source:
typically a current mirror.

Here: treat it as an ideal DC current source.
Differential Amplifier: DC bias analysis

FETs $Q_1, Q_2$:

$$ (\mu c_{ox} W_g / 2L_g ) = 1 \text{mA/V}^2 $$

$$ V_{th} = 0.3 \text{V} $$

$$ 1 / \lambda = 10 \text{V} $$

$$ I_{SS} = 1 / 2 \text{mA} $$

Circuit

$$ V_{dd} = 2.5 \text{V} $$

$$ R_L = 8 \text{k}\Omega $$

From symmetry: $I_{D1} = I_{D2} = I_{SS} / 2 = 0.25 \text{mA}$

$$ I_{D2} = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2 (1 + \lambda V_{DS}) $$

$$ 0.25 \text{mA} = (1 \text{mA/V}^2)(V_{gs} - 0.3 \text{V})^2 (\lambda V_{DS} \text{term neglected}) $$

$$ (V_{gs} - 0.3 \text{V}) = \sqrt{(0.25 \text{mA})/(1 \text{mA/V}^2)} \rightarrow V_{gs} = 0.80 \text{V} $$

$$ V_s = V_g - V_{gs} = 0 \text{V} - 0.80 \text{V} = -0.80 \text{V} $$

$$ V_D = V_{DD} - I_D R_L = 2.5 \text{V} - (0.25 \text{mA})(8 \text{k}\Omega) = 0.5 \text{V} $$
FETs \( Q_1, Q_2 \):

\[
(\mu c_{ox} W_g / 2 L_g) = 1 \text{mA/V}^2 \\
V_{th} = 0.3 \text{V} \quad I_D = 1/4 \text{mA} \\
1/\lambda = 10 \text{V} \quad V_{gs} = 0.8 \text{V}
\]

Once again, we must use the DC bias conditions to calculate the FET small-signal parameters:

\[
I_D = (\mu c_{ox} W_g / 2 L_g)(V_{gs} - V_{th})^2 (1 + \lambda V_{DS}) \\
g_m = (\mu c_{ox} W_g / L_g)(V_{gs} - V_{th})(1 + \lambda V_{DS}) \\
= (2\text{mA/V}^2)(0.8\text{V} - 0.3\text{V})(1+1.3\text{V}/10\text{V}) \\
= 1.13 \text{mS}
\]

\[
G_{ds} = \frac{1}{R_{ds}} \approx \lambda I_D \quad \frac{0.25 \text{mA}}{10\text{V}} = 25 \mu \text{S} = \frac{1}{40k\Omega}
\]
Before we analyze this problem, let us make it simpler.

→ differential and common-mode signals
Differential and Common-Mode Signals: Input

\[ V_{in}^+ = V_{in,cm} + \frac{V_{in,d}}{2} \]

\[ V_{in}^- = V_{in,cm} - \frac{V_{in,d}}{2} \]

\[ V_{in,D} = \text{differential input voltage} = V_{in}^+ - V_{in}^- \]

\[ V_{in,CM} = \text{common - mode (average) input voltage} = \frac{(V_{in}^+ - V_{in}^-)}{2} \]

\[
\begin{align*}
V_{in,d} &= V_{in}^+ - V_{in}^- \\
V_{in,cm} &= \frac{(V_{in}^+ - V_{in}^-)}{2}
\end{align*}
\]

\[
\begin{align*}
V_{in}^+ &= V_{in,cm} + \frac{V_{in,d}}{2} \\
V_{in}^- &= V_{in,cm} - \frac{V_{in,d}}{2}
\end{align*}
\]
Differential and Common-Mode Signals: Output

\[ V_{out}^- = V_{out,cm} - \frac{V_{out,d}}{2} \]

\[ V_{out}^+ = V_{out,cm} + \frac{V_{out,d}}{2} \]

\[ V_{out,d} = \text{differential output voltage} = V_{out}^+ - V_{out}^- \]

\[ V_{out,cm} = \text{common-mode (average) output voltage} = \frac{(V_{out}^+ - V_{out}^-)}{2} \]

\[ V_{out,d} = V_{out}^+ - V_{out}^- \]

\[ V_{out,cm} = \frac{(V_{out}^+ - V_{out}^-)}{2} \]
Analysis: Use the principle of superposition

The \((V_{in}^+, V_{in}^-)\) inputs can always be written as a superposition of \(V_d\) and \(V_{cm}\).

So, analyze the circuit for *differential* and *common-mode* gain.

To find \(V_{out}^+\) and \(V_{out}^-\), write the input as sum of \(V_{in,d}\) and \(V_{in,cm}\),
multiply \(V_{in,d}\) by the differential gain to get \(V_{out,d}\),
multiply \(V_{in,cm}\) by the common-mode gain to get \(V_{out,cm}\),
(if you want) find \(V_{out}^+\) and \(V_{out}^-\) using

\[ V_{out}^+ = V_{out,cm} + \frac{V_{in,d}}{2}, \quad V_{out}^- = V_{out,cm} - \frac{V_{in,d}}{2} \]
Differential gain

From symmetry, the small-signal voltage at this point must be zero.

So, it makes no difference if we ground this point. This is called a virtual ground.
Differential gain

From symmetry, all the voltages on the right side are negatives of those on the left.

..and, the virtual ground has broken the connection between the 2 sides of the circuit.

So, we can throw the right side away!
Differential gain: analysis

The circuit is now the same as a common-source stage. Be careful, however:

\[ V_{in} \text{ has become } \frac{V_d}{2}, \quad V_{out} \text{ has become } -\frac{V_d}{2} \]

Parameters:

- FET:
  - Circuit
    - \( g_m = 1.13 \text{ mS} \)
  - \( R_L = 8\text{k}\Omega \)
  - \( R_{DS} = 40\text{k}\Omega \)

Equivalent load resistance

\[ R_{L,eq} = R_L \parallel R_{DS} = 40\text{k}\Omega \parallel 8\text{k}\Omega = 6.666 \text{k}\Omega \]

Voltage gain

\[ \frac{V_{out}}{V_{in}} = -g_m R_{Leq} = -(1.13\text{mS})(6.66\text{k}\Omega) = -7.53 \]

But \( V_{in} = \frac{V_{in,d}}{2} \) and \( V_{out} = -\frac{V_{out,D}}{2} \), so:

\[ A_D = \frac{V_{out,D}}{V_{in,D}} = -\frac{V_{out}}{V_{in}} = +g_m R_{Leq} = +7.53 \]

The circuit has a differential gain of 7.53
Common-mode gain

From symmetry, the small-signal current in this wire must be zero.

So, it makes no difference if we cut this wire. This (should be) called a virtual open.
Common-mode gain

From symmetry, all the voltages on the right side are *the same as* those on the left.

...and, the virtual open has broken the connection between the 2 sides of the circuit.

So, again, we can throw the right side away!
Common-mode: analysis

The FET source has no connection
→ the source current is zero.
→ the drain current is zero.
→ the common-mode output voltage is zero.

\[ A_{cm} = \frac{V_{out,cm}}{V_{in,cm}} = 0 \]

Note:
This is an extremely idealized analysis.
We have assumed that the small-signal impedance of the current source is infinite.
This results in zero common-mode gain.

With a finite output resistance to the current source the common-mode gain will be small, but not zero.

We will analyze this in ECE137AB
Differential Amplifiers: Recap

\[ V_{in}^+ = V_{in,cm} + \frac{V_{in,d}}{2} \]

\[ V_{in}^- = V_{in,cm} - \frac{V_{in,d}}{2} \]

\[ V_{in,d} = V_{in}^+ - V_{in}^- \]

\[ V_{in,cm} = \frac{(V_{in}^+ - V_{in}^-)}{2} \]

\[ V_{out}^+ = V_{out,cm} + \frac{V_{out,d}}{2} \]

\[ V_{out}^- = V_{out,cm} - \frac{V_{out,d}}{2} \]

\[ V_{out,d} = A_d V_{in,d} \quad \text{where} \quad A_d = g_m R_{Leq} \]

\[ V_{out,cm} = A_{cm} V_{in,cm} \quad \text{where} \quad A_{cm} \rightarrow 0 \text{ if the current-source impedance is high} \]

\[ V_{out,d} = V_{out}^+ - V_{out}^- \]

\[ V_{out,cm} = \frac{(V_{out}^+ - V_{out}^-)}{2} \]
Differential Amplifiers: Applications

One application: amplifying the difference between two voltages seen in precision instrumentation, in op-amp input stages.

Another application: ease of design of DC-coupled stages.

→ Look at one simple example.
Example: Two-Stage Differential Amplifier

A pair of cascaded differential stages.
The differential design, and the NFET/PFET alternation, make it easy to design an amplifier with DC coupling and with zero volts DC at input and output.
Two-stage differential amplifier: DC bias analysis

All FETs
$(\mu c_{ox} W_g / 2 L_g) = 1 \text{mA/V}^2$

$|V_{th}| = 0.3 \text{V}$

$1 / \lambda = 10 \text{V}$

Circuit
$V_{dd} = 2.5 \text{ V}$
$V_{ss} = -2.5 \text{ V}$
$R_{L1,2} = 8 \text{ k}\Omega$
$R_{L3,4} = 10 \text{ k}\Omega$
$I_{SS1} = 1/2 \text{ mA}$
$I_{SS2} = 1/2 \text{ mA}$

The 1st stage is taken from the prior example.
$\rightarrow$ same DC bias conditions

Second stage bias conditions
From symmetry: $I_{D3} = I_{D4} = I_{SS2} / 2 = 0.25 \text{ mA}$

$I_{D2} = (\mu c_{ox} W_g / 2 L_g) (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$

$0.25\text{mA} = (1 \text{mA/V}^2)(V_{gs} - 0.3\text{V})^2 (\lambda V_{DS}\text{ term neglected})$

$(V_{gs} - 0.3\text{V}) = \sqrt{(0.25\text{mA})/(1 \text{mA/V}^2)} \rightarrow V_{gs} = 0.80\text{V}$

The gate is *more negative* than the source, so

$V_s = V_g + V_{gs} = 0.5\text{V} + 0.80\text{V} = 1.30\text{V}$

$V_D = -V_{SS} + I_D R_L = -2.5\text{V} - (0.25 \text{mA})(10\text{k}\Omega) = 0.0\text{V}$
Two-stage differential amplifier: s.s. parameters

The calculations are identical to those of the previous example, and all FETs have the same values for $\left(\mu c_{ox} W g / 2 L g \right)$ and $\lambda$.

$\rightarrow g_m = 1.13 \text{ mS}$

$\rightarrow G_{ds} = \frac{1}{R_{ds}} = 25 \mu S = \frac{1}{40k\Omega}$
In the small signal diagram at left, the supply voltages have been replaced by short-circuits, the supply currents have been replaced by open-circuits, but the transistors have not yet been replaced by their small-signal models.

This is a convention.

For a differential input, the indicated points have zero AC voltages and so can connected to virtual grounds.
Two-stage differential amplifier: s.s. analysis

Again, the virtual grounds allow us to delete half the circuit.

This leaves us with two cascade common-source stages.

Replace transistor symbols with small-signal models → AC small signal equivalent circuit
Two-stage differential amplifier: s.s. analysis

First stage (as before)
Equivalent load resistance
\[ R_{L,eq1} = R_L \parallel R_{DS1} = 40k\Omega \parallel 8k\Omega \]
\[ = 6.666 \text{ k}\Omega \]
Voltage gain
\[ \frac{V_{out}}{V_{in}} \bigg|_{\text{stage1}} = g_{m1}R_{Leq1} \]
\[ = (1.13\text{mS})(6.66 \text{ k}\Omega) \]
\[ = 7.53 \]

Second stage
Equivalent load resistance
\[ R_{L,eq2} = R_L \parallel R_{DS2} = 40k\Omega \parallel 10k\Omega \]
\[ = 8.0 \text{ k}\Omega \]
Voltage gain
\[ \frac{V_{out}}{V_{in}} \bigg|_{\text{stage2}} = g_{m2}R_{Leq2} \]
\[ = (1.13\text{mS})(8.0 \text{ k}\Omega) \]
\[ = 9.04 \]

2-stage amplifier
Overall Voltage gain
\[ \frac{V_{out}}{V_{in}} \bigg|_{\text{2 stages}} = A_{v1}A_{v2} \]
\[ = (7.53)(9.04) \]
\[ = 68.1 \]