High Speed Mixed Signal IC Design
Notes set 5:
Digital IC design at the Gate level

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High speed digital IC design at the transistor level

ECL and CML gate designs, DC design

circuit structures for and / or / xor / latches …

large-signal delay analysis, design for high speed

transmission line interconnects, signal distribution

power-delay relationships
Basic Gates, Logical Description

**And**

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**OR**

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**XOR (exclusive OR)**

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ECL gate, circa ~1965

This is an *OR/NOR gate….port 3 is high if ports 1 or 2 are high …port 4 is the logical complement of port 3
Emitter follower buffering of interconnect capacitance
(good ? Bad ?)

DC output swing is 400 Ohms * 1 mA = 400 mV.....IoRL in general
Minimum Input voltage swing is 2kT/q + 2IoRex.
Need IoRL >> (2kT/q + 2IoRex) for adequate noise margin
...typically 500-600 mV output swing employed

Current sources replaced by resistors or current mirrors
Problems with old-fashioned ECL gate

Gate is single-ended….differential ckt generally preferred
why ? (standard reasons given are not so convincing…)
one reason is 2:1 lower permissible logic swing, less power

Gate uses emitter followers on **output**….this can result in strong
transmission-line ringing…. 

Output impedance of emitter follower is
\[ Z_{out} \approx \frac{1}{g_m} + R_L \left( \frac{j f}{f_{\tau}} \right) \], which is inductive.
Load on receiving end is capacitive....
Line can ring strongly.

Partial mitigation : EF biased by pull-down resistor
on receiving end of line, biased at e.g. - 2 Volts...this consumes substantial power
Differential Gates, CML and ECL

CML

ECL

V_{ee}, buffer
Differential CML gate, other attributes

Operates with complementary inputs and outputs
Quite low power consumption, as not many pull-down current sources...
Differential CML gate, DC operation.

DC output swing is $\Delta V_{Logic} = I_o R_L$

DC linear input range is $\Delta V_{in} = 2kT/q + 2I_o R_{ex}$

Transistor operates at $V_{ce} = V_{be,on}$ when off

Transistor operates at $V_{ce} = V_{be,on} - I_o R_L$ when on

Need HBT with LOW $V_{ce,sat}$
Differential CML AND / NAND gate

2-input logic gates must be implemented using *series gated current steering*. 3 input gates would require cascading 2-level gates, or 3-level series current steering. 3 level current steering is faster, but needs a more negative supply. OR/NOR gate is created by taking complements of both inputs and output.
Differential Current-Steering Series-Gated Bipolar Logic Gates

CML

ECL
**HEMT Logic Gates**

**Direct-coupled FET logic**  
Need enhancement-mode and depletion-mode devices  
slow driving long wires  
single-ended…threshold problems with low $\Delta V$

**Source-Coupled FET logic:**  
Need a monolithic diode level-shift  
fairly high power due to source followers  
Source follows needed for level-shifting

**FET equivalent of CML:**  
Need a monolithic diode level-shift  
need enhancement mode device  
would be best for fast / low-power

Logic family plays strong role in power  
Need diodes for SCFL  
DCFL needs enhancement mode HEMTs:
the 6-transistor cell is often referred to as a Gilbert cell (originating with his analog multipliers…). Note that the whole gate requires 3 pull down current sources
emitter followers on high "A-level" inputs result in faster gate operation and larger Vce across switching transistors, at expense of considerably higher current consumption. Emitter followers are usually associated with gate inputs, not outputs.
Differential ECL AND / NAND gate

Same circuit structure as CML gate, except note added emitter followers on B level inputs and added diode level shifts on A-level inputs.
Differential ECL XOR gate
Driving Interconnects: EF associated with gate outputs

This can ring quite badly, due to inductive EF output impedance and capacitive CS input impedance.

\[ L_{eq} = \frac{R_L}{2\pi f_\tau} \]

\[ R_{out} = \left( \frac{R_L}{\beta} \right) + R_{ex} + \frac{1}{g_m} \]

\[ C_{in} = 2C_{cb} + C_{je} + \left( \frac{I_o}{\Delta V_{logic}} \right) \tau_f \]
Driving Interconnects, and basic power-delay products

sending end termination….matched termination…. line should not (ideally) ring…actually does due to receiving end capacitive load… logic swing is Io*Zo…with Zo of 100 Ohms typical, this requires 2 mA drive current for 200 mV logic swing in a 100 Ohm environment...
Driving Interconnects Receiving end termination

receiving end termination….matched termination…. line should not (ideally) ring…actually does due to transistor capacitances ...
logic swing is Io*Zo…with Zo of 100 Ohms typical, this requires 2 mA drive current for 200 mV logic swing in a 100 Ohm environment...
Double line termination

double matched termination….ringing more strongly suppressed, use where needed….

... logic swing is Io*Zo/2…with Zo of 100 Ohms typical, this requires 4 mA drive current for 200 mV logic swing in a 100 Ohm environment...
Unterminated lines

Here lines are not terminated. Acceptable only when line delay is short in comparison with risetimes of concern. A short unterminated line will act as a capacitive load; a long unterminated line will ring. More on this in a few slides.

...logic swing is $I_o*RL$...current consumption greatly reduced (and smaller HBTs used)....
terminated lines: delay due to wiring capacitance

If and only if $\tau_{\text{wire}} \ll T_{\text{rise/fall}}$, can treat as lumped interconnect.

If and only if $R_L \gg Z_{\text{wire}}$, then $L_{\text{wire}} / R_L \ll R_L C_{\text{wire}}$ & can ignore wiring inductance

Then:

$$C_{\text{wire}} = l_{\text{wire}} / v_{\text{wire}} Z_{\text{wire}} = \tau_{\text{wire}} / Z_{\text{wire}}$$

Charging time constant:

$$\tau_{\text{interconnect}} = R_L C_{\text{wire}} = \tau_{\text{wire}} \left( R_L / Z_{\text{wire}} \right) = \tau_{\text{wire}} \frac{\Delta V_{\text{logic}} / I_o}{Z_{\text{wire}}}$$
Power Consumption in ECL and CML with singly-terminated Lines

CML Gate:
Fast
emitter followers on lower level only
(level-shifting)
\[ V_{cc} = 3V_{be} + 300 \text{ mV} \]
\[ I = 3I_{\text{switched}} = 3*\Delta V_{\text{logic}}/Z_o \text{ (approx.)} \]

ECL Gate:
Adds emitter followers on upper level
Somewhat faster
\[ V_{cc} = 4V_{be} + 300 \text{ mV} \]
\[ I = 5I_{\text{switched}} = 5*\Delta V_{\text{logic}}/Z_o \text{ (approx.)} \]

\( \text{E}^2\text{CL Gate:} \)
Double emitter followers driving both levels
helps with \( \text{f/f}_\tau \), higher \( V_{ce} \) for high J/C
\[ V_{cc} = 5V_{be} + 300 \text{ mV} \]
\[ I = 7I_{\text{switched}} = 7*\Delta V_{\text{logic}}/Z_o \text{ (approx.)} \]

Need to use CML for low power
Power and Power-Delay Products

Device sized for 100 Ω load:
(300 mV ECL logic swing)
0.25 μm x 6 μm emitter
Jpeak=2 mA/μm^2
→ peak speed at 2 mA

Shorter stripe length device:
0.25 μm x 0.5 μm emitter
*peak speed at 250 μA bias*

The smaller device consumes 12:1 less power but cannot use terminated lines. The lines then act as capacitive parasitics, and circuit speed is reduced due to the resulting RLC_wire time constant.
Power-Delay Product for a “Baseline” Device
1 µm by 1 µm emitter

0.5 mA per transistor, 1.5 mA total for gate. 3.3 V supply

Power consumption:
- 5 mW @ FO=2

Power-delay product (assuming 5 ps delay):
25 fJ @ FO=2

\[ P \approx 3 \cdot (3.3V) \cdot (5 \cdot 10^4 \text{ A/cm}^2) \cdot (1 \mu m)^2 = 5 \text{ mW} \]

Wiring capacitance ignored
Power-Delay Product for Scaled Device

Design rules reduced to 0.1 µm
assume gate delay still - 4 ps

0.1 µm by 0.1 µm emitter
5 microamps per transistor

Power consumption:
- 50 µW @ FO=2

Power-delay product:
0.2 fJ @ FO=2

Wiring capacitance ignored

\[ P \approx 3 \times (3.3 V) \times (5 \times 10^4 \text{ A/cm}^2) \times (0.1 \mu\text{m})^2 = 50 \mu\text{W} \]
Low-power gates have large delay from wiring capacitance

\( \tau_{\text{interconnect}} = R_L C_{\text{wire}} / 2 = \tau_{\text{wire}} (R_L / 2Z_{\text{wire}}) = \tau_{\text{wire}} \frac{\Delta V_{\text{logic}}}{2I_o Z_{\text{wire}}} \)

\( \tau_{\text{gate}} = \tau_{\text{interconnect}} + \tau_{\text{transistor terms}} = \tau_{\text{wire}} \frac{\Delta V_{\text{logic}}}{2I_o Z_{\text{wire}}} + \tau_{\text{transistor terms}} \)

\( P_{\text{gate}} = V_{ee} NI_o, \) where \( N \) is the number of current sources per gate

\( \tau_{\text{gate}} P_{\text{gate}} = V_{ee} NI_o \tau_{\text{wire}} \frac{\Delta V_{\text{logic}}}{2I_o Z_{\text{wire}}} + V_{ee} NI_o \tau_{\text{transistor terms}} \)

\[
\frac{NV_{ee}(\Delta V_{\text{logic}})}{2} \frac{\tau_{\text{wire}}}{Z_{\text{wire}}} + V_{ee} NI_o \tau_{\text{transistor terms}}
\]

As transistors are scaled, becomes smaller, and power - delay product becomes interconnect - limited
Minimum allowable logic voltage swing

\[ \tau_{\text{gate}} P_{\text{gate}} = \frac{NV_{ee}(\Delta V_{\text{logic}})}{2} \frac{\tau_{\text{wire}}}{Z_{\text{wire}}} + V_{ee} NI_0 \tau_{\text{transistor terms}} \]

Interconnect - limited delay becomes smaller as \( \Delta V_{\text{logic}} \) is made smaller.
What are the limits to reducing \( \Delta V_{\text{logic}} \) ?

Linear input voltage range is \( 2kT / q + I_0 R_{\text{ex}} \)
\( \Delta V_{\text{logic}} \) must be several times this.
### Minimum Logic Voltage Swing

The linear input voltage range of the gate is

\[ \Delta V_{\text{linear}} = \frac{2kT}{q} + 2I_o R_{ex} \]

We need margin against signal degradation due to

- signal ringing (interconnects, circuit-level a2)
- gate-gate interference due to supply or ground coupling

This safety margin is called "noise" margin

has **absolutely nothing** to do with thermal noise \( \sqrt{4kTR\Delta f} \)

should instead be called "EMI + ringing" margin

In order to have adequate "noise" margin we need

\[ \Delta V_{\text{logic}} \sim 3 \Delta V_{\text{linear}} = \frac{6kT}{q} + 6I_o R_{ex} \sim 150 \text{ mV} + 6I_o R_{ex} \]
\[ \Delta V_{\text{logic}} > 3 \Delta V_{\text{linear}} = \frac{6kT}{q} + 6I_o R_{ex} \]

\[ \Delta V_{\text{linear}} = \frac{2kT}{q} + 2I_o R_{ex} \]
To tolerate ringing and EMI, $\Delta V_{\text{logic}}$ must be several times larger than $\Delta V_{\text{linear}}$. 
Circuits become interconnect limited

\[ \tau_{\text{gate}} P_{\text{gate}} = \frac{N V_{\text{ee}} (\Delta V_{\text{logic}})}{2} \frac{\tau_{\text{wire}}}{Z_{\text{wire}}} + V_{\text{ee}} N I_o \tau_{\text{transistor terms}} \]

Interconnect limits: as transistors are scaled, wiring capacitance dominates

Power\-delay becomes dependent only on supply voltage & logic voltage swing

independent of design rules, independent of transistor bandwidth
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<th>Power-delay product in interconnect limit</th>
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\[
P_{\text{gate}} T_{\text{prop}} = \frac{1}{2} C_{\text{wire}} V_{cc} \Delta V_{\text{logic}}
\]

**bipolar logic (static power)**

\[
P_{\text{gate}} / f_{\text{clock}} = \frac{1}{2} C_{\text{wire}} V_{cc} \Delta V_{\text{logic}}
\]

**CMOS logic (dynamic power)**

\[
\left( T_{\text{prop}} f_{\text{clock}} \right)^{-1} \approx \text{number gates between latches}
\]

For fast, low-power logic: reduce \( V_{cc} \Delta V_{\text{logic}} \)
The Interconnect Limit and Logic Gate Design

\[ A_v = \frac{R_L}{2kT/qI_2} = \frac{I_2 R_L}{2kT/q} = \frac{\Delta V_{\text{logic}}}{2kT/q} \]

Voltage Gain must be \( \gg 1 \)

So: \( \Delta V_{\text{logic}} = 10 \cdot \left(\frac{kT}{q}\right) \)

But: \( P_{\text{gate}} T_{\text{gate}} > \left(\frac{1}{2}\right)V_{cc}\Delta V_{\text{logic}}C_{\text{wire}} \)

\[ P_{\text{gate}} T_{\text{gate}} > \left(\frac{1}{2}\right)(1.5 \text{ Volt})(10 \cdot kT/q)C_{\text{wire}} \]

(power\cdot delay) is constrained by interconnects

a fast transistor doesn't result in a fast IC

**conclusion: a better circuit design is needed**

Similar derivation for CMOS (Meindl, Proc IEEE, 1995)
Wiring capacitance? What if we use terminated transmission lines? (which we often do...)

$$\Delta V_{\text{logic}} = I_o Z_0 > \text{about } 5 \times kT / q$$

$$P_{\text{gate}} = V_{ee} I_o = V_{ee} \Delta V_{\text{logic}} / Z_0$$

$$T_{\text{delay}} = T_{\text{gate}} + T_{\text{wire}}$$

$$T_{\text{wire}} = l_{\text{wire}} / v_{\text{wire}}$$

$$P_{\text{gate}} T_{\text{delay}} = T_{\text{gate}} (V_{ee} \Delta V_{\text{logic}} / Z_0) + T_{\text{wire}} (V_{ee} \Delta V_{\text{logic}} / Z_0)$$

$$P_{\text{gate}} T_{\text{delay}} > T_{\text{wire}} (V_{ee} \Delta V_{\text{logic}} / Z_0) = V_{ee} \Delta V_{\text{logic}} (l_{\text{wire}} / v_{\text{wire}} Z_0) = V_{ee} \Delta V_{\text{logic}} C_{\text{wire}}$$

so, even though “wiring capacitance” is no longer an accurate description, $CV_{cc} \Delta V_{\text{logic}}$ is still an accurate expression for the power-delay limit
When clock is high, output = input.
When clock is low, output = input at just before clock changed from high to low
Note the positive feedback pair which holds the output level when clock_bar is high
Cascading a pair of latches creates a circuit which reads the data input D, and outputs it as the value Q, *Only on a falling edge of clock* .... *output is otherwise held constant* .... MS latch is used as timing control element... output is a version of the input, but sampled only at falling edge of clock.
What are latches and MS latches used for?

timing control
in logic system, prop delays will be function of transition & critical path.
timing errors/fluctuations will accumulate…role of latch is to suppress this, restore timing.

decision element.
in ADCs and in communications receivers, must decide whether a signal exceeds / does not exceed a critical threshold
*at a particular set of points in time defined by a clock signal.*
E$^2$CL M/S Latch

Popular in Si/SiGe due to (1) $H_{21}^2$ current gain and (2) larger $V_{ce}$ across switching transistors helps $C_{cb}/I$ ratio
ECL M/S Latch connected as 2:1 static frequency divider
Fast ECL 2:1 static frequency divider

- inductive load
- transmission-line bus short signal path
- keep-alive bias currents
- emitter-follower damping
Logic Propagation delay analysis: start with one-level CML gate

First, basic assumptions: 2:1 fan-out, chain of identical gates
Basic Assumptions for Propagation delay analysis

Figure 4.1: a) Basic CML gate. b) HBT without parasitics. c) CML equivalent circuit used for calculating propagation delay.

Transistor is nonlinear, how do we solve?
Small - signal analysis: \( C_{s.s.} \equiv \frac{dQ}{dV}, g_m \equiv \frac{dI}{dV} \) etc.
Large - signal analysis: \( C_{s.s.} \equiv \frac{\Delta Q}{\Delta V}, g_m \equiv \frac{\Delta I}{\Delta V} \) etc.
where \( \Delta V \) is the logic swing.
Basic Assumptions for Propagation delay analysis

Large - signal analysis: \( C_{s.s.} \equiv \Delta Q / \Delta V, \quad g_m \equiv \Delta I / \Delta V \) etc.

This implies:

\[
g_m = \Delta I / \Delta V = I_o / I_o R_L = 1 / R_L << qI_o / kT
\]

\[
C_{be,diffusion} = \Delta Q / \Delta V = I_o \tau_f / \Delta V = \tau_f / R_L << I_o \tau_f / (kT / q) = g_m \tau_f
\]

\[
A_v = \Delta V_{out} / \Delta V_{in} = -1
\]

\[
C_{je,large\_signal} = \Delta Q / \Delta V = (\int_{V_{be,on}-\Delta V}^{V_{be,on}} C_{je}(v)dV) / \Delta V = C_{je,eff}
\]

\[
C_{cb,large\_signal} = \Delta Q / \Delta V = (C_{cb} \Delta V) / \Delta V = C_{cb}
\]

Note that large signal operation greatly reduces the effective values of \( g_m \) and the diffusion capacitance...by roughly a factor of 10. Logic speed is much more controlled by depletion capacitances than it is by HBT base and collector stored charge.
Why isn't base+collector transit time so important?

Diffusion capacitance:
\[ \delta Q_{\text{base}} = (\tau_b + \tau_c) \delta I_C \]
\[ = (\tau_b + \tau_c) \frac{dI_C}{dV_{be}} \delta V_{be} \]
\[ = \frac{(\tau_b + \tau_c)I_C}{kT/q} \delta V_{be} \]

...active only over \( kT/q \) voltage swing.

Under Large-Signal Operation:
\[ \Delta Q_{\text{base}} = (\tau_b + \tau_c)I_C \]
\[ = \frac{(\tau_b + \tau_c)I_{dc}}{\Delta V_{\text{LOGIC}}} \Delta V_{\text{LOGIC}} \]

Large-signal diffusion capacitance reduced by ratio of
\[ \left( \frac{\Delta V_{\text{LOGIC}}}{kT/q} \right), \text{ which is } \sim 10:1 \]

Depletion capacitances present over full voltage swing, no large-signal reduction
Gate Propagation delay analysis

We now solve for gate delay

Method: replace transistors with their *large-signal* models

Circuit has transfer function of

\[ \left[ \frac{V_{\text{out}}}{V_{\text{in}}} \right] = \left[ \frac{V_{\text{out}}}{V_{\text{in}}} \right]_{\text{mid-band}} \left( \frac{1 + b_1 s + b_2 s^2 + \ldots}{1 + a_1 s + a_2 s^2 + \ldots} \right) \]

It is elementary math to show that the *mean delay* of the transfer function is \((a_1 - b_1)\), hence \(1/2\) the mean delay (delay to the 50% switching points) is \(T_{\text{gate}} = (a_1 - b_1) / 2\)

Find \(a_1\) by the method of time constants

Find \(b_1 = \sum C_{be} / g_m - \sum C_{cb} / g_m, \text{large-signal} \)
Gate Propagation delay analysis

Note that although the methods appear to be quite different, MOTC delay analysis on the linearized (large - signal) circuit, is identical to delay analysis by the charge - control method,

e.g. \[ T_{\text{gate}} = \frac{1}{2} \sum \frac{\Delta Q}{\Delta I} = \frac{1}{2} \sum \frac{1}{\Delta I} \int_{V_{\text{low}}}^{V_{\text{high}}} C(v) dV \]

In both cases it is important to note that 2nd - order effects \( a_2 \) in the circuit transfer function are neglected. This means, specifically, that emitter - follower ringing is neglected, which is a serious limitation.
One-level CML Propagation delay analysis

Taking $T_{\text{prop}} = \tau \ln(2)$ is equivalent to assuming $(1 - \exp(-t/\tau))$ charging behaviour. To the level of accuracy of the assumptions used, we have instead assumed linear node charging with time, which gives $T_{\text{prop}} = \tau / 2$, e.g. $(1/2)$ the mean delay.
One-level CML Propagation delay analysis: fan-outs

Here we are analyzing a gate chain with a fan-out of 2:1
Simplifying treatment of fan-outs

$R_L$ is replaced by $2R_L$ by symmetry arguments. In order to count each parasitic capacitance ONCE per gate, we must consider only capacitors in the highlighted area.
Gate Delay Calculation

\[ a_1 = C_{be} (R_{bb} + NR_L) + C_{cbi} [(NR_L + R_{bb})(1 - A_v) + R_L] + C_{cbx} [NR_L (1 - A_v) + R_L] \]

\[ a_1 = \left[ C_{je} + \frac{I_o \tau_f}{\Delta V_{logic}} \right] R_{bb} + \frac{N \Delta V_{logic}}{I_o} + C_{cbi} \left[ R_{bb} + \frac{N \Delta V_{logic}}{I_o} \right] (1 + 1) + \frac{\Delta V_{logic}}{I_o} \]

\[ a_1 \]

\[ a_1 = C_{je} R_{bb} + C_{je} \frac{N \Delta V_{logic}}{I_o} + N \tau_f + R_{bb} \frac{I_o \tau_f}{\Delta V_{logic}} + (2N + 1) \left[ C_{cbx} + C_{cbi} \right] \frac{\Delta V_{logic}}{I_o} + C_{cbi} R_{bb} \]

\[ b_1 = -(C_{cbx} + C_{cbi})/g_m = -(C_{cbx} + C_{cbi})(\Delta V_{logic} / I_o) \]
Gate Delay Calculation: Single-level CML gate at N:1 fanout

\[ 2T_{\text{gate}} = C_{je} R_{bb} + C_{cbi} R_{bb} + N \tau_f \]

\[ + R_{bb} \frac{I_o \tau_f}{\Delta V_{\text{logic}}} \]

\[ + (2N + 2) \left[ C_{cbx} + C_{cbi} \left( \frac{\Delta V_{\text{logic}}}{I_o} \right) \right] + C_{je} \frac{N \Delta V_{\text{logic}}}{I_o} \]

Note that the \( C_{cb} (\Delta V_{\text{logic}} / I_o) \) and \( C_{je} (\Delta V_{\text{logic}} / I_o) \) terms usually dominate. This strongly favors the use of small logic swings and high current density.
Effect of Current Density

\[ 2T_{\text{gate}} = C_{je} R_{bb} + C_{cbi} R_{bb} + N \tau_f \]

\[ + R_{bb} \frac{J_o A_e \tau_f}{\Delta V_{\text{logic}}} + (2N + 2) \frac{\varepsilon A_c}{T_c} \left[ \frac{\Delta V_{\text{logic}}}{A_e J_o} \right] + C_{je} \frac{N \Delta V_{\text{logic}}}{A_e J_o} \]

\[ 2T_{\text{gate}} = C_{je} R_{bb} + C_{cbi} R_{bb} + N \tau_f \]

\[ + (R_{bb} A_e) \frac{J_o \tau_f}{\Delta V_{\text{logic}}} + (2N + 2) \frac{A_c}{A_e} \left[ \frac{\varepsilon \Delta V_{\text{logic}}}{T_c J_o} \right] + C_{je} \frac{N \Delta V_{\text{logic}}}{A_e J_o} \]
Effect of Logic Voltage Swing

\[
2T_{\text{gate}} = C_{je} R_{bb} + C_{cbi} R_{bb} + N \tau_f + R_{bb} \left( \frac{I_o \tau_f}{\Delta V_{\text{logic}}} \right) \\
+ (2N + 2) \left[ C_{cbx} + C_{cbi} \right] \left( \frac{\Delta V_{\text{logic}}}{I_o} \right) + NC_{je} \left( \frac{\Delta V_{\text{logic}}}{I_o} \right)
\]

Note that the linear input voltage range of the gate is

\[
\Delta V_{\text{linear}} = 2kT / q + 2I_o R_{ex}
\]

Recall than we need

\[
\Delta V_{\text{logic}} \sim > 3 \times \Delta V_{\text{linear}} = 6kT / q + 6I_o R_{ex} \sim 150 \text{ mV} + 6I_o R_{ex}
\]

Logic voltage swing should be as small as possible, consistent with this limit...the \( R_{bb} \left( \frac{I_o \tau_f}{\Delta V_{\text{logic}}} \right) \) term usually being nondominant.
Effect of Logic Voltage Swing

\[ 2T_{\text{gate}} = C_{je} R_{bb} + C_{cbi} R_{bb} + N \tau_f + R_{bb} \left( I_o \tau_f / \Delta V_{\text{logic}} \right) \]
\[ + (2N + 2) \left[ C_{cbx} + C_{cbi} \right] \left( \Delta V_{\text{logic}} / I_o \right) + NC_{je} \left( \Delta V_{\text{logic}} / I_o \right) \]

But

\[ \Delta V_{\text{logic}} \rightarrow 3 * \Delta V_{\text{linear}} = 6kT / q + 6I_o R_{ex} \sim 150 \text{ mV} + 6I_o R_{ex} \]

Note that \[ C_{cb} \left( \Delta V_{\text{logic}} / I_o \right) = \left( \varepsilon / T_c \right) \left( A_c / A_e \right) \left( \Delta V_{\text{logic}} / J_e \right) \]

Note that \[ I_0 R_{ex} = J_e \left( R_{ex} / A_e \right) \]

If we push up current density, we do reduce Ccb charging time, but we must reduce the emitter resistance per unit area. Otherwise, the voltage swing must increase, and no benefit is obtained.
Scaling Laws, Collector Current Density, $C_{cb}$ charging time

**Collector Field Collapse (Kirk Effect)**

$$V_{cb} + \phi > + (J / v_{sat} - qN_d)(T_c^2 / 2\varepsilon)$$

**Collector Depletion Layer Collapse**

$$V_{cb,\text{min}} + \phi > + (qN_d)(T_c^2 / 2\varepsilon)$$

$$\Rightarrow J_{\text{max}} = 2\varepsilon v_{sat} (V_{cb} + V_{cb,\text{min}} + 2\phi) / T_c^2$$

Note that $V_{be} \approx \phi$, hence $(V_{cb} + \phi) \approx V_{ce}$

$$C_{cb} \Delta V_{LOGIC} / I_C = (\varepsilon A_{\text{collector}} / T_c)(\Delta V_{LOGIC} / I_C) = \frac{\Delta V_{LOGIC}}{(V_{CE} + V_{CE,\text{min}})} \left( \frac{A_{\text{collector}}}{A_{\text{emitter}}} \right) \left( \frac{T_c}{2v_{sat}} \right)$$

Collector capacitance charging time is reduced by **thinning the collector** while increasing current.
ECL Propagation delay: upper-level circuit

again assume a fan-out of N:1
Simplify by assuming beta>>1, Ree>>Re.
Next key point:
Depending upon the details of the IC design, the emitter-followers may or may not switch.
For now, let us assume they do not.
We consequently use small-signal quantities for the EFs, and large-signal quantities for the CS transistors.
\[ a_1 \approx C_{c_{bx1}} N R_L + C_{c_{bi1}} (N R_L + R_{bb}) + (C_{je1} + \tau_f q I_{e1} / kT)(kT / q I_{e1}) \\
+ C_{c_{bx2}} \left[ (R_{ex1} + kT / q I_{e1})(1 + 1) + \Delta V_{\text{logic}} / I_0 \right] \\
+ C_{c_{bi2}} \left[ (R_{ex1} + kT / q I_{e1} + R_{bb2})(1 + 1) + \Delta V_{\text{logic}} / I_0 \right] \\
+ \left[ C_{je2} + (\tau_f I_o / \Delta V_{\text{logic}}) \right] R_{ex1} + kT / q I_{e1} + R_{bb2} \]

\[ b_1 = (C_{je1} + \tau_f q I_{e1} / kT)(kT / q I_{e1}) - (C_{c_{bx2}} + C_{c_{bi2}})(\Delta V_{\text{logic}} / I_0) \]

\[ 2T_{\text{gate}} = a_1 - b_1 = C_{c_{bx1}} N R_L + C_{c_{bi1}} (N R_L + R_{bb}) + (C_{c_{bx2}} + C_{c_{bi2}})(\Delta V_{\text{logic}} / I_0) \\
+ C_{c_{bx2}} \left[ 2(R_{ex1} + kT / q I_{e1}) + \Delta V_{\text{logic}} / I_0 \right] \\
+ C_{c_{bi2}} \left[ 2(R_{ex1} + kT / q I_{e1} + R_{bb2}) + \Delta V_{\text{logic}} / I_0 \right] \\
+ \left[ C_{je2} + (\tau_f I_o / \Delta V_{\text{logic}}) \right] R_{ex1} + kT / q I_{e1} + R_{bb2} \]
Writing $C_{cb} = C_{cbx} + C_{cbi}:

$$2T_{gate} = 2R_{bb2}C_{cbi2} + C_{cbi1}R_{bb1} + C_{je2}R_{bb2} + 2C_{cb2}[R_{ex1} + kT / qI_{e1}] + C_{je2}[R_{ex1} + kT / qI_{e1}] + \left(\tau_f I_o / \Delta V_{\text{logic}}\right)(kT / qI_{e1})$$

$$(\tau_f I_o / \Delta V_{\text{logic}})(R_{ex1} + R_{bb2}) + C_{cb1}N(\Delta V_{\text{logic}} / I_o) + 2C_{cb2}(\Delta V_{\text{logic}} / I_o)$$

Note that the net delay is a little smaller than CML due to

1) Reduced number of $R_L C_{cb}$ charging terms

2) *slight* improvement due to buffing $C_{be,\text{diff}2} = \tau_f I_o / \Delta V_{\text{logic}}$

3) Larger $V_{ce}$ permits increased $J$, hence improved $I_c / C_{cb}$ ratio
Do the emitter-followers switch ????

\[ \Delta I = C_L \Delta V_{\text{logic}} / \Delta T \]

\[ C_L = 2C_{cb} + C_{je} + (I_o \tau_f / \Delta V_{\text{logic}}) \]
Do the emitter-followers switch ????

There are 2 dangers. First, on a rising pulse, the peak EF current is:

\[ I_{ef,peak} = I_{ef} + \Delta I = I_{ef} + C_L \Delta V_{logic} / \Delta T \]

We must ensure that this peak current is below Kirk-effect limits.

Second, on a falling pulse, the minimum EF current is zero:

\[ I_{ef,min} = 0 = I_{ef} - \Delta I = I_{ef} - C_L \Delta V_{logic} / \Delta T \]

From which

\[ \Delta T_{min} = C_L \Delta V_{logic} / I_{ef} \]

This is slew-rate-limited discharging of \( C_L \).
CML Propagation delay: two-level circuit
The logic voltage swing on the collector of Q2 is also approximately $\Delta V_{\text{logic}}$. Justification of this is a long and somewhat messy discussion. Note that on the B level switching path that Q1 is an EF, Q2 is CE, and Q3 is CB. If the base of Q3 is high and Q4 is low, then Q4 remains off and simply loads the collector of Q3 in $C_{je4}$.
Also simplify the answer for clarity by assuming that $\beta \gg 1$, & that the EF voltage gain is very close to 1. Note that Q3 operates in CB mode... please refer back to earlier notes to review $a_1$ terms for CB stages.
\[ 2T_{\text{gate}} \cong N \left( \frac{\Delta V_{\text{logic}}}{I_0} \right) C_{cb1} + R_{bb} C_{cb1} + C_{cb2} \left[ 2(R_{ex1} + 1/g_{m1}) + (\Delta V_{\text{logic}}/I_0) \right] \\
+ C_{cbi2} 2R_{bb2} + (C_{je2} + I_0 \tau_f/\Delta V_{\text{logic}}) (R_{bb2} + R_{ex1} + 1/g_{m1}) \\
+ \left[ C_{je3} + C_{je4} + (I_0 \tau_f/\Delta V_{\text{logic}}) \right] (\Delta V_{\text{logic}}/I_0) \\
+ (N + 1)(\Delta V_{\text{logic}}/I_0) C_{cb3} + R_{bb3} C_{cbi3} \]
ECL Propagation delay: two-level circuit
Logic Speed

<table>
<thead>
<tr>
<th></th>
<th>$c_{je}$</th>
<th>$c_{cbx}$</th>
<th>$c_{cbi}$</th>
<th>$\tau_f J / \Delta V_L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta V_L / J$</td>
<td>1</td>
<td>6</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>$kT / q J$</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>$\rho_e$</td>
<td>-0.25</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>$r_{bb}$</td>
<td>0.5</td>
<td>0</td>
<td>1</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Approximate delay coefficients $a_{ij}$ for an ECL master-slave flip-flop, found by hand analysis. Gate delay is of the form $T_{gate} = 1 / 2 f_{clock,max} = \Sigma a_{ij} r_i c_j$, where $f_{clock}$ is the maximum clock frequency. The minimum logic voltage swing is $\Delta V_{LOGIC} > 6(kT / q + J\rho_{ex})$.

Caveat: ignores interconnect capacitance and delay, which is very significant
Logic Speed: definition of terms

\[ c_{je} : \text{emitter base depletion capacitance per unit emitter area} \]
\[ c_{cbi} : \text{intrinsic collector base capacitance per unit emitter area} \]
\[ c_{cbx} : \text{extrinsic collector base capacitance per unit emitter area} \]
\[ \tau_f : \text{sum of base and collector transit times} \]
\[ J : \text{emitter current per unit emitter area} \]
\[ \Delta V_{LOGIC} : \text{logic voltage swing} \]
\[ r_{bb} : \text{base resistance times emitter area (e.g. "per - area" } R_{bb}) \]
\[ \rho_{ex} : \text{emitter resistance times emitter area (e.g. "per - area" } R_{ex}) \]
**What HBT parameters determine logic speed?**

<table>
<thead>
<tr>
<th></th>
<th>Cje</th>
<th>Ccbx</th>
<th>Ccbi</th>
<th>$(\tau_b + \tau_c) \ (I/\Delta V)$</th>
<th>total</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta V/I$</td>
<td>33.5%</td>
<td>6.7%</td>
<td>27.8%</td>
<td></td>
<td>68.4%</td>
</tr>
<tr>
<td>$\Delta V/I$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>12.3%</td>
</tr>
<tr>
<td>$(kT/q) I$</td>
<td>1.4%</td>
<td>0.1%</td>
<td>0.4%</td>
<td></td>
<td>0.5%</td>
</tr>
<tr>
<td>Rex</td>
<td>-1.3%</td>
<td>0.1%</td>
<td>0.3%</td>
<td></td>
<td>0.9%</td>
</tr>
<tr>
<td>Rbb</td>
<td>10.2%</td>
<td></td>
<td>2.8%</td>
<td></td>
<td>3.7%</td>
</tr>
<tr>
<td>total</td>
<td>43.8%</td>
<td>6.8%</td>
<td>31.3%</td>
<td></td>
<td>17.5%</td>
</tr>
</tbody>
</table>

38%

**Sorting Delays by capacitances:**

44% charging $C_{je}$, 38% charging $C_{cb}$, only 18% charging $C_{diff}$ (e.g. $\tau_b + \tau_c$)

**Sorting Delays by resistances and transit times:**

68% from $\Delta V_{logic} / I$, 12% from $(\tau_b + \tau_c)$, 17% from $R_{bb}$

$R_{ex}$ has very strong indirect effect, as $\Delta V_{logic} > 6 \cdot (kT/q + I_C R_{ex})$

**Caveats:**
assumes a specific UCSB InP HBT (0.7 um emitter, 1.2 um collector 2kÅ thick, 400 Å base, 1.5E5 A/cm$^2$)
ignores interconnect capacitance and delay, which is very significant