mm-Wave IC Design:
The Transition from III-V to CMOS Circuit Techniques

*Patrick Yue, Mark Rodwell, UCSB*
Outline

• Background
  – Emerging mm-wave applications
  – Open design issues for mm-Wave CMOS
• CMOS for mm-wave design
  – Optimizing CMOS device performance – layout & bias
  – On-chip inductors in CMOS
  – Cell-based device modeling and design methodology
  – State of the art CMOS mm-Wave design examples
• mm-Wave design techniques
  – Device characterization issues
  – Unconditionally stable, gain-matched amplifier design procedure
  – Tuned amplifier, power amplifier design examples
  – On-chip transmission line design
• Summary
• References
Emerging mm-Wave Wireless Applications

- Unlicensed 60-GHz band for Gbit wireless link:
  - Outdoor, point-to-point wireless link
  - Wireless High-Definition Multimedia Interface (HDMI)
- Licensed point-to-point wireless link in E-band (71-76, 81-86 GHz, and 92-95 GHz)
- Vehicular radar at 76-77 GHz
- 94-GHz band for high-resolution imaging

Questions:
Can we leverage scaled CMOS to produce more cost-effective products and enable new markets?
Recent Evolution for CMOS RF

- Lower power, cost and size
- 0.25-μm CMOS
- 5-GHz RF transceiver

But difficult to migrate below 0.18μm even for RF SoC...

(D. Su, et al. ISSCC 2002.)

(S. Mehta, et al. ISSCC 2005.)

- 0.18-μm CMOS
- RF + baseband DSP
State of the Art mm-Wave IC: 330 GHz 16-Finger Power Amp

designs in progress: Michael Jones

device: 5 V, 650 GHz $f_{\text{max}}$, InP DHBT

wiring: thin film microstrip with 2 um BCB

Challenges:

- Line losses are very high
- Lines $> 60 \, \Omega$ are not feasible $\rightarrow$ increases Q of output tuning
- Lines of required impedance are narrow $\rightarrow$ limits on DC current

Small unmodeled parasitics will de-tune design

....must maintain microstrip environment to device vias with negligible lengths of unmodeled random interconnects
Open Design Issues

• RF CMOS design are by and large lumped circuits
• mm-Wave design are traditionally distributed circuits
• How will mm-Wave CMOS be designed?
  – Assuming that we will integrate an entire transceiver, should each block be impedance-matched?
  – Do we need new design flow / methodology?
  – Should all interconnect be modeled as T-line and be impedance-controlled?
  – Do we need a well-controlled global ground (plane)?
• How to optimize CMOS device performance?
## CMOS Device Parameter Scaling Trend

<table>
<thead>
<tr>
<th>Process</th>
<th>0.25 μm ('98)</th>
<th>0.18 μm ('00)</th>
<th>0.13 μm ('02)</th>
<th>90 nm ('04)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$ (V)</td>
<td>2.5 (1x)</td>
<td>1.8 (0.7x)</td>
<td>1.2 (0.5x)</td>
<td>1.0 (0.4x)</td>
</tr>
<tr>
<td>$I_{dsat}$ (μA/μm)</td>
<td>600 (1x)</td>
<td>600 (1x)</td>
<td>550 (1x)</td>
<td>850 (1.4x)</td>
</tr>
<tr>
<td>$I_{off}$ (nA/μm)</td>
<td>0.01 (1x)</td>
<td>0.02 (2x)</td>
<td>0.32 (32x)</td>
<td>7 (700x)</td>
</tr>
<tr>
<td>$I_{gate}$ (nA/μm)</td>
<td>2.5e-5 (1x)</td>
<td>1.8e-3 (100x)</td>
<td>0.65 (5e4)</td>
<td>6.3 (70000x)</td>
</tr>
<tr>
<td>$I_{on}/I_{off}$ (10e6)</td>
<td>60 (1x)</td>
<td>30 (0.5x)</td>
<td>1.7 (0.03x)</td>
<td>0.12 (0.002x)</td>
</tr>
<tr>
<td>$g_m$ (mS/μm)</td>
<td>0.3 (1x)</td>
<td>0.4 (1.3x)</td>
<td>0.6 (2x)</td>
<td>1.0 (3.3x)</td>
</tr>
<tr>
<td>$g_{ds}$ (μS/μm)</td>
<td>7.7 (1x)</td>
<td>15 (2x)</td>
<td>42 (5.4x)</td>
<td>100 (13x)</td>
</tr>
<tr>
<td>$g_m / g_{ds}$</td>
<td>39 (1x)</td>
<td>27 (0.7x)</td>
<td>14 (0.36x)</td>
<td>10 (0.26x)</td>
</tr>
<tr>
<td>$f_T$ (GHz)</td>
<td>30 (1x)</td>
<td>60 (2x)</td>
<td>80 (2.7x)</td>
<td>140 (4.7x)</td>
</tr>
<tr>
<td>Delay (ps/gate)</td>
<td>45 (1x)</td>
<td>30 (0.7x)</td>
<td>15 (0.3x)</td>
<td>11 (0.24x)</td>
</tr>
<tr>
<td>$C_g$ (fF/gate)</td>
<td>0.47 (1x)</td>
<td>0.35 (0.7x)</td>
<td>0.25 (0.5x)</td>
<td>0.16 (0.34x)</td>
</tr>
<tr>
<td>$C_j$ (fF/gate)</td>
<td>0.83 (1x)</td>
<td>0.80 (1x)</td>
<td>0.88 (1.1x)</td>
<td>0.66 (0.8x)</td>
</tr>
</tbody>
</table>

- **Positive:** $f_T$, $f_{max}$, $F_{min}$, $I_{dsat}$, $g_m$, $C_g$ and $C_j$
- **Negative:** $V_{dd}$ and $g_{ds}$
Challenges for RF/mm-Wave in 0.13-\(\mu\)m CMOS and Beyond

- High mask cost ($0.5M – $1M)
  - only makes sense if integration level increases, e.g. RF + large DSP, or mm-wave transceiver
- Lack of a streamline RF/mm-wave design flow
- Negative impact of technology scaling
  - Device
    - Process variations
    - Model uncertainty
    - Interconnect parasitic variations
  - Circuit
    - Low voltage headroom due to reduced Vdd

⇒ Develop a parasitic-aware design methodology
⇒ Explore low-voltage circuit techniques
High Frequency Figures of Merit

- Minimize $R_g$, $R_s$, and $R_{sub}$ for better performance
- Layout and biasing are both critical

\[ f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \]

\[ f_{\text{max}} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s)} + 2\pi f_T R_g C_{gd}} \]

\[ NF_{\text{min}} = 1 + K \cdot \frac{f}{f_T} \cdot \sqrt{1 + g_m(R_g + R_s)} \]
Complete Macro Model

- Core model (baseline BSIM model)
- Interconnect RC (3D EM field solver)
- Gate and substrate resistances (physical model)
Gate Resistance Components

- $R_{geltd}$: distributed gate electrode resistance
- $R_{gch}$: channel induced gate resistance

Ref. 16

Jin, IEDM’98
Gate Electrode Resistance

\[ R_{geltd} = R_{eltd} \left( \alpha \frac{W}{L} + \beta \right) \]

\[ \alpha = \begin{cases} 
1/3 & \text{one side connected} \\
1/12 & \text{two sides connected} 
\end{cases} \]

- \( \alpha \) models distributed effect of gate electrode
- \( \beta \) models external gate resistance

Ref. 16 & 18
Channel Conductance

Two components in $G_{ch}$:

- **Static** channel conductance $\propto \frac{L}{W}$
  
  $$G_{st} = \frac{1}{\int dR} = \frac{I_d}{\int dV} = \begin{cases} I_d/V_{dsat} & \text{in saturation} \\ I_d/V_{ds} & \text{in triode} \end{cases}$$

- **Excess-diffusion** conductance
  
  $$G_{ed} = \eta \frac{kT}{q} \mu_{eff} C_{ox} \frac{W}{L}$$

\[ \eta \sim 1 \]

Ref. 16

(ac effect – channel charge distribution modulated by gate voltage, derived based on diffusion current)
Layout Guideline for Gate Resistance

- Multi-finger layout in RF MOSFET is common to minimize $R_{	ext{gate}}$ (at the expense of more parasitic capacitance)

- Typical finger width for 0.25um device is about 5 um whereas in 0.13um CMOS is 1.5 um

- Total gate width ranges from a few 10’s of micron for LNA, mixer & VCO to a few millimeters for PA

- $R_{\text{eltd}}$ (poly resistance) scales with $1/n^2$

- External portion of $R_{\text{geltd}}$ (contact resistance) scale with $1/n$

- $R_{\text{ch}}$ is independent of $n$ to the first order
Substrate Resistance Model

- Active and STI regions have different sheet resistances
- Resistances in x and y directions modeled as parallel resistors

(R. Chang, et al. TED 2004.)
Analytical Model of Substrate Resistance

\[ R_{STI,x} = \frac{1}{2} R_{sh,STI} \frac{x_{STI}}{y_{act}} \]

\[ R_{active,x} = \frac{1}{12} R_{sh,act} \frac{x_{act}}{y_{act}} \]

Ref. 17
Optimization of Substrate Resistance

![Graph showing the relationship between substrate resistance ($R_{\text{sub}}$), number of fingers, and aspect ratio of device active area.

Ref. 17
Interconnect RC Modeling Using 3D Field Solver

Top view

Bottom view showing substrate taps

<table>
<thead>
<tr>
<th>Width (μm)</th>
<th>nf</th>
<th>$C_{gs_wire}$ (fF)</th>
<th>$C_{gd_wire}$ (fF)</th>
<th>$C_{ds_wire}$ (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0</td>
<td>4</td>
<td>2.42</td>
<td>1.61</td>
<td>1.41</td>
</tr>
</tbody>
</table>

- Wire capacitance per finger is extracted
RF Macro Model vs. Measurement (16 x 2µm/0.12 µm)

\[ R_g = 9.8 \, \Omega, \, R_{\text{sub}} = 475 \, \Omega, \, C_{\text{gs_ext}} = 4 \, \text{fF}, \, C_{\text{gd_ext}} = 2.9 \, \text{fF}, \, C_{\text{ds_ext}} = 5.2 \, \text{fF} \]
Optimized Layout for $f_T$, $f_{\text{max}}$ and NF

- Parallel $R_g$ improves $f_{\text{max}}$ and $NF_{\text{min}}$
- Gate connected at both ends
- Source drain metals do not overlap
- Bulk contacts surround device
Optimal Finger Width for f\(T\)

- \(f_T\) approaches \(v_{sat} / L\) deep in velocity saturation

![Graph showing the relationship between gate length and \(f_T\)](image)

![Graph showing the relationship between finger width and \(f_T\)](image)
Optimal Finger Width for $f_{\text{max}}$

- Reducing $R_g$ vs. increasing $C_{gg}$
- For 0.13-$\mu$m, optimal finger width is ~2 $\mu$m
- Optimal finger width decreases with device scaling
Noise due to $R_g$ and $R_{sub}$ can be minimized through layout optimization

Ref. 11
Optimal Biasing for $f_T$, $f_{\text{MAX}}$ and $\text{NF}_{\text{MIN}}$

- Peak $f_T$, $f_{\text{MAX}}$ and $\text{NF}_{\text{MIN}}$ characteristic current densities largely unchanged across technology nodes and foundries
- $\text{NF}_{\text{MIN}}$ (0.15mA/µm) and peak $f_{\text{MAX}}$ (0.2mA/µm) are close → LNAs simultaneously optimized for noise and high gain
- In CMOS PAs optimum current swing when biased at 0.3mA/µm

Source: Yao, RFIC 2006. - U. of Toronto
Frequency Response of On-Chip Inductor Q

\[ \frac{\omega L_s}{R_s} \]

- Copper
- Aluminum
- Model

\( Q \) vs. Frequency (GHz)
First Patterned Ground Shield (PGS)

- Inserted between the inductor and substrate
- PGS fingers connected in a “star” shape
- Terminates the E field
- No effect on the H field
- Improves isolation

Silicided polysilicon

Induced eddy current
Self-Shielded Stacked Inductors for high SRF

- Self-shielded layout can effectively boost-strap the overlap capacitance.
- 1-nH inductor can be achieved in 25x25 μm² using M5 through M8 in a 0.13-μm CMOS 8-metal process.

* C.-C. Tang, JSSC, April 2002.
Systematic mm-wave Design with P-Cells

- Stand-alone single device model is insufficient
- Interconnect model accuracy limited by digital RC extraction
- Test structure layout ≠ actual circuit layout

- Leverage the insight to device layout optimization
- Exploit the modularity at the sub-circuit level
Sample P-Cell Layouts and Circuit Models

**Diff Pair**

![Diff Pair Circuit Diagram](image1)

**Cross-Coupled Pair**

![Cross-Coupled Pair Circuit Diagram](image2)

**Cascode**

![Cascode Circuit Diagram](image3)
Sub-Circuit Cell Library for mm-wave Design

- A unified design and modeling framework
- Each sub-circuit P-Cell has its scalable circuit model
mm-wave P-Cell Characterization Test Structures

- Measured S-parameters to validate macro models
- UMC 0.13-μm CMOS with 8 copper layers
Outline

• Background
  – Emerging mm-wave applications
  – Open design issues for mm-Wave CMOS

• CMOS for mm-wave design
  – Optimizing CMOS device performance – layout & bias
  – On-chip inductors in CMOS
  – Cell-based device modeling and design methodology
  – State of the art CMOS mm-Wave design examples

• mm-Wave design techniques
  – Device characterization issues
  – Unconditionally stable, gain-matched amplifier design procedure
  – Tuned amplifier, power amplifier design examples
  – On-chip transmission line design

• Summary

• References
140-220 & 220-330 GHz On-Wafer Network Analysis

• HP8510C VNA,
  *Oleson Microwave Lab* mm-wave Extenders

• coplanar wafer probes made by:
  GGB Industries, Cascade Microtech

• connection via short length of waveguide

• Internal bias Tee’s in probes for biasing active devices

• measurements to 100 GHz can be in coax.
Measuring wideband transistors is very hard! Much harder than measuring amplifiers. Determining f\text{max} in particular is extremely difficult on high-f\text{max} or small devices.

Standard "short pads"
- must strip pad capacitance
- must strip pad inductance--or ft will be too high!
- cal can be bad due to substrate coupling
  - make pads small, and shield them from substrate
- cal can be bad due to probe coupling
  - use small probe pitch, use well-shielded probes
**High Frequency Measurements: On-Wafer LRL**

**Extended Reference planes**
- Transistors placed at center of long on-wafer line
- LRL standards placed on wafer
- Large probe separation → probe coupling reduced
- Still should use the best-shielded probes available

**Problem: substrate mode coupling**
- Method will fail if lines couple to substrate modes
- Method works very poorly with CPW lines
- Need on wafer thin-film microstrip lines

Note that calibration is to line $Z_0$. Line $Z_0$ is complex at lower frequencies, and must be determined.
Unilateral Power Gain

1) Cancel device feedback with external lossless feedback
   \[ Y_{12} = S_{12} = 0 \]
2) Match input and output

Resulting power gain is Mason's Unilateral Gain

\[ U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})} \]

Monolithic amplifiers are not easily made unilateral
   \[ \rightarrow U \ \text{mostly of historical relevance to IC design} \]

For simple BJT model, U rolls off at \(-20 \text{ dB/decade}\)
   \[ \rightarrow U \ \text{useful for extrapolation to find} \ f_{\text{max}} \]

In III-V FETs, U shows peak from \( C_{ds} - R_s - R_d \) interaction
   \[ \rightarrow U \ \text{hard to use for} \ f_{\text{max}} \ \text{extrapolation} \]

For bulk CMOS, \( C_{ds} \) is shielded by substrate
   \[ \rightarrow U \ \text{should be OK for} \ f_{\text{max}} \ \text{extrapolation} \]
Design Tools: Power Gain Definitions

**Transducer Gain**

\[ G_T = \frac{P_{load}}{P_{av,gen}} \]

- Load power
- Power available from generator
- General-case gain

\[ Z_L = Z_{out}* \]

**Available Gain**

\[ G_A = \frac{P_{av,a}}{P_{av,gen}} \]

- Power available from amplifier
- Power available from generator
- Gain with output matched

\[ Z_s = Z_o \]

**Insertion Gain**

\[ \|S_{21}\|^2 = \frac{P_{av,a}}{P_{av,gen}} \]

- Power delivered to \( Z_o \) load
- Power available from \( Z_o \) generator
- Gain in a 50 Ohm environment

\[ Z_L = Z_o \]

**Operating Gain**

\[ G_P = \frac{P_{load}}{P_{gen,delivered}} \]

- Load power
- Power delivered from generator
- Gain with input matched

**Maximum Available Gain**

\[ G_{Max} = \frac{P_{av,a}}{P_{gen,delivered}} \]

- Power available from amplifier
- Power delivered from generator
- Gain with both ports matched
- MAG may not exist...

\[ Z_s = Z_{in}* \]

**After impedance-matching:**

\[ \|S_{21,matched}\|^2 = G_{max,raw} \]

\[ S_{11,matched} = S_{22,matched} = 0 \]

...but only if unconditionally stable...
Design Tools: Stability Factors, Stability Circles

\[ \Gamma_{in} = S_{11} + \Gamma_L \frac{S_{12}S_{21}}{1 - S_{22}\Gamma_L} \]

Load Stability Circle

\[ \Gamma_{out} = S_{22} + \Gamma_S \frac{S_{12}S_{21}}{1 - S_{11}\Gamma_S} \]

Source Stability Circle

Values of \( \Gamma_L \) which make \( \| \Gamma_{in} \| = 1 \rightarrow \) beyond lies negative \( R_{in} \)

Values of \( \Gamma_S \) which make \( \| \Gamma_{out} \| = 1 \rightarrow \) beyond lies negative \( R_{out} \)

Unconditionally stable (stable with all \( (\Gamma_L, \Gamma_S) \)) if:

\[ K = \text{Rollet stability factor} \]

\[ = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + \det^2[S]}{2|S_{21}S_{12}|} > 1 \]

and \( B = \text{stability measure} \)

\[ = 1 - |S_{11}|^2 - |S_{22}|^2 - \det^2[S] > 0 \]

Negative port impedance \( \rightarrow \) negative-\( R \) oscillator
Tuning for highest gain \( \rightarrow \) infinite gain (oscillation)
Design Tools: Maximum Stable Gain

Maximum stable gain = MSG

\[
\frac{|S_{21}|}{|S_{12}|} = \frac{|Y_{21}|}{|Y_{12}|} = \frac{|Z_{21}|}{|Z_{12}|}
\]

Adding series/shunt resistance excludes source or load from unstable regions → stabilizes
Design Procedure: Simple Gain-Matched Amplifier

First: stabilize at the design frequency

--- device is potentially unstable at 100 GHz design frequency

source stability circle: ~5 Ohm on input will overstabilize the device

After stabilizing (slightly over-stabilizing)
Design Procedure: Simple Gain-Matched Amplifier

**Second:**
Determine required interface impedances

The Ga & Gp circles define the source & load impedances which the transistor must see

...it is necessary to OVERSTABILIZE the device to move the Ga & Gp circles towards the Smith chart center

**Third:**
Design Input & Output Tuning Networks
...to provide these impedances...

...added to device, the amplifier is not yet complete...
**Design Procedure: Simple Gain-Matched Amplifier**

**Forth:**
Add out-of-band stabilization potentially unstable below 75 GHz

...caused only slight mistuning & slight gain drop @ 100 GHz

...and is unconditionally stable above 10 GHz
Finally:
adjusting for line losses

high line skin effect losses → reduced gain

but line losses also increase stability factor

loss in gain are partly recovered by reducing stabilization resistance & re-tuning the design

--no analytical procedure; just component tweaking

line losses have severe impact...in VLSI wiring environment...particularly at 50 + GHz...particularly with high-power amplifiers
Tuned Amplifier Examples

3-stage cascode in 180 nm CMOS

III-V HBT small-signal amplifiers

Note: simple gain-tuned amplifiers → limited applications
Transmitters need power amplifiers: need output loadline-match, not gain-match
Receivers need low-noise amplifiers: need input noise-match, not gain-match
For maximum saturated output power, & maximum efficiency, device intrinsic output must see optimum loadline set by:

- breakdown
- maximum current
- maximum power density.

\[ P_{\text{max}} = \frac{1}{8}(V_{\text{max}} - V_{\text{min}})I_{\text{max}} \]

parasitic C's and R's represented by external elements... ammeter monitors intrinsic junction current without including capacitive currents

\[ (V_{\text{collector}} - V_{\text{emitter}}) \]

measures voltage internal to series parasitic resistances...
Power Amplifier Design (Cripps Method)

Design steps are
1) input stabilization (in-band)
2) output tuning for correct load-line
3) input tuning (match)
4) out-of-band stabilization

Example: 60 GHz, 30 mW PA, 130 nm BiCMOS
Design: Multi-Finger Power Amplifiers: Even-mode method

-- Most multi-finger amplifiers do not use Wilkinson combiners: lines are too long
Even-mode equivalent circuit maps combined design into single-device design
Final design tuning (E&M simulation) with full circuit model

This method explicitly models all feed parasitics in a large multi-finger transistor
MUCH more reliable than using single lumped model for multi-finger device
If each transistor finger is individually stabilized, high-order modes are stable.
Amplifier layout usually does not allow sufficient space for this.
All spatial modes must then be stabilized.

Stabilization method: bridging resistors → parallel loading to higher-order modes
Select so that \((Z_S, Z_L)\) presented to device lie in the stable regions

etc...
Design: Multi-Finger Amplifiers: Layout Examples

W-band InP HBT power amplifier - UCSB

mm-wave InP HBT power amplifier - Rockwell

mm-wave InP HBT power amplifier - Rockwell
Low-Noise Amplifier Design-- device model

Basic model: Van der Ziel

\[ S_{VV,R_g} = 4kT R_g \ (V^2 / Hz) \]
\[ S_{VV,R_i} = 4kT R_i \ (V^2 / Hz) \]
\[ S_{VV,R_s} = 4kT R_s \ (V^2 / Hz) \]
\[ S_{II,channel} = 4kT \Gamma g_m \ (A^2 / Hz) \]

\[ \Gamma = \begin{cases} 
2/3: \text{long channel, constant mobility} \\
> 2/3 \text{ under high field} 
\end{cases} \]

Cross spectral densities can be neglected

(B. Hughes, IEEE Trans MTT)

Simplified noise model

\[ S_{VV,R_{in}} = 4kT R_{in} \ (V^2 / Hz) \]
\[ S_{II,channel} = 4kT \Gamma'' g_m \]

\[ \Gamma' \rightarrow \Gamma \text{ as } g_m R_s \rightarrow 0 \]
\[ \Gamma'' \rightarrow 1 \text{ as } g_m R_s \rightarrow \infty \]
Low-Noise Amplifier Design—sketch of steps in $F_{\text{min}}$ calculation

Total input noise voltage & current spectral densities:

\[ S_{E_a}(f) = 4kTR_m + \frac{4kT}{g_m} \left( 1 + \left( 2\pi f C_{gs} \right)^2 R_{in}^2 \right) \left( V^2 / \text{Hz} \right) \]

\[ S_{I_a}(f) = \frac{4kT}{g_m} \left( 2\pi f C_{gs} \right)^2 \left( A^2 / \text{Hz} \right) \]

\[ S_{E_{aI_a}}(f) = \frac{4kT}{g_m} \left( 1 + j2\pi f C_{gs} R_m \right) \left( V \times A / \text{Hz} \right) \]

Noise figure with a particular source impedance:

\[ F = 1 + \frac{S_{E_a} + |Z_s|^2 S_{I_a} + 2 \cdot \text{Re}(Z_s^* S_{E_{aI_a}})}{4kT \cdot \text{Re}(Z_s)} \]

Minimum noise figure

\[ F_{\text{min}} = 1 + \frac{1}{4kT} \left[ 2 \sqrt{S_{E_a} S_{I_a} - \left( \text{Im}[S_{E_{aI_a}}] \right)^2} + 2 \text{Re}[S_{E_{aI_a}}] \right] \]

\[ Z_{\text{opt}} = R_{\text{opt}} + jX_{\text{opt}} = \sqrt{\frac{S_{E_a}}{S_{I_a}}} \left( \frac{\text{Im}[S_{E_{aI_a}}]}{S_{I_a}} \right) - j \frac{\text{Im}[S_{E_{aI_a}}]}{S_{I_a}} \]

→ Fukui Expression (rough)

\[ F_{\text{min}} \approx 1 + 2 \sqrt{\Gamma (R_s + R_g + R_f) g_m} \cdot \left( \frac{f_{\text{signal}}}{f_r} \right) \]

\[ Z_{\text{opt}} \approx \sqrt{\frac{R_s + R_g + R_f}{\Gamma g_m}} \cdot \left( \frac{f_r}{f_{\text{signal}}} \right) + \frac{1}{j2\pi f_{\text{signal}} C_{gs}} \]
Low-Noise Amplifier Design

Design steps are
1) output stabilization (in-band)
2) input tuning for $F_{\text{min}}$
3) output tuning (match)
4) out-of-band stabilization

Discrepancy in input noise-match & gain-match can be reduced by adding source inductance (R. Van Tuyl)

Example: 60 GHz, LNA, 130 nm BiCMOS
III-V MIMIC Interconnects -- Classic Substrate Microstrip

Thick Substrate → low skin loss

Zero ground inductance in package

No ground plane breaks in IC

High via inductance

TM substrate mode coupling

12 pH for 100 μm substrate → 7.5 Ω @ 100 GHz

Strong coupling when substrate approaches ~λ/4 thickness

lines must be widely spaced

ground vias must be widely spaced

all factors require very thin substrates for >100 GHz ICs → lapping to ~50 μm substrate thickness typical for 100+ GHz

12 pH for 100 μm substrate → 7.5 Ω @ 100 GHz
Coplanar Waveguide

No ground vias
No need to thin substrate

Hard to ground IC to package

Parasitic microstrip mode

Parasitic slot mode

ground plane breaks → loss of ground integrity

substrate mode coupling or substrate losses

Repairing ground plane with ground straps is effective only in simple ICs
In more complex CPW ICs, ground plane rapidly vanishes → common-lead inductance → strong circuit-circuit coupling

40 Gb/s differential TWA modulator driver note CPW lines, fragmented ground plane
35 GHz master-slave latch in CPW note fragmented ground plane
175 GHz tuned amplifier in CPW note fragmented ground plane

poor ground integrity
loss of impedance control
ground bounce
coupling, EMI, oscillation
III-V MIMIC Interconnects -- Thin-Film Microstrip

- **narrow line spacing → IC density**
- **no substrate radiation, no substrate losses**
- **fewer breaks in ground plane than CPW**
- **... but ground breaks at device placements**
- **still have problem with package grounding**
- **...need to flip-chip bond**

\[ Z_o \sim \frac{\eta_0}{\varepsilon_r^{1/2}} \left( \frac{H}{W + H} \right) \]

- **thin dielectrics → narrow lines**
  - **high line losses**
  - **low current capability**
  - **no high-\(Z_o\) lines**
III-V MIMIC Interconnects -- Inverted Thin-Film Microstrip

- **narrow line spacing → IC density** ☀

- **Some substrate radiation / substrate losses** ☹

- **No breaks in ground plane** ☀

- **...no ground breaks at device placements** ☀

- **still have problem with package grounding** ☹

  ...need to flip-chip bond

- **thin dielectrics → narrow lines** ☹
  → **high line losses**
  → **low current capability**
  → **no high-Z₀ lines**

---

*Image 1: Inverted microstrip line*

*Image 2: S.I. Substrate*

*Image 3: InP 150 GHz master-slave latch*

*Image 4: InP 8 GHz clock rate delta-sigma ADC*
If It Has Breaks, It Is Not A Ground Plane!

coupling / EMI due to poor ground system integrity is common in high-frequency systems whether on PC boards ...or on ICs.
No clean ground return? → interconnects can't be modeled!

35 GHz static divider
interconnects have no clear local ground return
interconnect inductance is non-local
interconnect inductance has no compact model

8 GHz clock-rate delta-sigma ADC
thin-film microstrip wiring
every interconnect can be modeled as microstrip
some interconnects are terminated in their Zo
some interconnects are not terminated
...but ALL are precisely modeled

InP 8 GHz clock rate delta-sigma ADC
VLSI mm-Wave Interconnects with Ground Integrity

- Narrow line spacing → IC density
- No substrate radiation, no substrate losses
- Negligible breaks in ground plane
- Negligible ground breaks @ device placement
- Still have problem with package grounding
  ...need to flip-chip bond

- Thin dielectrics → narrow lines → high line losses → low current capability → no high-Z₀ lines
Example: 150 GHz Master-Slave Latch

Device Technology:
500 nm InP HBT

Interconnects:
inverted thin-film microstrip

Design:
All lines modeled as microstrip lines
representative lines simulated in Agilent / Momentum
fit to simple lossy line model (loss, Zo, velocity)

Minimum input power (dBm)

frequency (GHz)
Example: 20 GHz DDFS Design (Rockwell)

designs in progress: MJ Choe

design target: 
20 GHz clock rate

circuit topology: 
ECL

device technology: 
350 GHz (500 nm) InP HBT (Rockwell)

Interconnect technology: 
inverted thin-film microstrip throughout → all lines are controlled-impedance

shorter lines: 
unterminated, but modeled

longer lines: 
modeled and terminated
Summary

- At 90-nm or below, CMOS can be a cost-effective choice for highly integrated mm-wave circuits
- Consideration for optimizing device layout and biasing are very similar for mm-wave and RF
- Pre-characterized cell-based mm-wave design flow will be a key enabler
References on other mm-Wave CMOS Efforts


- Prof. F. Chang – “A 60GHz CMOS VCO using on-chip resonator with embedded artificial dielectric for size, loss, and noise reduction,” *2006 ISSCC*.

In case of questions