High-Current InP-Based Triple Heterojunction Tunnel Transistors

Pengyu Long1, Jun Z. Huang1, Michael Povolotskyi1, Devin Verreck1,3, Gerhard Klimeck1, Mark. J.W. Rodwell2

1Network for computational nanotechnology, Purdue University, West Lafayette, IN 47906

2ECE Department, University of California, Santa Barbara, CA 93106-95603

3Department of Electrical Engineering, imec, KU Leuven, 3001 Leuven, Belgium Email: davidlong180@gmail.com

*Abstract*— We report the design and simulated performance of a GaAsSb/GaSb/InAs/InP n-type triple heterojunction (3-HJ) tunnel field-effect transistor (TFET). GaAsSb/GaSb source and InAs/InP channel HJs both increase the field imposed upon the tunnel junctions and introduce two resonant bound states. The tunneling probability, and hence the transistor on-current, are thereby greatly increased. The devices were simulated using a non-equilibrium Green function quantum transport approach and the k.p method within NEMO5. With 10-3 A/m (*I*OFF) and a 0.3 V power supply *V*DD, we simulate 380 A/m ON-current (*I*ON) at 30-nm gate length (*L*g) and 275 A/m at 15-nm *L*g. Unlike a previously-reported high-current AlGaSb/GaSb/InAs/InGaAsSb 3-HJ design, the GaAsSb/GaSb/InAs/InP design employs channel materials to which high-quality, low-interface-state-density gate dielectrics have been demonstrated. *Keywords*—Tunnel FET, Tunnel transistors.

Future VLSI devices will require low *CVDD*2/2 switching energy, large on-currents (*I*ON), and small off-currents (*I*OFF). Low switching energy requires a low supply voltage *VDD*, yet reducing *VDD* typically increases *I*OFF and reduces the *I*ON*/I*OFF ratio. Though tunnel FETs (TFETs) have steep subthreshold swings and can operate at a low *VDD*, their *ION* is limited by low tunnel probability. This low *I*ON will result in large *CV*DD*/I* delay and slow operation.

To obtain high on-currents, we had previously proposed [1] an AlGaSb/GaSb/InAs/InAlAsSb triple-heterojunction (3HJ) tunnel FET, the design using materials lattice-matched to InAs. In this device, (10) confinement reduces both the hole tunnel effective mass and the tunnel barrier energy at the GaSb/InAs interface, both increasing the tunnel probability. The tunnel probability was further increased by source [2] and channel heterojunctions. The heterojunctions increase the junction built-in potential and field, hence reduce the tunnel distance. Further, the heterojunctions introduce two resonant states; in combination with the reduced tunnel distance, the tunnel probability increased from ~3% for a reference GaSb/InAs TFET design to > 50% over the conduction window between the source Fermi level and the conduction-band edge. *I*on is thereby greatly increased, by 26:1, from 30A/m for the reference GaSb/InAs design, to 750 A/m for the AlGaSb/GaSb/InAs/InAlAsSb design, given 30nm *L*g, 10-3 A/m *I*off , and 0.3V *V*DD. Despite the high simulated *I*ON, the materials selection is problematic; critically, no low-interface-trap density gate dielectrics have been demonstrated for InAlAsSb. In contrast, very low-interface-trap density gate dielectrics have been demonstrated for InAs, InGaAs, and InP [3,4,5]. Here we report high-current 3-HJ TFET design using InAs/InP channel materials. Except for a thin strained GaSb/InAs tunnel junction, the materials are lattice-matched to InP, and the channel materials are compatible with established high-quality dielectrics.

The use of InP channel materials forces the GaSb/InAs tunnel junction layers to be strained; first we consider design of this junction. In the  orientation, at 3nm body thickness (*T*b), a GaSb/InAs junction, if unstrained, has a low 0.078 eV barrier energy, but a high off-state tunneling probability (fig 1) because of the low InAs conduction-band mass (m\*) and low InAs bandgap (Eg). If GaSb/InAs are grown lattice-matched to InP, the compressive biaxial strain will increase m\* and *E*g, therefore reducing *I*OFF, but tunnel barrier height will also increase, therefore reducing the tunnel probability and *I*ON compared to unstrained InAs/GaSb TFET (Fig. 2).

The triple HJ TFET decreases the tunnel distance and adds two resonant states, both increasing *I*ON. The high m\* and *E*g of InP channel also reduces *I*OFF. A graded source HJ further decreases the tunnel distance; its design includes a GaAs0.56Sb0.44 source (*N*A=*2×1019*cm-3), an 1.5 nm GaAs0.38Sb0.62 (*N*A=*5×1019*cm-3) grade layer, a 3 nm GaSb (*N*A=*5×1019*cm-3) P-layer, a 3 nm InAs undoped N-layer, and an undoped InP channel. The TFETs have double gates (e.g. are finFETs) with 2.56nm thick gate dielectric (*εr,ox=*9), and 3nm thick channels. Resonant states are located in the source GaSb well and channel InAs well (Fig. 4b). Fig. 5a) compares the band diagram of a triple HJ TFET with a strained GaSb/InAs TFET in the on-state. The depletion region is reduced from both source and channel side, so tunnel distance reduced from 3.9nm to 1.4nm at 30nm Lg, and from 5.2nm to 2.5nm at 15nm Lg.

The devices are studied using NEMO5 [6] with quantum transmitting boundary method [7], using eight-band k.p method with strain [8, 9]. The device shows 12mV/dec. S.S. and380A/m ballistic *I*ON at 30nm *L*G, and shows 30mV/dec S.S, and 275A/m *I*on at 15 nm *L*G (Fig. 6). Phonon-assisted tunneling will increase *I*OFF, an effect not modeled here, but modeled in [2]. Note that if the on-current is adequate, even a 53mV/dec TFET will save 50% in energy compared to a MOSFET [10]. A detailed analysis of *I*OFF will follow.

[1] P. Long, *et al.*, 2016 DRC [2] M. G. Pala, *et al.*, IEEE J. EDS, vol.3, no.3 (2015) [3] S Lee *et al.*, 2014 VLSI Symp. [4] C. Y. Huang *et al.*, 2014 Lester Eastman Conf. [5] C. Y. Huang *et al.*, IEDM (2015) [6] J.E. Fonseca, *et al.*, J. Comput. Electron, vol.12, no.4, [7] M. Luisier, *et al.* Phys. Rev. B, vol. 74, no. 20 (2006), [8] T. B. Bahder, Phys. Rev. B, vol. 41, no. 17, (1990). [9] I. Vurgaftman, et al, J. Appl. Phys. vol. 89, no. 11, 2001. [10] I. A. Young, et al, IEDM (2015).

Acknowledgements: The nanoHUB.org computational resources are funded by the US NSF grant Nos. EEC-0228390, EEC-1227110, EEC-0634750, OCI-0438246, OCI-0832623 and OCI-0721680. This work is supported by the NSF Grant No. 1509394. NEMO5 developments are supported by OCI-0749140 and by Intel Corp. D.Verreck gratefully acknowledges support from IWT-Vlaanderen and FWO-Vlaanderen

|  |  |
| --- | --- |
| C:\Temp\Dropbox\IPRM\2016\figures\EcToff.eps | C:\Temp\Dropbox\IPRM\2016\figures\Fig2EcT.eps |
| **Fig. 1.** Band diagram (a) and transmission probability (b) of a 3nm thick -confined GaSb/InAs UTB tunnel FET in OFF-state bias with *L*g=15nm. The transport is along [110]. | **Fig. 2.** Band diagram (a) and transmission probability (b) of a unstrained GaSb/InAs TFET and one biaxially strained to InP at *L*g=15nm*.* |
| C:\Temp\Dropbox\IPRM\2016\figures\Fig2short.eps  **Fig. 3.** Device cross-section of a TFET with a GaSb/InAs tunnel heterojunction (a), a InAs/InP channel heterojunction (b), (c) with both source (GaAsSb/GaSb) and channel heterojunctions In (d), the source heterojunction can be graded. | |
| **C:\Temp\Dropbox\IPRM\2016\figures\dosJ.png** | **C:\Temp\Dropbox\IPRM\2016\figures\EcTon2.eps** |
| **Fig. 4.** a) Energy resolved current density b) Local density of states in on-state bias of a (10)-confined triple-HJ TFET. Resonant states are circled. | **Fig. 5.** Band diagram (a) and transmission probability (b) of a ()-confined GaSb/InAs TFET and a triple-HJ TFET with source grading. |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | |  | LG=30nm | | LG=15nm | | | Tunnel  barrier (nm) | ION  (A/m) | Tunnel barrier (nm) | ION  (A/m) | | Unstrained GaSb/InAs | 0.9 | 240 | 1.6 | -- | | Strained GaSb/InAs | 3.9 | 25 | 5.2 | 8 | | channel HJ | 2.5 | 165 | 2.6 | 120 | | Triple HJ | 1.4 | 380 | 1.5 | 275 |   **Table 1:** *I*ON and tunneling distance for (10) GaSb/InAs HJ, channel HJ, and triple-HJ TFETs. | **C:\Temp\Dropbox\IPRM\2016\figures\IVcompare.eps**  **Fig. 6.** Transfer characteristics of () confined TFETs for *L*G=30nm (a) and *L*G=15nm (b). |