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High-efficiency Millimeter-wave Power Amplifiers and Packaging Design

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in
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by

Ahmed Samir Hamed Sayed Ahmed

Committee in charge:

Professor Mark Rodwell, Chair
Professor James Buckwalter
Professor Ali Niknejad, University of California, Berkeley
Professor Loai Salem
Dr. Miguel Urteaga, Teledyne Scientific and Imaging

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The Dissertation of Ahmed Samir Hamed Sayed Ahmed is approved.

Professor James Buckwalter

Professor Ali Niknejad, University of California, Berkeley

Professor Loai Salem

Dr. Miguel Urteaga, Teledyne Scientific and Imaging

Professor Mark Rodwell, Committee Chair

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Curriculum Vitæ
Ahmed Samir Hamed Sayed Ahmed

Education

2020	Ph.D. in Electrical and Computer Engineering (Expected), University of California, Santa Barbara.
2015	M.Sc in Electronics and Electrical Communications Engineering, Cairo University, Cairo, Egypt.
2012	B.S. in Electronics and Electrical Communications Engineering, Cairo University, Cairo, Egypt.

Professional Experience

9/2015 -2020	Research Assistant at the High-Frequency Electronics Group at University of California, Santa Barbara, USA.
6/2019 -12/2019	Summer Internship at Samsung Research America, Dallas, Texas, USA.
6/2017 - 10/2017	Summer Internship at Skyworks, Newbury Park, Ventura, USA.
9/2015 -2020	Research and Teaching Assistant at Cairo University, Cairo, Egypt.

Publications

1. **A. S. H. Ahmed**, Munkyo Seo, A. A. Farid, M. Urteaga and M. J. W. Rodwell, "**A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology**,"2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 492-495.
2. **A. S. H. Ahmed**, Munkyo Seo, A. A. Farid, M. Urteaga and M. J. W. Rodwell, "**A 200mW D-band Power Amplifier with 17.8% PAE in 250-nm InP HBT Technology**,"accepted to 2020 15th (EuMIC), Utrecht, 2020
3. **A. S. H. Ahmed**, A. Simsek, A. A. Farid, A. D. Carter, M. Urteaga and M. J. W. Rodwell, "**A W-Band transmitter channel with 16dBm output power and a receiver channel with 58.6mW DC power consumption using heterogeneously integrated InP HBT and Si CMOS technologies"**," 2019 (IMS), Boston, MA, USA, 2019.
4. **A. S. H. Ahmed**, A. A. Farid, M. Urteaga and M. J. W. Rodwell, "**204GHz Stacked-Power Amplifiers Designed by a Novel Two-Port Technique**," 2018 13th European Microwave Integrated Circuits Conference (EuMIC), Madrid, 2018, pp. 29-32.

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9. A. Simsek, **A. S. H. Ahmed**, A. A. Farid, U. Soylu and M. J. W. Rodwell, "A 140GHz Two-Channel CMOS Transmitter Using Low-Cost Packaging Technologies," 2020 IEEE Wireless Communications and Networking Conference Workshops (WCNCW), Seoul, Korea (South), 2020, pp. 1-3,

Abstract

High-efficiency Millimeter-wave Power Amplifiers and Packaging Design

by

Ahmed Samir Hamed Sayed Ahmed

There is an increasing demand for high data rate communications. The available spectrum is nearly full, and industry considered 5G systems. In this research, we considered the next-generation systems (100-340GHz). Millimeter frequencies permit much larger spectrum and shorter wavelengths provides massive MIMO array and high image resolution. The thesis focuses on building the hardware and necessary components for such systems. There are lots of challenges in building the hardware; path loss and weather attenuation are high which demands high output power with high efficiency. Additionally, mm-wave packaging is very challenging. Here, we introduce a network theory to analyze the amplifiers degrees of freedom and design for maximum PAE. The proposed theory considers the stacking and parallel power combing approaches using network theory techniques. From the theory, we can design using arbitrarily complex transistor models, and lossy interconnect for maximum PAE. The theory establishes a design framework for high efficiency power amplifier design.

We demonstrate high efficiency mm-wave power amplifiers (140, 210, and 300GHz) with moderate output powers. The 140GHz amplifiers produce measured output power (20.5-23dBm) with record efficiency of 17.8-20.8%PAE. We are also presenting 17.7-18.5dBm output power over 190-210GHz frequency range with high efficiency of 6.9-8.5% PAE. We simulated 17dBm saturated power at 300GHz. The design key features are: 1) Low loss

combiner: we proposed transmission line network combiner which is more compact and less lossy compared to Wilkinson. 2) careful selection for the power cell. We have done a comparative study between different topologies and found that common base showed superior performance, compared to common emitter, at the frequency of interest and Teledyne technologies. 3) driver design: We optimized the driver size and topology to achieve high PAE.

The last part of the thesis is massive MIMO demonstration and mm-wave packaging. We started with a CMOS transmitter and receiver with advanced copper pillar. We also have bare InP power amplifiers. We present all the design procedures and challenges moving from the wafer level to the packaging and complete system. We demonstrate a single CMOS channel transmitter and receiver with eight element series fed patch antenna showing EIRP of 13dBm at 135 GHz. We also built a tile with eight elements transmitter or receiver which is currently in fabrication. High efficiency with 100mW InP amplifier is integrated with the CMOS transmitter to increase the system EIRP and cover long ranges

Contents

Curriculum Vitae **vi**

Abstract **viii**

List of Figures **xiv**

List of Tables **xxi**

1 Introduction **1**
1.1 Millimeter Wave for Next Communication Generation 1
1.2 Dissertation Contributions and Organization 2
1.3 Permissions and Attributions 5

2 Millimeter-Wave Power Amplifier Fundamentals **7**
2.1 Introduction 7
2.2 Unit Cell Design 8
2.2.1 Loadline Matching 8
2.2.2 LoadLine Matching Limitations 11
2.2.3 Load-pull techniques 12
2.3 Driver Design 13
2.4 Power Combining Techniques 14
2.5 Stability Analysis 14
2.6 Technology Selection Criteria 16

3 Network Theory for High-Efficiency Amplifier Design **19**
3.1 Introduction 19
3.2 Degrees of Freedom in Amplifiers 21
3.3 Key Factors for High-Efficiency Amplifiers 24
3.4 Optimum Cell Selection 25
3.5 Stacked Power Amplifier 29
3.5.1 Stack Concept 29
3.5.2 Conventional Stack Design Procedures 31

3.5.3 Limitations of the Existing Approach . . . 32
3.5.4 Network Theory for Stacked Power Amplifier: Motivation . . . 32
3.5.5 Stack Design Procedure . . . 33
3.5.6 2-port Transistor Modeling . . . 33
3.5.7 V&I Distribution for Maximum PAE . . . 34
3.5.8 Generic Stack Cell Design . . . 36
3.5.9 Stacked Stages for Maximum PAE . . . 40
3.5.10 Example: Three CB Stacked PA . . . 44
3.5.11 CE Stack Procedures . . . 48
3.5.12 CE Stack Design Procedure . . . 49
3.5.13 Example: Three CE Stacked PA . . . 50
3.5.14 Example: Neutralization Impact . . . 53
3.5.15 General Form of the Equations . . . 54
3.6 Area Progression Techniques (Parallel Combining Techniques) . . . 57
3.6.1 Motivation . . . 57
3.6.2 Analysis of Amplifier Designed by Area Progression Technique . . . 58
3.6.3 Wilkinson Power Combiner . . . 60
3.6.4 Pros . . . 62
3.6.5 Cons . . . 63
3.6.6 Proposed General Transmission Line Combiner . . . 64
3.6.7 Pros . . . 65
3.6.8 Limitations . . . 65
3.6.9 Example for Area Progression Technique: Three-Stage Amplifier 65
3.6.10 Area Progression Technique Efficiency . . . 67
3.7 Stacked Amplifier with Area Progression . . . 69
3.7.1 Motivation . . . 69
3.8 Design Guide for Amplifier Design . . . 73

4 Experimental Verifications for High-Efficiency Power Amplifiers (∼140GHz, 210GHz, and 300GHz) 76
4.1 Introduction . . . 76
4.2 250nm and 130nm InP HBT technology . . . 78
4.3 140GHz Power Amplifier with 20.8%PAE and 20.5dBm Output Power . . . 79
4.3.1 Amplifier Design . . . 79
4.3.2 Unit Cell design . . . 80
4.3.3 Driver design . . . 83
4.3.4 Combiner design . . . 84
4.3.5 S-Parameters measurements . . . 85
4.3.6 Power Measurements . . . 87
4.3.7 Summary . . . 89
4.4 131GHz Power Amplifier with 17.8%PAE and 200mW Output Power . . . 91
4.4.1 Power and Driver Cells Design . . . 91

4.4.2 Low Loss Transmission Line Combiner . . . 93
4.4.3 S-parameters Measurements . . . 96
4.4.4 Power Measurements . . . 98
4.4.5 Summary . . . 99
4.5 204GHz Stacked-Power Amplifiers . . . 101
4.5.1 Two Cell Amplifier Design . . . 101
4.5.2 Four-Cells Amplifier Design . . . 102
4.5.3 S-Parameters Measurements . . . 103
4.5.4 Power Measurements . . . 104
4.6 325GHz Stacked Power Amplifier with 8.6-13.6 mW Output Power . . . 106
4.6.1 Single Cell Power Amplifier Design . . . 106
4.6.2 2:1 Power Combined Design . . . 108
4.6.3 Measurement Results . . . 109
4.7 Summary and Conclusion . . . 112

5 210GHz Transmitter for MIMO Demonstration 113
5.1 Motivation . . . 113
5.2 210GHz Transmitter with ∼ 2dBm Output Power . . . 114
5.3 210GHz Transmitter with a simulated ∼ 18dBm Output Power . . . 116
5.3.1 210GHz Amplifier Design with ∼18dBm output power and 8% PAE 116
5.3.2 Amplifier Design . . . 118
5.3.3 Measurement Results . . . 120
5.3.4 Transmitter Simulation Results . . . 121
5.4 Comparison of the State-of-the-Art Amplifiers . . . 122
5.5 Packaging Options for 210GHz Transmitter . . . 123
5.6 2x2 Transmitter with Quartz Antenna . . . 124
5.6.1 Two Cells Amplifier Design . . . 125
5.6.2 Amplifier Measurement Results . . . 126
5.6.3 Quartz Antenna Design . . . 127
5.6.4 2x2 Array Design . . . 128

6 Massive MIMO Demonstration and Millimeter-Wave packaging 130
6.1 Introduction . . . 130
6.2 System Level Requirement: Link Budget . . . 133
6.3 Tile Design Overview . . . 133
6.3.1 Challenges in tileable approach . . . 135
6.4 Millimeter-Wave packaging . . . 135
6.5 Chip to Package Transition . . . 137
6.5.1 Wirebond . . . 137
6.5.2 C4 Flip Chip . . . 139
6.5.3 Copper Pillars . . . 139
6.5.4 Microstrip to Antenna Coupling . . . 140

6.6 LTCC vs PCB Approaches . . . 140
6.7 Interposer Design . . . 141
6.8 Carrier Board Design . . . 142
6.9 135GHz CMOS Transmitter Tile . . . 142
6.9.1 Copper Pillar Matching . . . 144
6.9.2 Packaging Results for a Single CMOS Chip . . . 144
6.9.3 Antenna Design . . . 146
6.9.4 CMOS to Antenna Transition . . . 148
6.9.5 Single Transmitter Element: Measurement Results . . . 148
6.10 135GHz CMOS Receiver Tile . . . 151
6.11 135GHz CMOS transmitter with InP PA Transmitter Tile . . . 152
6.11.1 Wirebond transition . . . 153
6.11.2 Thermal Consideration . . . 154
6.11.3 InP PA to Antenna and CMOS Transition . . . 155

7 Conclusions and Future Work 158

Bibliography 160

List of Figures

1.1 Atmospheric loss [1]. 2

2.1 Ideal and Real Loadline for class A operation plotted on the SOA. 9
2.2 (a) Transistor with output and input tuning. (b) Transistor with output tuning using an inductor and transformer. 10
2.3 Two stages power amplifier. 13

3.1 Unit Cell: a) Showing the circuit details. b) Omitting the circuit details using network theory. 21
3.2 Amplifier's degrees of freedom: a) Conventional stacked amplifiers with single element matching. b) Stacked power amplifiers with full impedance matching. c) Amplifier design with area progression technique under constant normalized base impedance. d) Amplifier design with area progression and impedance scaling techniques. 22
3.3 Large signal characteristic (Output power, gain, and PAE versus input power) for CE and grounded CB at 140GHz in 250nm InP HBT technology. 27
3.4 Schematic diagram of: (a) CE (b) CB with grounded base. (c) CB with 600fF base capacitor. 28
3.5 Conceptual drawing for three stacked with full impedance tuning PA; a) CB and b) CE topologies. c) Conventional stack representation for CB stack with limited tuning elements. 30
3.6 Equivalent transistor model in different representations a) Using simplified model. b) Including more parasitics. c) Using 2-port network. 34
3.7 Large signal characteristic (output power, gain, and PAE versus input power) for CE and grounded CB at 140GHz in 250nm InP HBT technology. 35
3.8 Schematic diagram of: (a) CE (b) CB with grounded base; (c) CB with 600fF base capacitor. 36
3.9 Generic CB stack cell showing the complex input, output powers, voltage and current distribution 37
3.10 Generic CB stack cell showing the complex input, output powers, voltage and current distribution. 38

3.11 Real output power, input power, PAE, and Gain, versus the base reactance. 40
3.12 a) Compressed Gain, Linear Gain versus the base reactance b) Compression level versus the base reactance 41
3.13 a) Real output power, input power, PAE, gain, and total gain versus the base reactance showing the optimum stack stage location using lossless matching network b) Block diagram for the amplifier. 42
3.14 a) Real output power, input power, ideal PAE, PAE including loss , gain, and total gain versus the base reactance showing the optimum stack stage location using lossy matching network (1dB per each interstage matching). b) Block diagram for the amplifier. 44
3.15 a) Required load impedance and actual input impedance contours versus the stack index. The black arrows show the required interstage impedance transformation in lossy network (1dB per each interstage matching) b) Block diagram for the amplifier. 45
3.16 CB example: a) schematic diagram of three CB stacked amplifier. b) Magnitudes of the internal voltages ($V_{out,t} - V_{in,t}$) versus the input power for the first stage c) Magnitudes of the internal currents (I_{int}) versus the input power for the first stage 46
3.17 CB example: a) Simulated and theoretical stages power are in perfect agreement. b) Simulated and theoretical stages impedances are in perfect agreement. 47
3.18 Analogy between CB and CE. 48
3.19 Real output power, input power, PAE, and Gain versus the emitter reactance for CE stack. 50
3.20 a) Compressed Gain, linear gain versus the emitter reactance b) Compression level versus the emitter reactance 51
3.21 CE example: a) Schematic diagram of three CE stacked amplifier. b) Simulated and theoretical stages power showing the location of the proper emitter reactance. c) Simulated and theoretical stages impedances highlighted at the location of the proper emitter reactance value 52
3.22 CE example: a) Magnitudes of the internal voltages ($V_{out,t} - V_{in,t}$) versus the input power for the first stage b) Magnitudes of the internal currents (I_{int}) versus the input power for the first stage 53
3.23 General form of neutralization. 54
3.24 Pout, gain, PAE with 20fF C_{CB} neutralization for lossless matching. . . 55
3.25 P_{outR}, gain, PAE with 20fF C_{CB} neutralization for lossy matching. . . . 56
3.26 Amplifier design using area progression technique: a) Block diagram. b) Visual representation. c) unit cell. 58
3.27 Block diagram of eight-50Ω cells. 61
3.28 Quarter wave transformation. 61
3.29 (a) 2:1 Wilkinson combiner. (b) Even mode analysis. (b) Odd mode analysis. 62

3.30 a) Proposed 8:1 transmission-line combiner for 50Ω load. b) An 8:1 Wilkinson combiner (with bridging resistors omitted) 63
3.31 Stack design contours at constant normalized base impedance. 66
3.32 a) Output power, input power, gain, and PAE versus the areas scaling factor. b) Amplifier block diagram. 67
3.33 Z_L and Z_{in} as a function of the stage index. It shows the required interstage impedance transformation contours 68
3.34 P_{outR}, gain, PAE versus the area progression factor including splitter loss. 69
3.35 a) Contour plots for the output power function of the normalized base impedance and area progression factor. b) Contour plots for the gain function of the normalized base impedance and area progression factor. . 71
3.36 a) Output power contours showing the power of the first stage's power. b) Contour for the input power highlighting the design contour for the second stage. c) General amplifier form considering impedance and area progression techniques. 72
3.37 a) Output power contours showing the design procedures. b) Contour for the input power highlighting the design contours. c) Block diagram for amplifier designed with area and stacking techniques. 73
3.38 a) Impedance chart showing the load and input impedance versus the normalized base impedance. b) Impedance values for the amplifier after applying the proper scaling factor. 74
3.39 CB example using stacking and area progression techniques: a) Schematic diagram. b) Simulated and theoretical stages power showing the location of the proper base reactance. c) Simulated and theoretical stages impedances highlighted at the location of the proper base reactance value. 75
3.40 Amplifier design guideline. 75

4.1 Schematic cross section of a) 130nm InP HBT. b) 250nm InP HBT technologies[2]. 79
4.2 Schematic diagram of: (a) CE. (b) CB with grounded base. (c) CB with 600fF base capacitor. 80
4.3 P_{out}, gain, and PAE for CE, grounded CB, and CB with base capacitor. . 81
4.4 Transistor footprint for compact 4 fingers connected together. Each is 6μm emitter length. Total emitter periphery is 24μm 82
4.5 (a) Schematic diagram of two combined power amplifier cells driven by a single driver cell. (b) Corresponding layout. 83
4.6 Schematic diagram of: (a) Driver stage with input/output matching circuits. (b) Driver layout. 84
4.7 Schematic diagram (a) 4:1 low loss transmission line combiner for 50Ω load. (b) 4:1 Wilkinson power combiner (with bridging resistors omitted) for 50Ω load. 85
4.8 (a) Chip micrograph of the power amplifiers. The area is 1.08mm 0.63mm including the pads. (b) Amplifier block diagram. 86

4.9 Measured (solid) and simulated (dashed) S-parameters. 87
4.10 Power measurement setup. 88
4.11 Measured and simulated output power, PAE, and gain versus the input power at 140GHz. 89
4.12 Measured saturated output power, PAE and the compressed gain versus frequency. 90
4.13 Amplifier block diagram. 92
4.14 Schematic diagram of: a) Two combined power amplifier cells. The pair of power cells are driven by a single driver cell. b) Driver cell with input and output matching networks. 93
4.15 a) Proposed 8:1 transmission-line combiner for 50Ω load. b) an 8:1 Wilkinson combiner (with bridging resistors omitted). 94
4.16 Simulations comparing the insertion losses and input reflection coefficients of the two designs. 95
4.17 Chip micrograph of the PA (1.23mm 1.09mm) including the pads. 96
4.18 S-parameters measurements setup. 97
4.19 Measured (solid) and simulated (dashed) S-parameters. 98
4.20 Power measurement setup. 99
4.21 a) Measured and simulated output power, PAE, and gain versus the input power at 140GHz. b) Measured P_{out}, PAE, and gain versus the input power at 127, 131, and 143GHz. 100
4.22 Measured saturated output power, PAE and the compressed gain versus frequency. 101
4.23 Simplified schematic diagrams of a 204GHz, 3:1 series-connected stack with gain-matching on Q_1 and power-matching on Q_2 and Q_3. 103
4.24 (a) Die photo of design 1, and (b) Design 2, with 2:1 transmission-line combining. The die areas are 0.63 mm × 0.54 mm, and 0.7 mm × 1.3 mm respectively. 104
4.25 Measured and simulated S-parameters of a) Design 1 a) Design 2. 105
4.26 a) Measured and simulated output power, PAE, and gain for Design 1. b) Measured and simulated output power, PAE, and gain for Design 2. . . 105
4.27 PA unit cell (two stacked HBTs with matching circuits). Q_1 and Q_2 are two finger transistors each 5μm emitter length. The inductors (red) are added to represent the base inductance model and are not real inductors. 107
4.28 PA unit cell (Chip micrograph of the power amplifiers: a) Design #1 (dimensions = 600 μm 585 μm). b) Design #2 (dimensions = 0.98 mm 1 mm). 108
4.29 PA unit cell (a) Simulated and measured s-parameters of the unit-cell design. b) Comparison of measured and resimulated s-parameters of the unit-cell design assuming an additional 3.5 pH base feed inductance per two-finger each 5 μm emitter length HBT. 109

4.30 a) Simulated and measured power transfer characteristics at 325GHz of the unit-cell design. b) Comparison of measured and resimulated power transfer characteristics at 325GHz of the unit-cell design assuming an additional 3.5 pH base feed inductance per two-finger each 5 μm emitter length HBT. 110
4.31 a) Simulated and measured s-parameters of the 2:1 power-combined design. b) Simulated and measured power transfer characteristics of the 2:1 power-combined design. 111
4.32 a) Measured output power at different frequencies versus the input power for design#1. b) Measured output power at different frequencies versus the input power for design#2. 112

5.1 210GHz transmitter with a ∼2dBm output power (Courtesy of Munkyo Seo). 115
5.2 Measured and simulated results for the 210GHz transmitter with 2dBm output power. a) Conversion gain. b) Output power versus the baseband input power (Courtesy of Munkyo Seo). 116
5.3 210GHz transmitter with simulated ∼18dBm output power. 117
5.4 a) Die photo, area is 1.2mmx0.95mm. b) Amplifier block diagram. . . . 118
5.5 Schematic diagram of: a) Two combined power amplifier cells. b) Driver cell. 119
5.6 Measured (solid) and simulated (dashed) S-parameters at different bias conditions a) DC power (445mW). b) DC power (858mW). 120
5.7 Power measurement setup: a) calibration mode. b) measuring the PA. . . 122
5.8 Power measurement setup: a) Measured output power with associated PAE and compressed gain versus the frequency reported at saturated output power. b) Measured and output power, PAE, and gain versus the input power at 194GHz. 123
5.9 Simulation results for 210GHz transmitter with ∼19dBm. a) Up conversion gain. b) Large signal characteristic. 124
5.10 a) Die photo, area is 0.58mmx1.1mm. b) Amplifier block diagram. . . . 126
5.11 a) Measured (solid) and simulated (dashed) S-parameters at different bias conditions. b) Simulated large-signal characteristics at 210GHz. 127
5.12 Quartz Design: a) EM simulation stack, b) Patch and coupler dimensions (Courtesy of Zhe). 128
5.13 2x2 Transmitter array with Quartz antenna. The thesis work is highlighted by yellow boxes. Other blocks are designed by Munkyo and antenna is designed by Zhe. 129

6.1 a) Hardware-efficient imaging. b) Cooperative/sparse imaging (Courtesy of Mark Rodwell). 131
6.2 a) Point to point MIMO array. b) Cartoon drawing for single tile (Courtesy of Mark Rodwell). 132

6.3 a) Massive MIMO hub. b) Cartoon drawing for MIMO array. c) Single tile (Courtesy of Mark Rodwell). 132
6.4 a) Cross section of the LTCC approach **(this work)** showing the interposer, chips, PCB carrier board with the DC and RF connectors. b) Top view of the LTCC approach. c) Cross section of the low-cost PCB approach (Courtesy of Ali Farid). d) Top view of the low-cost PCB approach. 134
6.5 a) Cavity approach to reduce the wirebond length. b) Chip mounted on the surface of the LTCC. c) Epoxy leaking problem. 138
6.6 a) Sketch for the CMOS chip filpped on the interposer. b) Drawing for the copper pillar. c) Drawing for the SOP. 139
6.7 Wiring stack for the ceramic interposer. 142
6.8 a) Wiring stack of the PCB. b) Cross section in the wiring stack showing the RF and DC routing techniques 143
6.9 a) Photos for the transmitter module showing the LTCC ceramic interposer and PCB carrier board. b) Cartoon drawing for the CMOS transmitter chip to the interposer showing the different type of transitions. c) Close look on the LTCC ceramic interposer showing the antenna arrays and chip footprints. 144
6.10 a) HFSS model for copper pillar. b) Different views for the transition. c) S-parameters simulations. d) S-parameters simulations on smith chart. . 145
6.11 Packaging results for 135GHz transmitter with copper pillar transition: a) CMOS transmitter chip mounted on LTCC interposer. b) Measurement setup. c) Measured transmitter's output power versus the input power including the copper pillar transition loss d) Transmitter conversion gain versus the output frequency 146
6.12 Antenna Design: a) Modular element. b) Eight series fed patch antenna. 147
6.13 a) Photo for the eight-element series fed patch antenna and the chip footprint. b) Measured and simulated radiation patterns at the azimuth and elevation. at 135GHz. c) Measured and simulated input reflection coefficient and gain 149
6.14 Antenna radiation pattern Setup from different angles (Courtesy of Ali Farid). 150
6.15 Single CMOS transmitter channel with eight series fed patch antenna array) a) photo. b) EIRP at elevation and azimuth. c) conversion gain versus the output frequency. d) EIRP at broadside direction at 135GHz versus the input power (Courtesy of Ali Farid). 151
6.16 Single CMOS transmitter channel with eight series fed patch antenna array a) Output power versus the input power at 135GHz at fundamental and IM3 b) LO tuning range versus the LO frequency (Courtesy of Ali Farid). 152

6.17 Packaging results for 135GHz receiver with copper pillar transition: a) Receiver conversion gain versus the output frequency. b) Measured receiver's output power versus the input power, including the copper pillar transition loss. 153
6.18 a) Photos for the receiver module showing the LTCC ceramic interposer and PCB carrier board. b) Cartoon drawing for the CMOS receiver chip to the interposer showing the different type of transitions. c) Close look on the LTCC ceramic interposer showing the antenna arrays and chip footprints. 154
6.19 a) Photos for the high-power transmitter module (CMOS with InP PAs) showing the LTCC ceramic interposer and PCB carrier board. b) Cartoon drawing for the CMOS transmitter and InP chips to the interposer showing the different type of transitions. c) Close look on the LTCC ceramic interposer showing the antenna arrays and InP and CMOS chips footprints. 155
6.20 a) HFSS model for the wirebond transition. b) Simulated S-parameters. 156
6.21 Thermal simulation: a) Amplifier is mounted directly on a copper block. b) Amplifier is mounted on ceramic layer with thermal vias. c) Amplifier is mounted on ceramic piece without thermal vias. 156
6.22 a) CMOS integrated to an InP chip and an eight-element series-fed patch antenna. b) Simulated S-parameters for the transition between InP and CMOS chips. c) Simulated antenna gain and the input reflection coefficient. 157

List of Tables

4.1 DC biases for S-parameters 86
4.2 DC biases for power measurements. 88
4.3 Comparison between state-of-the-art D-band amplifiers. 90
4.4 Comparison between state-of-the-art 130-140GHz amplifiers. 100

5.1 State-of-the-art High-Efficiency G-Band Amplifiers 125

Chapter 1

Introduction

1.1 Millimeter Wave for Next Communication Generation

There is an increasing demand for high data rate wireless communication [3]. The population is getting larger and everyone demands access to high-speed internet, HD video, Skype... etc. On the other hand, we have a limited spectrum. Communication engineers are doing their best to increase spectrum efficiency by using higher-order modulation schemes to send more bits in the same frequency. But there is a point where we need to exploit more frequency bands.

Considering millimeter frequencies for the next communication generation exploits more frequency spectrum and the shorter wavelengths support massive spatial multiplexing [4], [5], and [3]. Unfortunately, λ^2/R^2 path loss and weather attenuation are high. This demands building mm-wave transceivers with high output powers [1]. Building transceivers at high frequency requires advanced technologies with high power gain cutoff frequency (f_{max}) such as InP [2].

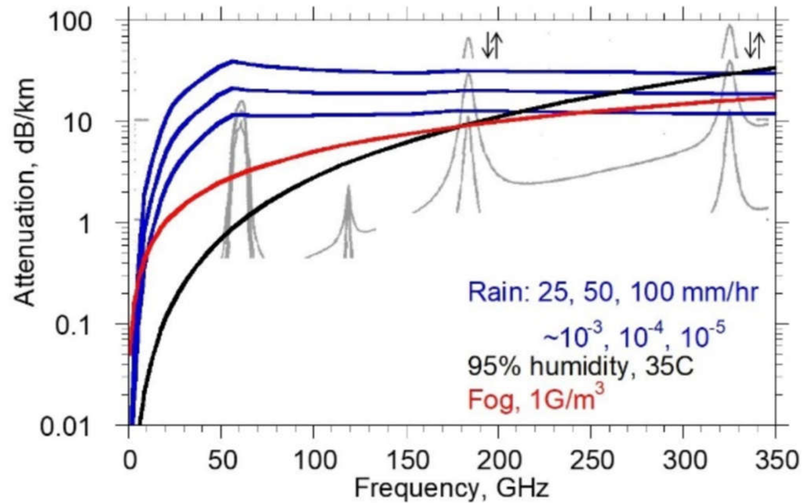


Figure 1.1: Atmospheric loss [1].

In this thesis, we provide solutions beyond the research limit. It is great to have a working transceiver on the circuit level. However, there are limited applications for the bare die. We spent a considerable amount of time thinking about how to package the IC so they can be usable in a real communication system. Millimeter-wave packaging is one of the most challenging parts of the design. It requires different types of expertise. We had lots of interactions with the assembly houses such as Kyocera [6] to comply with their specifications and tolerance.

1.2 Dissertation Contributions and Organization

Chapter 2 reviews the millimeter-wave power amplifier fundamentals. We provide the necessary background for beginners. We start from the system level that defines the requirements for the power amplifier. The power amplifier basics are covered and the concepts of loadline and load-pull matching for maximum saturated output power are introduced. The power amplifier design starts from a single cell, moving to a practical

power amplifier which demands more gain and power. The design techniques are briefly discussed here while the following chapter presents detailed analysis and design. Power amplifier stability is demonstrated in different ways such as stability factors, transient analysis... etc.

Chapter 3 provides a design guide for optimum amplifier design. The amplifier's degrees of freedom are discussed. We can get higher output power by stacking, by scaling the stage's area, or combined approach. We propose a network theory that is considered the core of the chapter. The network theory introduces a new design technique by a two-port network. First, the conventional stack is reviewed and the limitations are discussed. Then we use the network theory to design the stack with two-port network techniques. Using the network theory in the stack adds more degrees of freedom and simplifies the design. The interstage matching is designed as a two-port network with full impedance matching. From the network theory, we can easily design with arbitrarily complex transistor models, complex interconnects, arbitrarily matching circuits, include neutralization techniques, and more.

We also cover parallel power combining techniques such as Wilkinson. We present the pros and cons of Wilkinson then we introduced a proposed general transmission line combiner. The proposed combiner is much more compact and has lower loss compared to the Wilkinson combiner. We present different ways of implementation based on the number of combined cells.

Finally, we combined the area progression techniques with the stack approach to provide a design guide for power amplifier considering most of the degrees of freedom. The network theory computes the efficiency for different design techniques so we can select the approach that gives the highest PAE. This chapter covers most of the intellectual

points in power amplifier design.

Chapter 4 presents lots of experimental results. We have designed lots of amplifiers at 140GHz, ∼210GHz, and ∼310GHz. The amplifiers are designed in 250nm and 130nm InP HBT technologies from Teledyne. The amplifiers demonstrate record PAE across all frequency bands. This chapter discusses the practical circuit implementation in real life. For each of the presented amplifiers, we analyze the power and driver cells. We stated the justification for such a choice. The combiner design is also demonstrated. After presenting the design details, we present the experimental verification. We have done S-parameters measurements and large-signal power measurements for most of the amplifiers. There are still ongoing measurements for newer versions. Most of the data are presented in several publications.

In **Chapter 5**, we demonstrate different variants of 210GHz transmitter. Prof. Munkyo Seo is the leading designer for the transmitter. Munkyo designed all the transmitter building blocks except for the power amplifier. The amplifiers are designed by the thesis author. To reduce the risk, the first transmitter does not have a high-output power amplifier. The second transmitter integrates a high-efficiency power amplifier. We also considered packaging options for the transmitter. We designed a 2x2 transmitter array. We followed the packaging approach that is proposed by UCSD and Zhe designed the Quartz antenna that is integrated with the 210GHz transmitter.

Massive MIMO demonstration and mm-wave packaging is covered in **Chapter 6**. We have 140GHz CMOS transceivers, designed by Ali Farid. GlobalFoundries gave us access to the advanced Copper pillar option. We also have bare dies for InP power amplifiers. The purpose of this chapter is to package those chips and build a tile in a modular fashion. We go step by step, starting from chip to package transition and matching.

Then demonstrating a single channel transmitter and receiver which consists of CMOS transmitter or receiver matched to a series fed patch antenna. Then we present the tile design which holds eight transmitters or receivers. We repeat the same steps for the higher power module where we have high output power InP power amplifiers. The chapter gives a great depth for mm-wave packaging design and challenges.

1.3 Permissions and Attributions

The material in this dissertation is partly based on the following publications. The dissertation author is the primary contributor to these published works and the co-authors have approved the use of the material for this dissertation.

1. **A. S. H. Ahmed**, Munkyo Seo, A. A. Farid, M. Urteaga, and M. J. W. Rodwell, "**A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology**, "2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 492-495.

2. **A. S. H. Ahmed**, Munkyo Seo, A. A. Farid, M. Urteaga, and M. J. W. Rodwell, "**A 200mW D-band Power Amplifier with 17.8% PAE in 250-nm InP HBT Technology**," accepted to 2020 15th (EuMIC), Utrecht, 2020

3. **A. S. H. Ahmed**, A. Simsek, A. A. Farid, A. D. Carter, M. Urteaga, and M. J. W. Rodwell, "**A W-Band transmitter channel with 16dBm output power and a receiver channel with 58.6mW DC power consumption using heterogeneously integrated InP HBT and Si CMOS technologies"**, 2019 (IMS), Boston, MA, USA, 2019.

4. **A. S. H. Ahmed**, A. A. Farid, M. Urteaga, and M. J. W. Rodwell, "**204GHz Stacked-Power Amplifiers Designed by a Novel Two-Port Technique**, 2018

13th European Microwave Integrated Circuits Conference (EuMIC), Madrid, 2018, pp. 29-32.

5. **A. S. H. Ahmed**, A. Simsek, M. Urteaga, and M. J. W. Rodwell, "**8.6-13.6 mW Series-Connected Power Amplifiers Designed at 325 GHz Using 130 nm InP HBT Technology**, 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), San Diego, CA, 2018, pp. 164-167.

Chapter 2

Millimeter-Wave Power Amplifier Fundamentals

2.1 Introduction

Power amplifiers are the key components in any transmitter. Based on Friis [7] equation (2.1), the amplifier's output power limits the transmission range for a required minimum received power. Efficiency is one of the key factors in PA. High-efficiency PA dissipates less heat and the battery lasts longer. This is necessary for any practical communication system. The power amplifier design starts with a unit cell. There are many different matching techniques (gain, power, PAE... etc.). Proper matching should be considered to achieve the required purpose. PA biasing defines the class of operation. Each class has its own characteristics (different gain, efficiency, and power) [8]. In practical cases, a single unit does not satisfy the system level requirement in terms of the required output power or gain. Multiple cells could be combined with various power combining techniques to reach the required power level. Driver stages are necessary to

increase the gain.

$$\frac{P_r}{P_t} = \frac{A_r A_t}{d^2 \lambda^2} \tag{2.1}$$

This chapter will review the unit cell and driver design considerations. Different matching techniques will be reviewed. Then, we will cover briefly the tradeoff between different classes especially at mm-wave frequencies. Different power combining techniques will be presented. Finally, we will show the challenges in the PA stability simulation.

2.2 Unit Cell Design

There are different types of matching to achieve different purposes. In power amplifiers, the main objective is to deliver the maximum saturated output power from the cell. This matching is called load line matching [8] or load-pull techniques. We will focus on class A design.

2.2.1 Loadline Matching

The relation between the collector (drain) current and collector to emitter (drain to source) voltage could be represented graphically (Fig. 2.1). There is a maximum voltage which is defined by the transistor breakdown and maximum current density. Each technology defines those values and is usually referred to as a safe operating area (SOA). The transistor should reach the maximum voltage and current simultaneously to deliver the maximum output power. The blue straight line represents the ideal contour for maximum output power. Any deviation from the straight line leads to early saturation for the current or the voltage and leads to lower power.

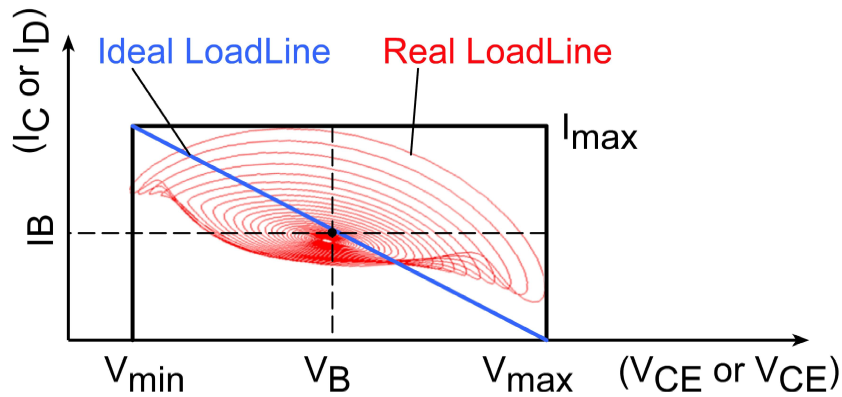


Figure 2.1: Ideal and Real Loadline for class A operation plotted on the SOA.

Real transistors have parasitics. Therefore, the relation between the internal collector (drain) current and V_{CE} (V_{DS}) becomes elliptical and no longer linear (red curve in Fig. 2.1). In addition, the slope of the loadline is defined by $1/(R_L)$ where R_L is the load impedance presented to the transistor. Generally, there is no guarantee that this impedance matches the optimum loadline impedance for maximum output power. The blue line represents the real loadline contours for a real transistor. The transistor will not reach the maximum voltage and current swing simultaneously. Either the voltage or the current will clip earlier.

The output Tuning network (Fig. 2.2) is necessary to transform the load impedance to the optimum loadline impedance for maximum output power. The transistor parasitics are tuned by a reactive element (inductor). This ensures that the loadline contours become linear. The optimum slope could be achieved by controlling the transformer ratio. This aforementioned matching method is just an example and there is an infinite number of ways to achieve the optimum impedance. With the optimum loadline impedance, the transistor can achieve the maximum voltage and current swings. This leads to maximum

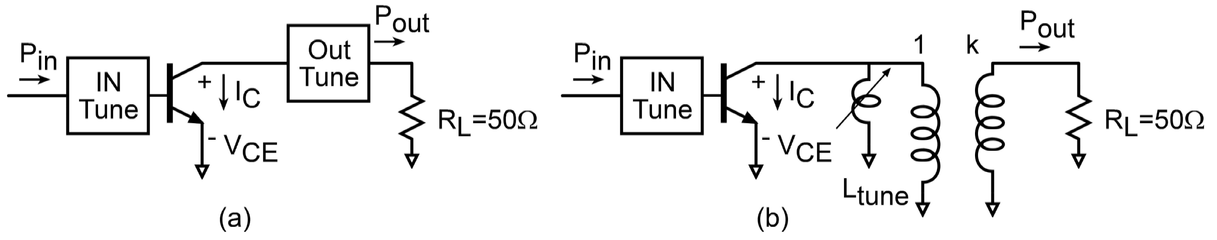


Figure 2.2: (a) Transistor with output and input tuning. (b) Transistor with output tuning using an inductor and transformer.

output power (class A) of (2.2)

$$P_{out,max} = (V_{max} - V_{min})I_{max}/8 \tag{2.2}$$

Transistor biasing determines the class of operation and the loadline shape. Each class has its own characteristic. In class A (Fig. 2.1), the transistor has maximum of 50% drain efficiency and is biased at:

$$V_B = \frac{V_{max} - V_{min}}{2} \tag{2.3}$$

$$I_B = \frac{I_{max}}{2} \tag{2.4}$$

Class A is commonly used at mm-wave frequencies since it offers the highest power gain. Class B has a higher drain efficiency (78.5%). However, it has a lower gain compared to class A which makes the design more challenging. More sophisticated amplifier design such as class F, D, switching amplifier... etc. becomes very challenging. For example, if we design a 210GHz power amplifier, we want to shape the harmonics at 420GHz, 630GHz... etc. This requires careful transistor modeling at such frequencies which is

very hard. Additionally, the matching loss might make such techniques less practical for current technologies. Things could change with better technologies and transistor models.

2.2.2 LoadLine Matching Limitations

It is not sufficient to maximize only the PA's output power. The PA can deliver a lot of power, but it will not be practical if the gain is too low. Since the stage will require input power comparable to the output power. This shows the limitation of the drain efficiency (η_{drain}) which focuses only on the output power and ignores the gain. That is why power added efficiency (PAE) is widely used to report the efficiency instead of the drain efficiency. The PAE definition (2.6) includes the gain. Therefore, optimizing for the PAE becomes more practical.

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} \tag{2.5}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta_{drain}(1 - \frac{1}{Gain}) \tag{2.6}$$

Loadline matching technique, in section 2.2.1 is an intuitive way to design the output tuning network yet, it did not consider the stage gain. So, this technique optimizes the drain efficiency and does not provide the best PAE. Loadline technique is acceptable for high gain systems since the drain efficiency and PAE are almost the same. However, it becomes tricky for low gain stages.

Power amplifier operation is a large signal. The small-signal approximation is no longer valid. Transistor parameters (g_m, C_{be}, and f_t) are function of bias. This means that power gain cutoff frequency f_{max} varies across the loadline contours. The optimum

loadline impedance, in section 2.2.1, did not consider the transistor speed variation along the contour.

In the loadline matching, we presumed that the transistor parasitics could be tuned by a reactance element and the load line becomes linear. This is valid for a linear system. As the input power increases, the transistor starts to saturate and produce higher-order harmonics. The loadline can no longer be linear and the optimum impedance could differ from the one at lower input power. Fortunately, in practical communication systems, we usually, work in the linear regime before OP_{1dB}. This is to support higher-order modulation schemes. This means that the loadline approach is still a reasonable way of design.

2.2.3 Load-pull techniques

Load-pull technique is another way to get the optimum impedance for maximum saturated output power or PAE. This is a numerical way to determine the optimum load impedance. Modern software such as ADS offers templates for such simulation. The simulator can sweep all the possible load impedances and calculate the output power, gain, PAE... etc. at each point. Then it generates contours on smith charts. Based on those contours, we can determine the optimum load impedance for maximum output power, PAE, or other parameters.

Load pull is based on an exhaustive search, so it is less intuitive compared to the loadline technique. However, it offers more degrees of freedom compared to the loadline. The output power and associated gain can be calculated so, we can get the optimum impedance for PAE which is hard to find by loadline. Also, there are other templates to consider higher-order harmonics optimization. The optimum load impedance could be

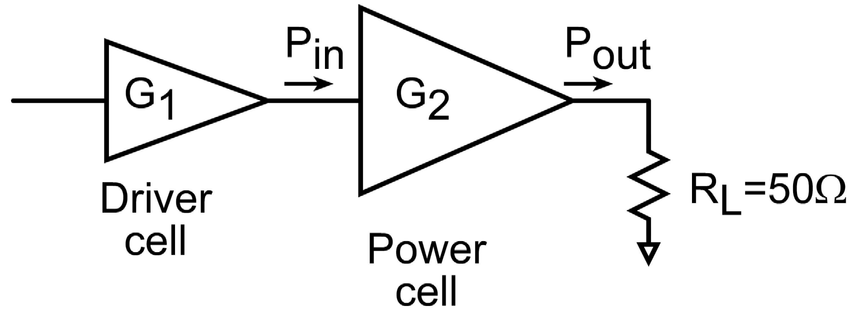


Figure 2.3: Two stages power amplifier.

calculated at each harmonic which is not easy from the loadline.

Load-pull contours are calculated based on specific input power. It is important to generate those contours at the required output power. If the amplifier should work at OP_{1dB}, we should generate that impedance at this power level.

2.3 Driver Design

Usually, a single-stage amplifier does not satisfy the required gain and more stages are required. Driver design procedure is similar to the unit cell design in Section 2.2 with different output power levels. The driver should be carefully designed to operate at its highest PAE when it delivers the necessary input power for the power cell. The PAE of the multi-stage amplifier could be calculated from the individual PAE for each stage. There are various ways to deliver the required power with the maximum PAE; transistor scaling or stacking concepts are good candidates for delivering lower power while maintaining high PAE. More details will be described in Chapter. 3

2.4 Power Combining Techniques

The power cell has a limited output power. We can keep increasing the number of fingers to get higher output power yet, there is maximum cell size. At mm-wave frequency, the wavelength is very small. The cell size is a reasonable fraction from the wavelength. Increasing the number of fingers beyond a certain limit will increase the routing loss between fingers. The required load impedance becomes smaller and harder to match with reasonable loss. A big cell means that it dissipates a lot of heat. This reduces the combining efficiency.

There are some techniques to increase the output power and they will be presented in detail in Chapter 3. We can utilize the stacking concept where transistors are added in series allowing higher voltage swing at the output. We also can use parallel combiner techniques such as Wilkinson or more general transmission line combiners. This provides an easy way to combine and match the cells. Or we can utilize both techniques (stack and parallel combiner). The critical point is how to do the proper design given all those degrees of freedom and that is what we are going to address in Chapter 3.

2.5 Stability Analysis

Stability is one of the most important steps in amplifier design. Checking the stability at mm-wave frequency [9] is different from analog amplifiers [10]. At mm-wave frequency, we must make sure that the amplifier is unconditionally stable for different load or source impedances. That might raise a question why do not we just stabilize the transistor for a particular load impedance? and the answer is that it is hard to get clean load impedance which comes from the nature of the measurement. In mm-wave measurement, we use microwave probes. We cannot guarantee that the impedance is precisely 50Ω. So, a

conditionally stable design would be very risky. There are different ways to analyze the amplifier stability. The analog technique such as gain margin and phase margin is rarely used since it assumes fixed load impedance which is not enough at mm-wave frequency.

The stability factor and stability measure are very common techniques at mm-wave frequency. Those are techniques to check the amplifier stability for all the possible combinations of load and source impedances. Stability factor and measure could be represented as a function of S-parameters. The basic idea is that we want to make sure the input and output reflection coefficients are less than 1. This guarantees that there are no negative impedances that might cause oscillation. We can satisfy this condition if the stability factor is more than 1 with a positive stability measure at all frequencies. It is critical to check the stability in band and more importantly out of band. The amplifier fails even if the oscillation is out of band.

CAD tools [11], [12] offers small-signal S-parameters and large-signal one. We can calculate the stability factor and measures from the small signal or large signal. Power amplifier design is a large operation so, it is more prudent to check the large-signal stability parameters at the expense of the simulation time.

Rigorous simulation for the stability is hard and we should perform all the possible techniques to reduce the possibility of oscillation. It is a good habit to run a transient analysis for the amplifier to make sure that there is no anomaly or oscillation. We can run the transient analysis at the frequency of operation. Also, we can apply just a trigger to see whether we have an oscillation or not. It is tricky to detect the oscillation using transient analysis since you should give the simulator the approximate oscillation frequency. This might be useful if we know the frequency of oscillation but in many cases, it is not known. The other challenge in transient simulation is that we are using

s-parameters files extensively and sometimes it causes convergence problems.

Power supply oscillation is one of the crucial problems in power amplifier design. The main reason is that there is no mature framework to do such a check. The amplifier has DC and RF pads. We usually use microwave probes for the RF input and RF output. The manufacturer guarantees that the impedance of such probes to be $\sim 50\Omega$. Unfortunately, the impedance of the DC probe is unknown. This means that we have more than a 2-port system and we want to check the stability of such systems. To the best of my knowledge, multiport system stability has not been addressed in CAD tools yet. The naive way that I followed is to use the 2-port stability check with varying the impedance of the DC terminals to make sure that it is stable for all the possible combinations.

Isolation between amplifier stages is important especially for high gain systems. Suppose that we have a multistage amplifier sharing the same supply lines (V_{CC} and V_{BB}). Part of the signal may leak from the output to the input and this might cause oscillation problems. Capturing the isolation problem requires that we simulate the whole amplifier together which demands huge simulation resources. Since we do not have access to those fast servers, we add a conservative amount of bypass capacitors with small series resistors. This helps in increasing the isolation between stages.

2.6 Technology Selection Criteria

Power amplifier demands careful technology selection. There are multiple technology options. We can use silicon or III-V technologies. The factors are:

1) power gain cutoff frequency (f_{max}). This parameter is important especially when we design a high-frequency amplifier. Technologies with a higher f_{max} compared to the

operating frequency can get reasonable gain which is necessary for amplifiers design. The design becomes challenging when the operating frequency is close to f_{max}. We can use some neutralization techniques to boost the gain but are still quite complicated. Generally, III-V technologies such as InP or SiGe have higher f_{max} than CMOS. But there are recent advances in CMOS technology and f_{max} is getting higher and higher.

2) Breakdown voltage and current density: since our focus is building power amplifiers. The breakdown voltage and current density strongly determine the maximum output power that we can get. Although it might be obvious that we need higher f_{max}, higher breakdown voltage, and higher current density, we will see that they are going in opposite directions. The more that we get higher f_{max}, the less breakdown voltage that we get. So, proper selection for both parameters is important. III-V technologies have usually significantly higher breakdown voltage and current density compared to CMOS.

3) Wiring stack and dummy filling: The wiring stack and dummy filling play an important role in the high-frequency design. We may have a technology with high f_{max} for the transistor level but as soon as we include the wiring stack the performance degrades significantly. Wiring metal stack with large separation permits implementing low loss transmission lines. The other challenge is the dummy filling and metal density. Silicon technologies have lots of metal layers and each one requires a certain density. So, we have to add dummy metal to satisfy this condition. Those dummies are hard to simulate and cause performance degradation. III-V technologies such as InP have fewer metal layers and we do not have this stipulation. We can have continuous thick metal layers without any dummies which helps in microwave circuit design.

Yield, cost, and integration are other important factors. Based on the required application we can determine the right decision. III-V technologies are usually much more

expensive than CMOS. Additionally, the CMOS yield is pretty high. For mass production requirements such as cell-phone industries, the cost is a huge factor. Low-cost solutions are definitely preferable.

Chapter 3

Network Theory for High-Efficiency Amplifier Design

3.1 Introduction

Practical amplifiers demand more gain and power. Series (stack) [13], [14], [15], [16], [17], [18], [19], [20], and [21] or parallel power combining [22], [23], and [24] techniques are well known techniques in power amplifiers design. In this chapter, we will review the design procedures for stacked power amplifiers and standard Wilkinson power combiner. Conventional stack design procedures have limitations since the design relies on the transistor equivalent circuit model, which is, by necessity, simple and specific. The conventional procedures [25] ignore the interconnect parasitics and the matching loss. We proposed a network theory for stacked design, which relies on the network representation for the transistor and tuning elements. From the theory, we can determine the base impedance, required load impedance, and actual input impedance for each stage. Therefore, the interstage matching is well defined, including the complicated transistor models, parasitic, or matching loss. The theory models the transistor as a two-port net-

work, which broadens its usage. This means that the theory is valid for any technology (III-V or CMOS), any frequency, and any topology (common emitter or common base).

Wilkinson is an example of parallel power combining. Wilkinson design [26] is easy, yet it is bulky and lossy. We introduce a more general transmission line combiner that uses a single $\lambda/4$ transformation section. The proposed combiner is compact and has lower losses compared to Wilkinson. We integrate the parallel combining techniques in the network theory to add more degrees of freedom. Now, the network theory provides design procedures for stacked power amplifiers and parallel combining techniques at the same time. The theory shows the efficiency degradation in each approach and provides a design guide for the best approach.

We reviewed the power amplifier fundamentals in Chapter 2. In this chapter, we present a proposed network theory for power amplifier design. The network theory considers most of the amplifier degrees of freedom, such as stacking or parallel power combining techniques. We will review the conventional way of staked power amplifier design with the limitations then introduce the network theory framework to solve those issues.

The theory outcome gives insight regarding the invariance of PAE w.r.t to the feedback. It compares the PAE of different typologies (CE versus CB). The theory gives insight pertaining to arbitrarily neutralization techniques in a lossy network. Class A power amplifier is commonly used at mm-wave frequencies so we applied the theory mainly on the fundamental frequency, yet the theory could be extended to include higher-order harmonics and establish a framework for other amplifier classes.

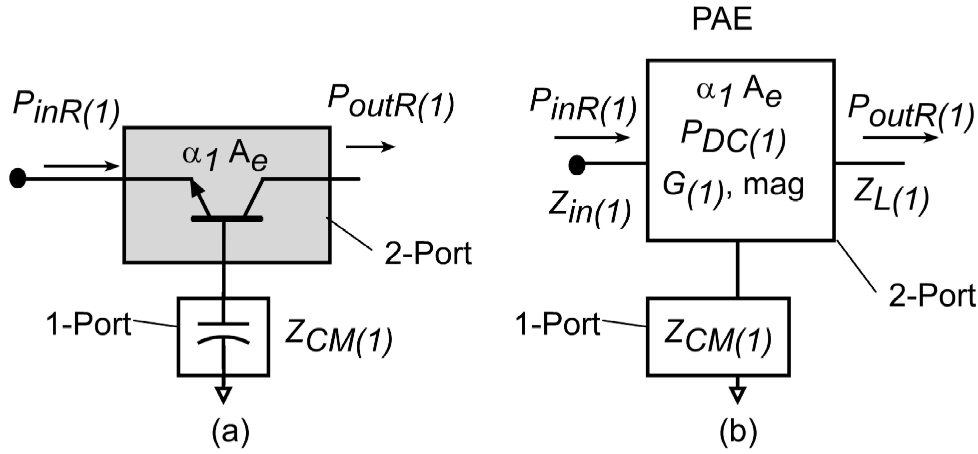


Figure 3.1: Unit Cell: a) Showing the circuit details. b) Omitting the circuit details using network theory.

3.2 Degrees of Freedom in Amplifiers

In power amplifier design (Chapter 2), the transistor is matched to produce the maximum saturated output power or maximum PAE to work as a power cell. The transistor could be in CE or CB configuration. The transistor biasing determines the class of operation (A, AB, C... etc.). Each class has its own characteristics (efficiency, gain, or linearity). Usually, a single power cell has a limited power and gain. Practical amplifiers demand higher output power and gain compared to a single power cell. Let's consider a CB topology (Fig. 3.1a shows the circuit details and Fig. 3.1b uses network theory representation hiding the circuit details) with total emitter area of (A_e) and area progression factor (α_1=1) biased at class A. This cell produces certain amount of output power ($\mathrm{P}_{\mathrm{outR}(1)}$), has certain gain ($G_{(1)}$), and by necessity requires certain amount of input power ($\mathrm{P}_{\mathrm{inR}(1)}$). We are assuming that this cell has a base impedance of $Z_{CM(1)}$.

The output power of this cell could be increased by either increasing the base impedance (stack concept) or increase the area progression factor (α). We can get higher gains by adding more stages. According to the area progression factor α_1 and the normalized base

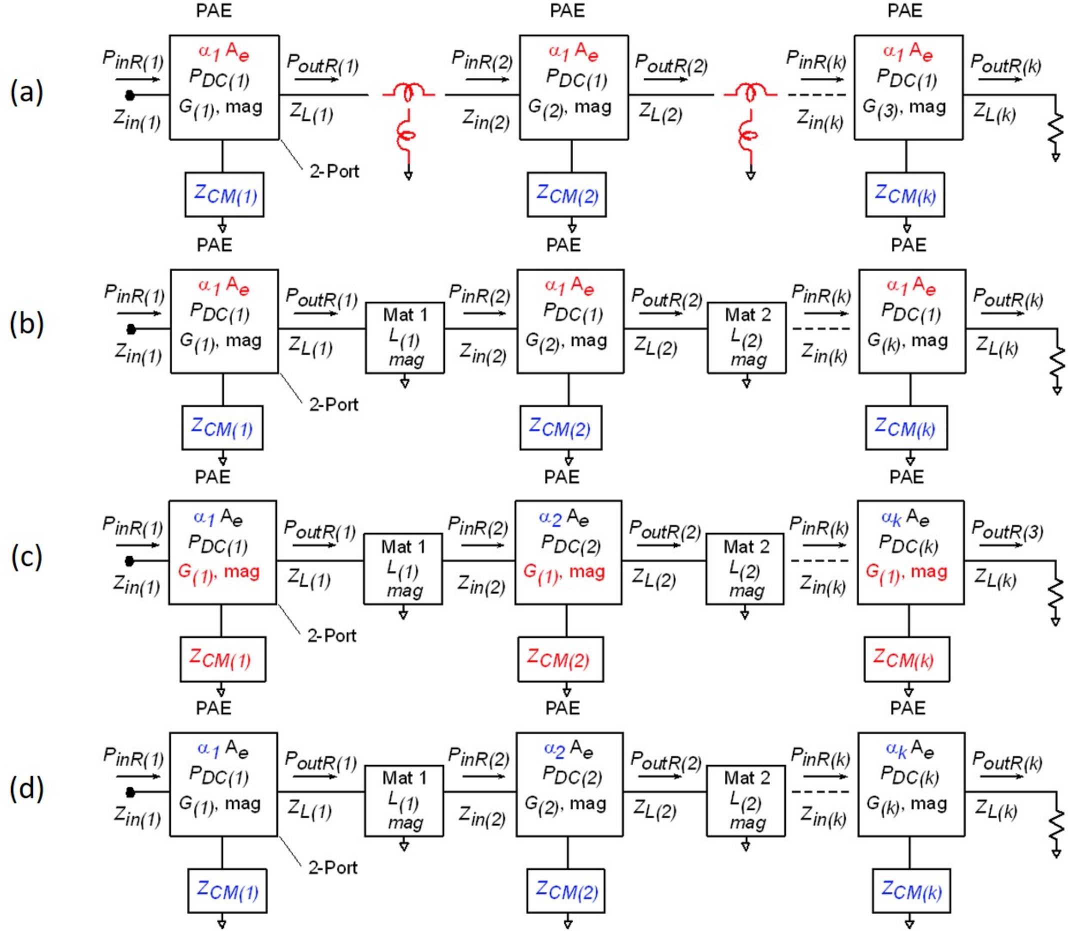


Figure 3.2: Amplifier's degrees of freedom: a) Conventional stacked amplifiers with single element matching. b) Stacked power amplifiers with full impedance matching. c) Amplifier design with area progression technique under constant normalized base impedance. d) Amplifier design with area progression and impedance scaling techniques.

impedance (αZ_{CM}), we can categorize the amplifiers techniques as follows:

1- Stacking approach: Stacking is an old technique to get higher output power [25]. Fig. 3.2a shows a conventional k CB stacked amplifier. The conventional stack is reviewed in Section 3.5.2. In stack design, all stages have the same size, given by ($\alpha_1 A_e$). α_1 is the area progression factor ($\alpha_1 = 1$), and A_e is the area of this cell. We vary the normalized common lead impedance ($\alpha_k Z_{CM(k)}$) where k is the stage index. As we

will show later in the chapter, scaling $\alpha_k Z_{CM(k)}$ yields higher output power with proper design. It also yields a different gain for each stage ($G_{(k)}$). All stages have the same bias. The conventional stack approach uses only a single element for impedance tuning and has other limitations that will be discussed. We are proposing a network theory to design stacked power amplifiers with full impedance matching (Fig. 3.2b). We still have the same stipulation that all the stages have the same area, and we vary the normalized base impedance. The design details will be presented in Section 3.5.4, showing the privilege of using the network theory approach.

2- Area progression technique: Scaling the area is an intuitive way to increase the output power. The output power (mag) is linearly proportional to the area. Note that we usually start with a cell having a certain number of fingers or total area is (A_e). Then we combine multiple of these cells, according to the area progression factor α_k, using combining techniques presented later. Fig. 3.2c shows k stages amplifier using area progression technique. In this approach (Section 3.6), we assume that all stages have the same normalized base impedance ($\alpha Z_{CM(k)}$ is constant). With proper scaling procedures, this stipulates that all stages have the same gain ($G_{(1)}$) with different DC power consumption according to the scaling factor.

3- Combined approach: In this approach, we are getting higher output power by scaling the area α_k and normalized base impedance $\alpha_k A_e$. Fig. 3.2d shows a block diagram for the general case. Each stage could have a different scaling factor α_k and different normalized base impedance (αZ_{CM} is NOT constant). This is the most complicated case to reach the optimum design for maximum PAE. Our proposed network theory provides a rigorous answer for this case in Section 3.7.

As we can see in Fig. 3.2, there are many options in power amplifier design. We can vary the area progression factor or normalized base impedance. In each approach, we can get different gain per stage, different power consumption, and different load ($Z_{L(k)}$) and input ($Z_{in(k)}$) impedances. We used the stack index k to indicate that this value is a function of the stage index, and it is indicated by a number such as ($G_{(1)}$), that means that it is independent of the stage index. The next section covers the design procedures in each approach and how to compute all the tuning network for maximum PAE. Finally, we will provide the selection criteria that lead to the highest PAE among all cases.

3.3 Key Factors for High-Efficiency Amplifiers

As we mentioned earlier, that practical amplifiers require more stages to get enough gain. Considering the general amplifier design in Fig. 3.2d, we can notice that each stage is designed to have its maximum PAE level. Our definition for the optimum design is that the total PAE for the amplifier (PAE_{tot}) equals the PAE for the individual stages.

Let's consider the following example to show the basic idea for maximum PAE design. Let's consider only two stages from the generic amplifier in Fig. 3.2d. Stage1 has a maximum output power (P_{outR1}), associated linear Gain ($G_{(1)}$) and DC power consumption (P_{DC1}). Stage1 requires certain amount of input power (P_{inR1}) to reach its maximum output power. Stage2 has a maximum power (P_{outR2}), associated Gain ($G_{(2)}$) and DC power consumption (P_{DC2}). It also requires certain amount of input power (P_{inR2}) to drive the amplifier into saturation. Both stages have the same PAE (3.1) or (3.2). We can write the total PAE assuming that Stage1 drives Stage2 in (3.3).

For lossless interstage matching circuit, the cascaded amplifiers can have the same PAE (3.3) similar to Stage1 or Stage2 only if ($P_{out1} = P_{in2}$). The stage's output power can

be optimally designed by; stacking, area progression, or both. If Stage1 is oversized and produces more output than Stage2 requires ($P_{out1} > P_{in2}$), this leads to a total PAE less than the PAE for each Stage. The latter case happens if the stage is not properly scaled or if we used the wrong value for the common lead impedance in the stack approach.

For lossy matching circuits, the output power for the first stage must satisfy the necessary input power for the second stage, including the matching loss ($P_{out1} = P_{in2}$+matching loss). This leads to PAE degradation for the system, but this is still the maximum possible PAE given this particular loss.

$$PAE(stage1) = PAE = \frac{P_{out1} - P_{in1}}{P_{DC1}} \tag{3.1}$$

$$PAE(stage2) = PAE = \frac{P_{out2} - P_{in2}}{P_{DC2}} \tag{3.2}$$

$$\begin{aligned} PAE_{tot} = \frac{P_{out2} - P_{in1}}{P_{DC1} + P_{DC2}} &= \frac{(P_{out2} - P_{in2}) + (P_{in2} - P_{in1})}{P_{DC1} + P_{DC2}} \\ &= \frac{PAEP_{DC2} + PAEP_{DC1}}{P_{DC1} + P_{DC2}} \\ = PAE \qquad & if \qquad P_{out1} = P_{in2} \\ and < PAE \qquad & if \qquad P_{out1} > P_{in2} \end{aligned} \tag{3.3}$$

3.4 Optimum Cell Selection

The first step to design any amplifier, including the stacked PA, is to evaluate the performance of different topologies. The two main typologies are CE and CB. Here we are not considering cascode as a new topology. It is just a combination of CE (CS) and CB

(CG), with no matching in between. As we mentioned in Chapter 2, power amplifiers can have poor S_{22} since there is no guarantee that optimum loadline impedance for maximum output power equals the optimum impedance for gain matching. This means that looking at the maximum available gain (MAG) curves to evaluate the cell performance is quite misleading. MAG assumes that the amplifiers are conjugate matched to achieve the highest gain, not power.

The proper way is to compare the large-signal characteristic between different topologies. Fig. 3.3 shows a large signal comparison between CE, grounded CB, and CB with base capacitance (Fig. 3.4) at 140GHz in 250nm InP HBT technology. Comparison is done for the same transistor size and biasing for the optimum loadline impedance (maximum power) for each topology. These curves show the output power, gain, and PAE versus the input power. The peak PAE is almost identical between CE and CB. The saturated output power is almost the same. The main difference is that CB shows a higher gain and hard compression characteristics compared to CE, which makes CB more favorable. In communication systems, we usually work below OP_{1dB}. This means that we should pay more attention to the performance at OP_{1dB}. This means that hard compression characteristics, where OP_{1dB} is close to the saturated power, is usually preferred. Those curves Fig. 3.3 are an example for 250nm InP HBT technology. Transistors have 4 fingers each 6um and biased at 2.5V for V_{CE} and 1.4mAμm. The OP_{1dB} for grounded base CB is 13.5dBm with 22.4% PAE and for CE is 12dBm with 15.4% PAE. It becomes clear that CB has superior performance compared to CE for this particular base termination.

The optimum load impedance is determined by the transistor size. Large transistors require smaller loadline impedance. Therefore, the transistor size should be properly cho-

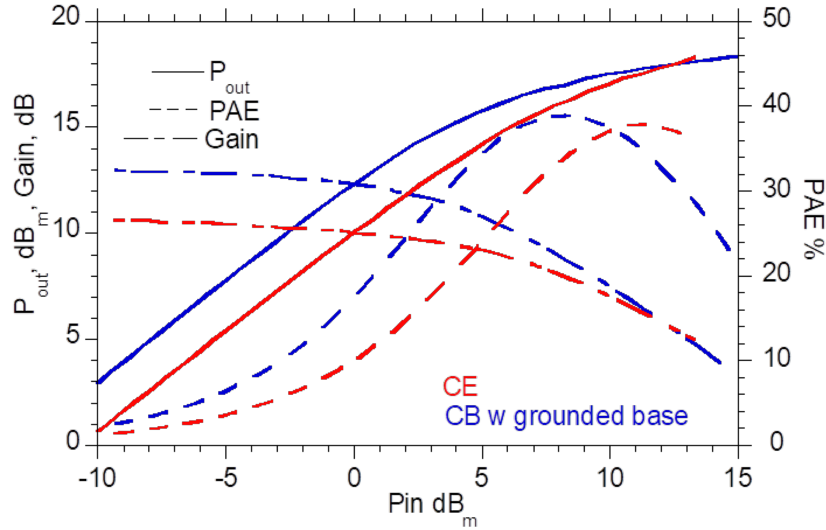


Figure 3.3: Large signal characteristic (Output power, gain, and PAE versus input power) for CE and grounded CB at 140GHz in 250nm InP HBT technology.

sen to simplify the matching circuit. For a single-cell amplifier, the transistor's loadline impedance should be close to the load impedance, which is 50Ω in many cases. And for bigger amplifiers where we combine many cells, the transistor loadline impedance should be compatible with the combining techniques. Wilkinson requires 50Ω, and generic TL combining can absorb different impedances.

A transistor footprint is another size limitation. In Teledyne HBT technology, we have discrete values for the emitter length. Shorter emitter length shows fewer parasitics, which is desired at higher frequencies. However, we need to route many fingers for a desired total emitter periphery. There is a maximum limit for the transistor fingers. Otherwise, the routing parasitic dominates the performance. There is a similar analogy for CMOS. The transistor consists of short fingers connected to each other. Transistor layouts require lots of experience. We should have good symmetry for all fingers. The distance between internal bases, collectors, and emitters to the external ones should be almost the same for all fingers. Otherwise, there will be an unbalance leading to efficiency

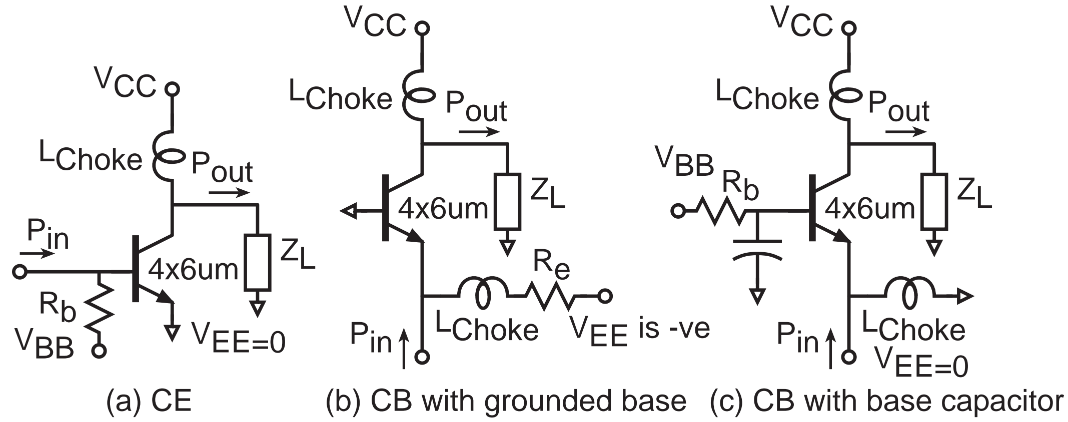


Figure 3.4: Schematic diagram of: (a) CE (b) CB with grounded base. (c) CB with 600fF base capacitor.

degradation.

Transistor biasing determines the class of operation. Each class has different characteristics. Class A is a linear amplifier with the highest gain and lowest efficiency, which is very common at mm-wave frequency. Class B has higher drain efficiency with lower gain compared to class A. There are more harmonics tuning techniques to increase the efficiency, but they are very challenging at higher frequencies.

There are different types of stability. We can check the stability factor to check the RF stability performance. It is acceptable to start with a conditionally stable amplifier, but the whole amplifier must be stable in band and out of band. There is also bias and thermal stability [27], and this is relevant for BJT design. There is an exponential relation between the collector current and base to emitter voltage (3.4). We cannot bias the transistor with a direct voltage source. The bias becomes extremely sensitive. An emitter or base resistance (R_{bias}) must be inserted to ensure stable operation and almost linear operation between the bias voltage and current (3.5). Adding the base resistance is much more efficient compared to the emitter resistance since the base current is much

lower than the emitter one, leading to better efficiency performance.

$$I_C = I_o e^{V_{BE}/V_t} \tag{3.4}$$

$$I_C = \beta \frac{V_{bias} - V_{BE}}{R_{bias}} \tag{3.5}$$

The optimum cell requires careful consideration of all the previous factors. The objective is to pick the proper combination (topology, biasing, sizing... etc.) for the maximum PAE for a desired output power and gain.

3.5 Stacked Power Amplifier

3.5.1 Stack Concept

Transistors have limited voltage swings across the device. The maximum voltage swing is defined by the breakdown voltage defined for each technology. Hence, the output power is limited for a certain number of transistor fingers. Stacking or adding transistors in series is one way to increase the total voltage swing. Each internal device cannot exceed its maximum voltage swing across the transistor terminals. However, the total voltage at the output is a series combination of the internal voltages and would be much larger than the device limit. Fig. 3.5 shows a conceptual schematic diagram for three stacked transistors in CB and CE configurations, bias is not shown for simplicity. The internal voltages are marked by red colors and they should be the same across all the transistors in the stack.

The voltage swing at node A is $V_X + V_{CM(2)}$ and $V_X + V_{CM(3)}$ at node B. As we can

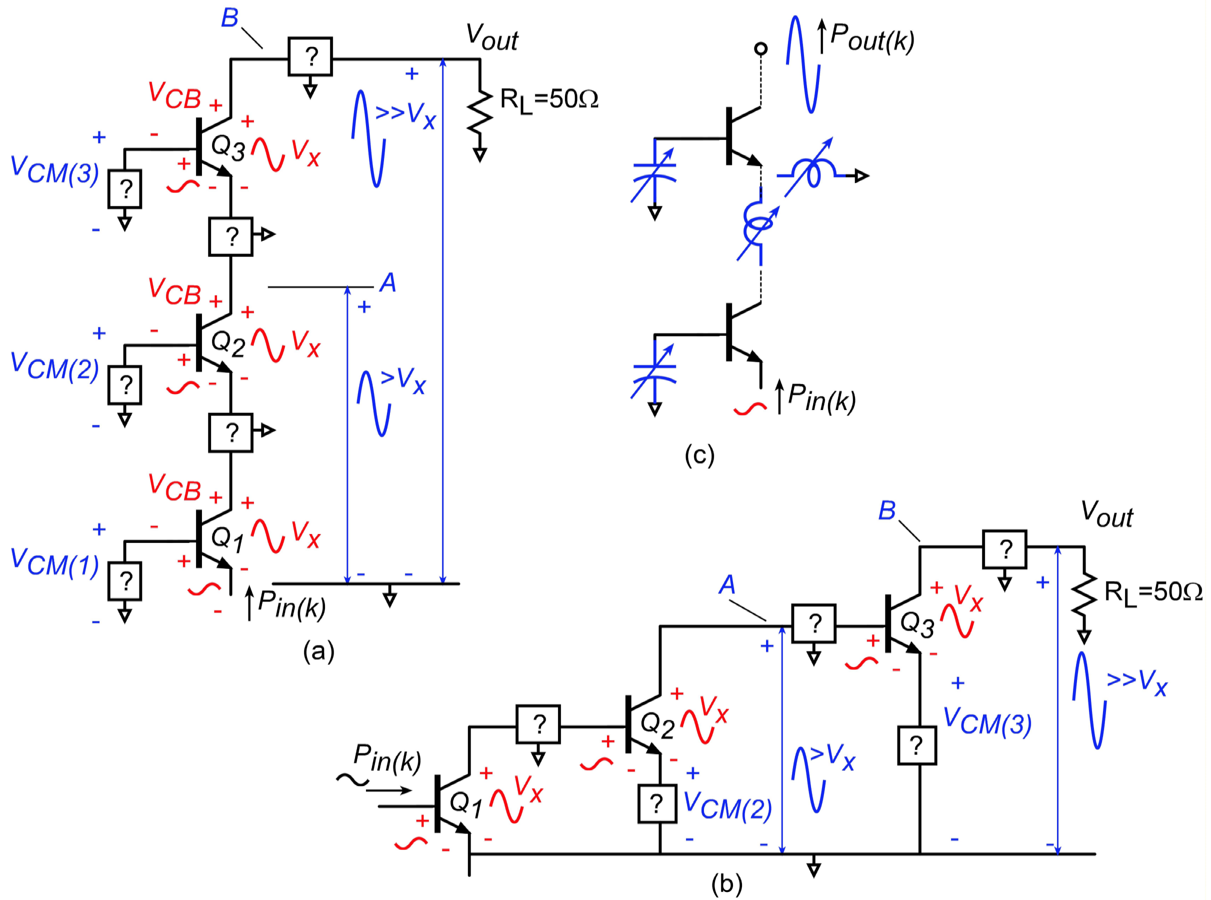


Figure 3.5: Conceptual drawing for three stacked with full impedance tuning PA; a) CB and b) CE topologies. c) Conventional stack representation for CB stack with limited tuning elements.

see, the voltages at nodes A and B can exceed the maximum voltage swing for the device given by V_X since the base/emitter impedances permits a proper voltage swing given by $V_{CM)}$. This schematic (Fig.3.5) shows lots of degrees of freedom labeled by ? and we will rigorously determine the optimum values for those elements in the chapter. The transistors must clip simultaneously to reach the proper voltage swing. This is the main stipulation for those tuning networks. If the transistors are added without proper design, destructive summation may happen, leading to lower output swing, output power, and PAE drop.

CB stack (Fig.3.5c) is widely used in the literature. Base impedances allow proper voltage swing at the transistors' bases to increase the total voltage swing (at nodes A and B) while keeping the same local voltages across the device. By analogy, we are also proposing a CE stack. Adding emitter degeneration impedances is doing a similar action compared to the base impedances in the CB stack. The degeneration elements allow voltage swing at the transistor emitters. This permits higher voltage swings without exceeding the local voltages across the devices.

3.5.2 Conventional Stack Design Procedures

Stacked power amplifiers are analyzed based on transistor models in [25]. The objective is still the same. The transistor has a limited output swing due to breakdown. More transistors should be added in series to increase the total voltage swing. The critical point in the stacked PA is to determine the optimum interstage matching and base (gate) impedance for each stage. Optimum base impedances must be presented to each transistor in the stack to hold the appropriate voltage swing (magnitude and phase), which guarantees simultaneous voltage and current clippings.

The established procedures [25] use brute force circuit techniques to determine the required base impedances and load impedance for each stage. We start the procedures by drawing the transistor circuit models then we solve KCL equations. From those equations, we can determine the required base impedance and the required load impedance for each stage. The procedures also proposed some examples for the interstage tuning. However, the interstage matching was limited (to my knowledge) to a single element tuning only (Fig. 3.5c). It was inconvenient to include full impedance matching.

3.5.3 Limitations of the Existing Approach

There are limitations to the conventional procedures. The procedures rely on transistor equivalent circuits, which are, by necessity, simple and specific transistor models. They ignore the complicated interconnect parasitics and the matching loss. Additionally, the required impedances are functions of the circuit parameters. The tuning network is usually a single element (Fig. 3.5c). Those assumptions are very challenging at mm-wave frequencies. At mm-wave frequencies, transistors models are complicated. Usually, we use EM simulators to model the transistor parasitics in terms of S-parameters files. The equivalent circuit model becomes very complex. The nodal analysis becomes very difficult, particularly with lossy matching networks. Additionally, any change in the circuit requires re-derivation of all the equations from scratch. This is inconvenient, especially if we want to examine the impact of changing the transistor models or adding any extra circuit component.

3.5.4 Network Theory for Stacked Power Amplifier: Motivation

The limitations of the conventional approach are the motivation for this two-port network theory. In the proposed two-port network theory, we design with arbitrarily complex transistor models, and arbitrarily lossy complex interconnect models at any frequency using any technology. We developed the analytic procedures to design all the tuning network with full impedance matching and determine the proper base impedance and load impedances for all transistors. We will present a graphical representation of the equations to provide more intuition during the design. Common base stacks are very common. However, we will present a common emitter stack analogy using the proposed procedures. We will focus on class A stacked PA, though the theory could be easily

extended to include more harmonics and could be used for other classes. The proposed approach provides a design framework, and the design procedures could be automated using modern CAD tools and provide optimum amplifier design.

3.5.5 Stack Design Procedure

The procedures start with modeling the transistor as a two-port network. We can use load-pull techniques to determine the optimum V&I distribution across this 2-port network for maximum PAE. Optimum selection criteria are introduced, and hence we can use the optimum topology (CB or CE). Then, we analyze the generic stack cell. The analysis shows the relation between the input, output powers, and common lead impedances. The common lead impedance refers to the base impedance in the case of CB stack design and emitter degeneration impedance in the case of CE stack design. The theory also shows the relation between the required load impedance, actual input impedance, and the common lead impedance. We determined the optimum common lead impedance values for each stage to provide the maximum PAE. Common lead impedance values define the required load impedance and actual input impedance for each stage, and hence we can design the interstage tuning network. We included a simplified loss model for the matching network to show the degradation in the efficiency. The proposed network can accommodate different neutralization techniques and shows the impact on the performance.

3.5.6 2-port Transistor Modeling

We will focus the discussion on three-terminal transistors (BJT or MOSFET) to use two-port network modeling. Some design kits provide more than three terminals, but we will ignore them for simplicity. Transistors could be modeled by the equivalent circuit

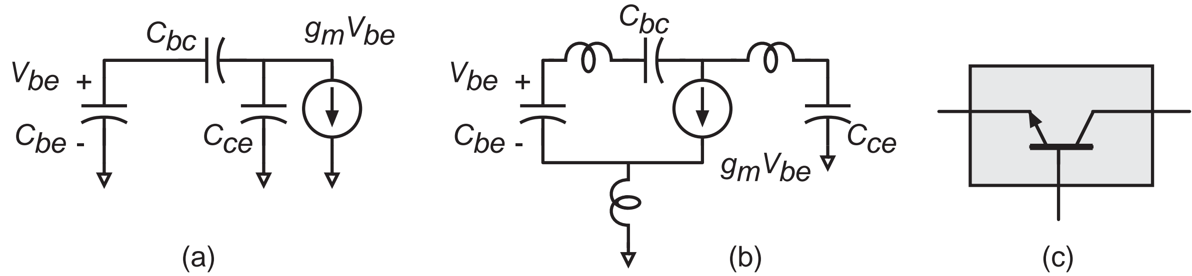


Figure 3.6: Equivalent transistor model in different representations a) Using simplified model. b) Including more parasitics. c) Using 2-port network.

models (simple model in Fig. 3.6a and including more parasitics in Fig. 3.6b). However, those models are usually simplified. Real transistor models are very complicated, especially at mm-wave frequency. Transistors have many fingers, and we usually use EM tools to model those parasitics using S-parameters files. It is not convenient to convert the S-parameters file into circuit models. Three-terminal transistors also could be modeled using a 2-port network (Fig. 3.6c). The main advantage of using a two-port network is that we no longer care about the transistor details. The 2-port involves the complicated transistor models, and we just consider the voltage across the network and current flowing into it. Using the two-port network modeling generalizes the following network theory derivation since the network could model any transistor, whether it is BJT or MOS, in any configuration (CE or CB).

3.5.7 V&I Distribution for Maximum PAE

The first step in any design is to run a few simulations, following the guides mentioned earlier, to pick the proper topology for each technology. We will consider 140GHz PA design in 250nm InP HBT Teledyne Technology as an example. But all the steps are generic and could be used for other technology or frequency. From Fig. 3.7, we found that CB shows superior performance compared to CE. So, we will use CB everywhere in the design. CB has several forms depending on the base (gate) termination. The base

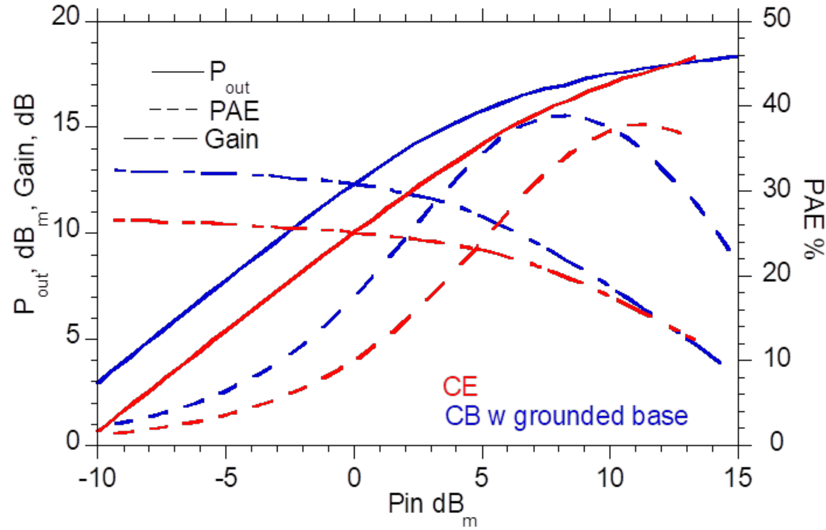


Figure 3.7: Large signal characteristic (output power, gain, and PAE versus input power) for CE and grounded CB at 140GHz in 250nm InP HBT technology.

could be shorted (grounded CB) as in Fig. 3.8b or terminated by a base impedance (Fig. 4.2c). Grounded CB requires -ve supply. For BJT transistor, the collector current is stably controlled by adding the emitter resistance, which significantly degrades the efficiency. The other approach is to add a base impedance and bias the base using base resistance. This scheme is much more efficient since the base current is much smaller than the emitter current.

The first step in our proposed procedure is to determine the optimum voltage and current distribution across the stack cells. For proper stack design, all transistors must have the same V&I distribution regardless of the base impedance value. So, we can run load pull for a grounded common base and report all the voltage across the transistor and current flowing into it. Fig. 3.9 shows the grounded CB (ADS schematic and 2-port model) with the optimum V&I for maximum PAE at 140GHz. The load impedance is optimized for the maximum saturated output power with the highest PAE. Yet the complex V&I are reported at 1dB gain compression for grounded CB.

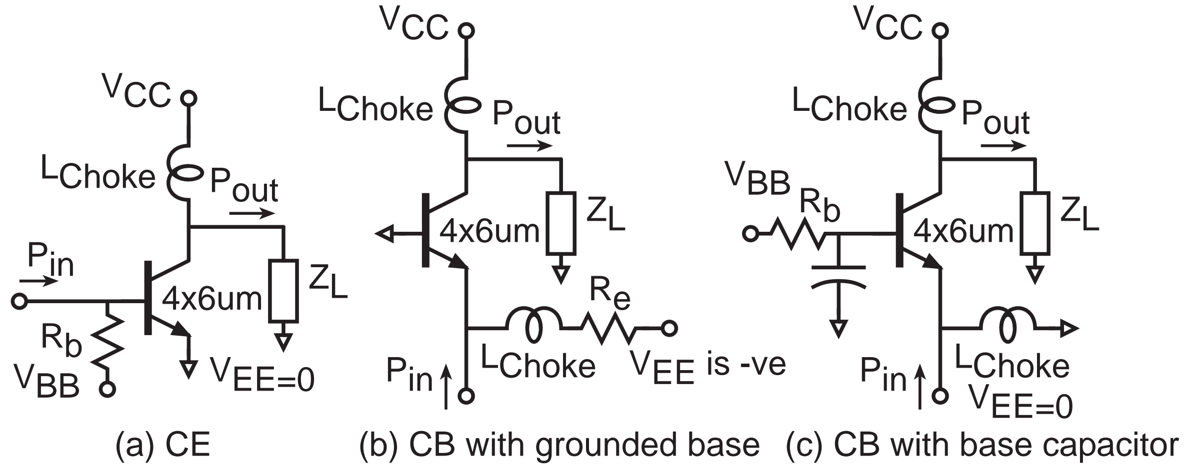
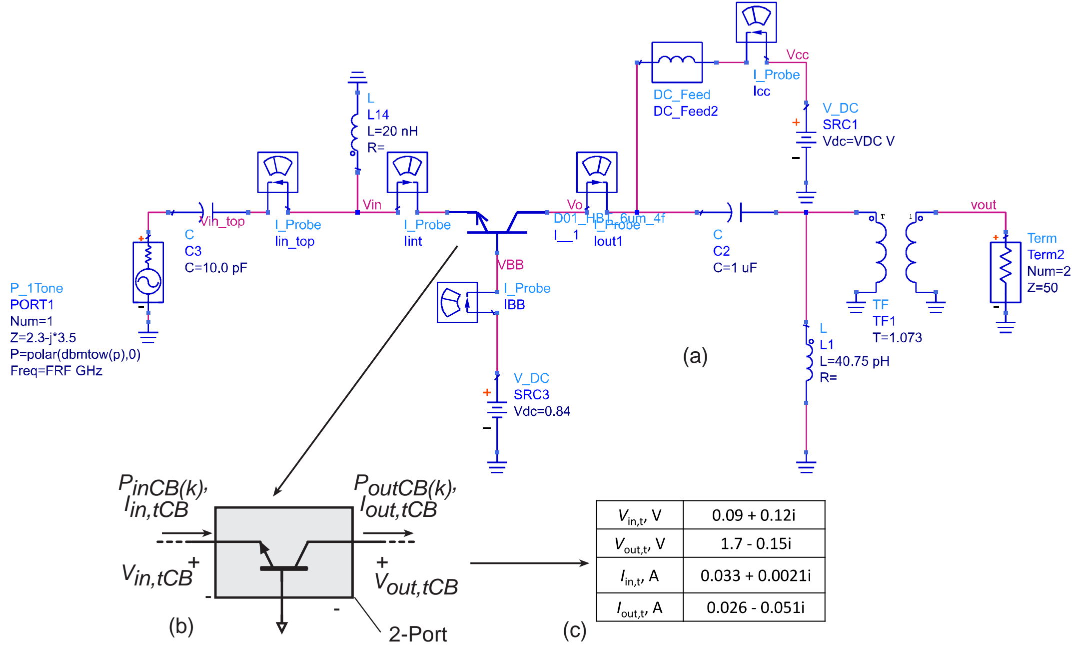


Figure 3.8: Schematic diagram of: (a) CE (b) CB with grounded base; (c) CB with 600fF base capacitor.

3.5.8 Generic Stack Cell Design

Fig. 3.10 shows the generic CB stack cell. The input power, output power, and base impedance for this generic cell depend on the stack index (k). However, the internal V&I are the same all the time for maximum PAE. These V&I patterns are already known from Fig. 3.9c. We will derive the equations for the complex input and output powers as a function of the common lead impedance ($Z_{CM(k)}$). Then we will prove, given proper design, that all cells add the same amount of power. Each stage in the stack produces a certain amount of power and requires a certain amount of input power for a given common lead impedance value. Each stage in the stack is designed to drive the next stage with the maximum PAE. We will present an easy way to determine the optimum common lead impedance values for all the stack stages to satisfy the previous stipulation. Once we get the common lead impedances, we can derive the required load impedance and actual input impedance for each cell in the stack. All the tuning networks would be rigorously defined.



$V_{in,t}$, V	0.09 + 0.12i
$V_{out,t}$, V	1.7 - 0.15i
$I_{in,t}$, A	0.033 + 0.0021i
$I_{out,t}$, A	0.026 - 0.051i

Figure 3.9: Generic CB stack cell showing the complex input, output powers, voltage and current distribution

The complex input power for cell (k) in Fig. 3.10 is written as:

$$P_{in(k)} = 0.5(V_{in,t} + Z_{CM(k)}(I_{CM}))I_{in,t}^{*} \tag{3.6}$$

From nodal equation:

$$I_{CM} = I_{in,t} - I_{out,t} \tag{3.7}$$

Then we can substitute from (3.7) in (3.6):

$$P_{in(k)} = 0.5(V_{in,t} + Z_{CM(k)}(I_{in,t} - I_{out,t}))I_{in,t}^{*} \tag{3.8}$$

The base impedance is assumed to be reactive and written as follows:

$$Z_{CM(k)} = -jX_k \tag{3.9}$$

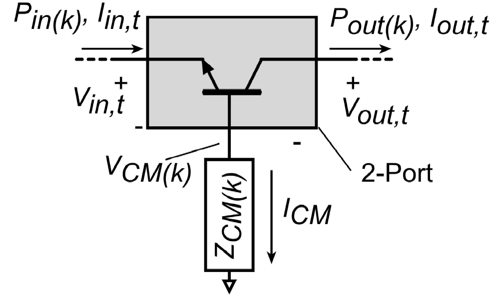


Figure 3.10: Generic CB stack cell showing the complex input, output powers, voltage and current distribution.

Then we can write the real input power as:

$$P_{inR(k)} = Re(P_{in(k)}) = 0.5|V_{in,t}||I_{in,t}|cos(\angle V_{in,t} - \angle I_{in,t}) + \\ 0.5|Z_{CM(k)}(I_{CM})I_{in,t}|cos(\angle Z_{CM(k)} + \angle I_{CM} - \angle I_{in,t}) \quad (3.10)$$

After simplification (3.11) becomes:

$$P_{inR(k)} = 0.5|V_{in,t}||I_{in,t}|cos(\angle V_{in,t} - \angle I_{in,t}) - 0.5X_k|I_{in,t}I_{out,t}|(sin(\angle I_{out,t} - \angle I_{in,t})) \quad (3.11)$$

Similarly, we can write the complex output power as

$$P_{out(k)} = 0.5(V_{out,t} + Z_{CM(k)}(I_{CM}))I^*_{out,t} \quad (3.12)$$

or

$$P_{out(k)} = 0.5(V_{out,t} + Z_{CM(k)}(I_{in,t} - I_{out,t}))I^*_{out,t} \quad (3.13)$$

The real output power could be written as:

$$P_{outR(k)} = Re(P_{out(k)}) = 0.5|V_{out,t}||I_{out,t}|cos(\angle V_{out,t} - \angle I_{out,t}) \\ -0.5X_k|I_{in,t}I_{out,t}|(sin(\angle I_{out,t} - \angle I_{in,t})) \quad (3.14)$$

Notice that the stack index shows only in the second terms in (3.11) and (3.14), and the second terms are equal. The difference between the output power and input power is given by (3.15). It is a constant value and independent of the stack index. This proves that all stages add the same amount of power, which satisfies the optimum stack design. The gain is also determined in (3.16, magnitude) and (3.17, dB).

$$PAE = \frac{P_{outR(k)} - P_{inR(k)}}{P_{DC}} = \frac{|V_{out,t}||I_{out,t}|cos(\angle V_{out,t} - \angle I_{out,t}) - |V_{in,t}||I_{in,t}|cos(\angle V_{in,t} - \angle I_{in,t})}{2P_{DC}} \tag{3.15}$$

$$Gain(k), mag = \frac{P_{outR}}{P_{inR}} = \frac{Re[(V_{out,t} + Z_{CM}(k)(I_{in,t} - I_{out,t}))I^*_{out,t}]}{Re[(V_{in,t} + Z_{CM}(k)(I_{in,t} - I_{out,t}))I^*_{in,t}]} \tag{3.16}$$

$$Gain(dB) = 10log(P_{outR(k)}) - 10log(P_{inR(k)}) \tag{3.17}$$

Equations (3.14, 3.11, 3.17) are plotted in Fig. 3.11 based on the V&I at $\mathrm{OP_{1dB}}$ in 3.9. As we decrease the base capacitance value (C_k), the base impedance increases. This allows higher voltage swing on the transistor bases leading to higher output swing and output power, which is consistent with the figure. The PAE is kept constant, even for a very small gain, since we are not adding any additional loss. We will include the loss model later. The gain decreases with smaller base capacitance. This could be justified by the feedback mechanism between C_{CB} and C_k. The feedback factor increases with smaller C_k, which decreases the gain. It also worth mentioning that Fig. 3.11 shows only the compressed gain and does not show the degree of compression. Although we reported the V&I at $\mathrm{OP_{1dB}}$. The gain compression value (1dB) is valid only at $C_k = \infty$ or

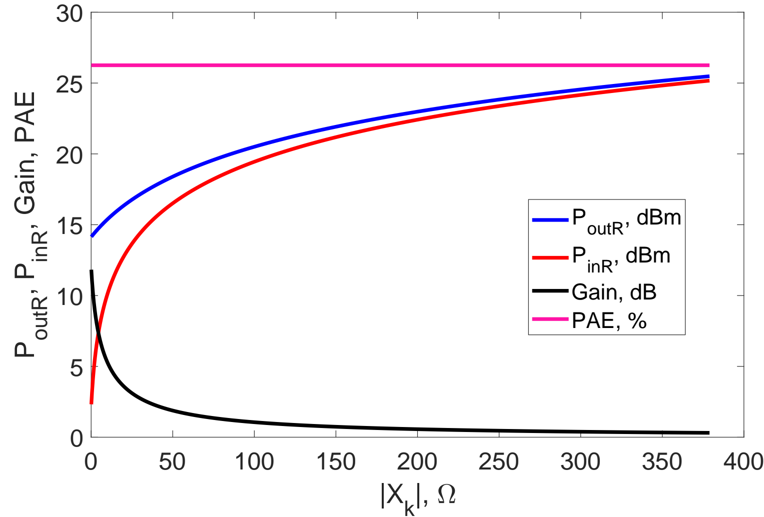


Figure 3.11: Real output power, input power, PAE, and Gain, versus the base reactance.

$(X_k = 0)$ where we first recorded those values. However, as we decrease C_k, the feedback linearizes the stage showing a lower level of compression.

We can plot the gain equation (3.17) using the V&I at very low output power. The resulting gain would be the uncompressed gain. Fig. 3.12a shows the linear gain and the compressed gain. The compression level is shown in Fig. 3.12b. As we decrease the base capacitance, the base impedance increases. The compression level is getting smaller, which means that the cell becomes more linear.

3.5.9 Stacked Stages for Maximum PAE

Our objective is to design the stacked stages for the maximum possible PAE. We considered an example to show the basic idea to get the highest PAE for the cascaded system in Section 3.3. The cascaded amplifiers can have the same PAE similar to the individual stages only if each stage delivers the necessary input power for the following stage. i.e. $(P_{out1} = P_{in2}, P_{out2} = P_{in3}...$ etc. $)$. If we oversized the stage and produced

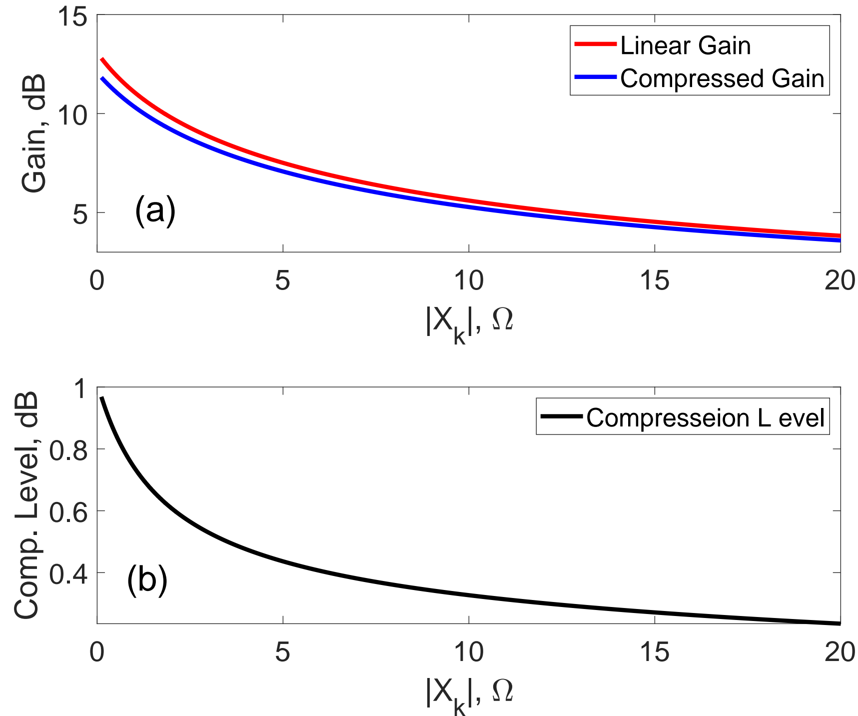


Figure 3.12: a) Compressed Gain, Linear Gain versus the base reactance b) Compression level versus the base reactance

more output than the following stage requires ($P_{out1} > P_{in2}, P_{out2} > P_{in3}$, ... etc.), this leads to a total PAE less than the PAE for each Stage.

Moving to the stack design and let's revisit Fig. 3.11. Fig. 3.13a shows the relation between the input, output powers, gain, and PAE as a function of the base capacitance. The available input source power defines the base impedance location of the first stage. In this example (Fig. 3.13), we assume the first stage has 600fF base capacitance, and the input source power is sufficient to drive this cell.

Once we define the 1st stage, the following stages are very well defined (Fig. 3.13a). The output power of the 1st stage must equal the input power of the 2nd stage to reach the max PAE. This will define the required base reactance (X_2 or $Z_{CM(2)}$) for the second

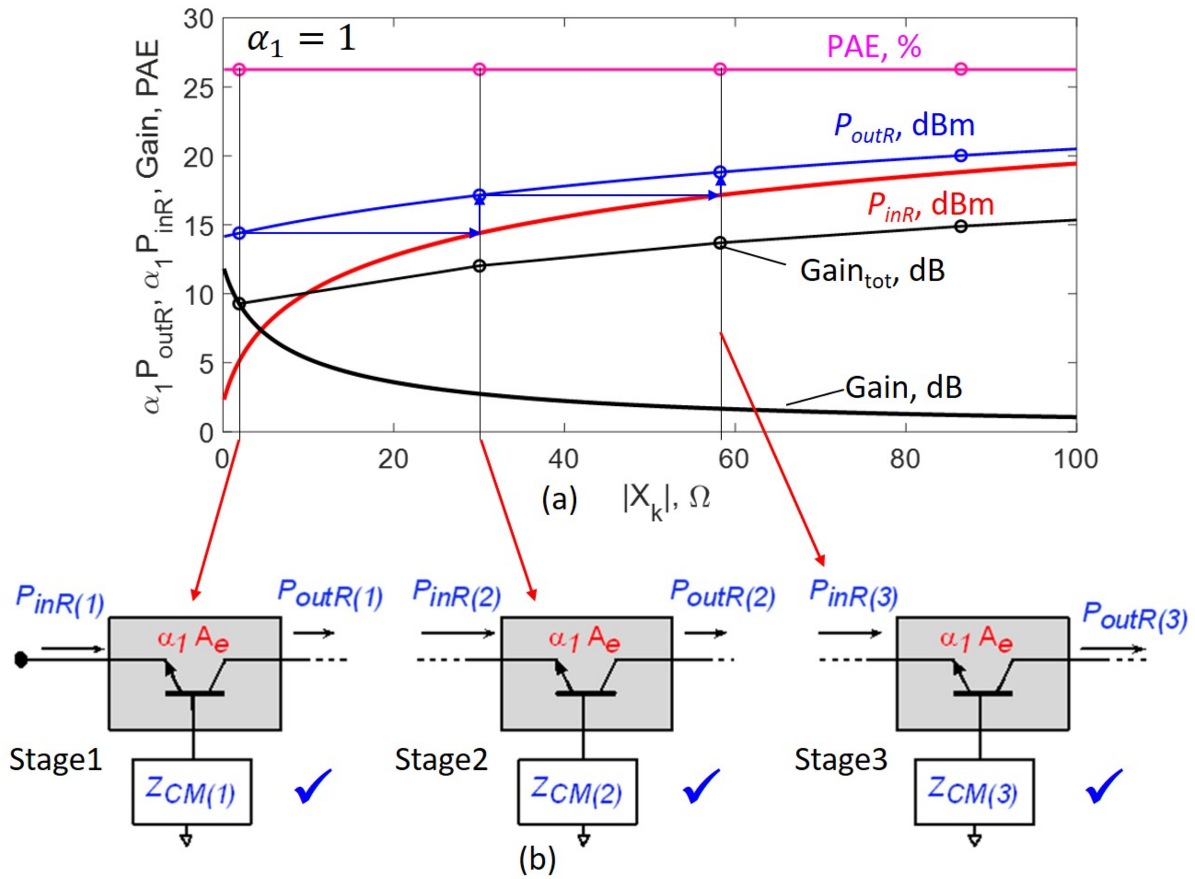


Figure 3.13: a) Real output power, input power, PAE, gain, and total gain versus the base reactance showing the optimum stack stage location using lossless matching network b) Block diagram for the amplifier.

stage. Here we are ignoring the matching loss. The second stage produces higher output power (P_{out2}) and has a lower gain with the same PAE. Similarly, we can design the 3rd stage. The output power from the 2nd stage must equal the input power for the 3rd stage and hence we defined the required base reactance for the 3rd stage (X_3 or $Z_{CM(3)}$) and so on. We can keep adding more stages to get higher output power and increase the gain. For three-stack design (Fig. 3.13b), the output power would be the output power of the 3rd stage (P_{out3}) and the input power is the input power of the 1st cell (P_{in1}). The total gain is the summation of three stages' gain. The general gain equation for kth stage is

(3.18). We can also define the PAE for kth stage stack in (3.30).

This is the equation for the total gain at kth stage:

$$Gain_{tot}(k), dB = \sum_{m=1}^{k} Gain(m), dB \tag{3.18}$$

Where m is a temporary index and k is the stack index =1, 2... Similarly, we can get the accumulated PAE for kth stage as follows:

$$PAE = \frac{P_{outR(k)} - P_{inR(1)}}{kP_{DC}} \tag{3.19}$$

From the previous steps, we computed the base reactance ($Z_{CM(k)}$) for each stage. We computed the load impedance ($Z_{L(k)}$) and actual input impedance ($Z_{in(k)}$) as a function of the stack index k and base impedance ($Z_{CM(k)}$), and internal voltages and current according to (3.20, 3.21). The load and input impedance are plotted in the smith chart (Fig. 3.15a) using the previous 140GHz CB example numbers. The chart highlights the location of the input and load impedance for each stage (Fig. 3.15b). This is precisely defined since the base impedances are previously determined, and the chart shows the impedances ($Z_{L(k)}$ and $Z_{in(k)}$) versus the base impedance ($Z_{CM(k)}$).

This is the load impedance ($Z_{L(k)}$)

$$Z_{L(k)} = \frac{V_{out,t} + Z_{CM(k)}(I_{in,t} - I_{out,t})}{I_{out,t}} \tag{3.20}$$

Similarly, this is the actual input impedance ($Z_{in(k)}$)

$$Z_{in(k)} = \frac{V_{in,t} + Z_{CM(k)}(I_{in,t} - I_{out,t})}{I_{in,t}} \tag{3.21}$$

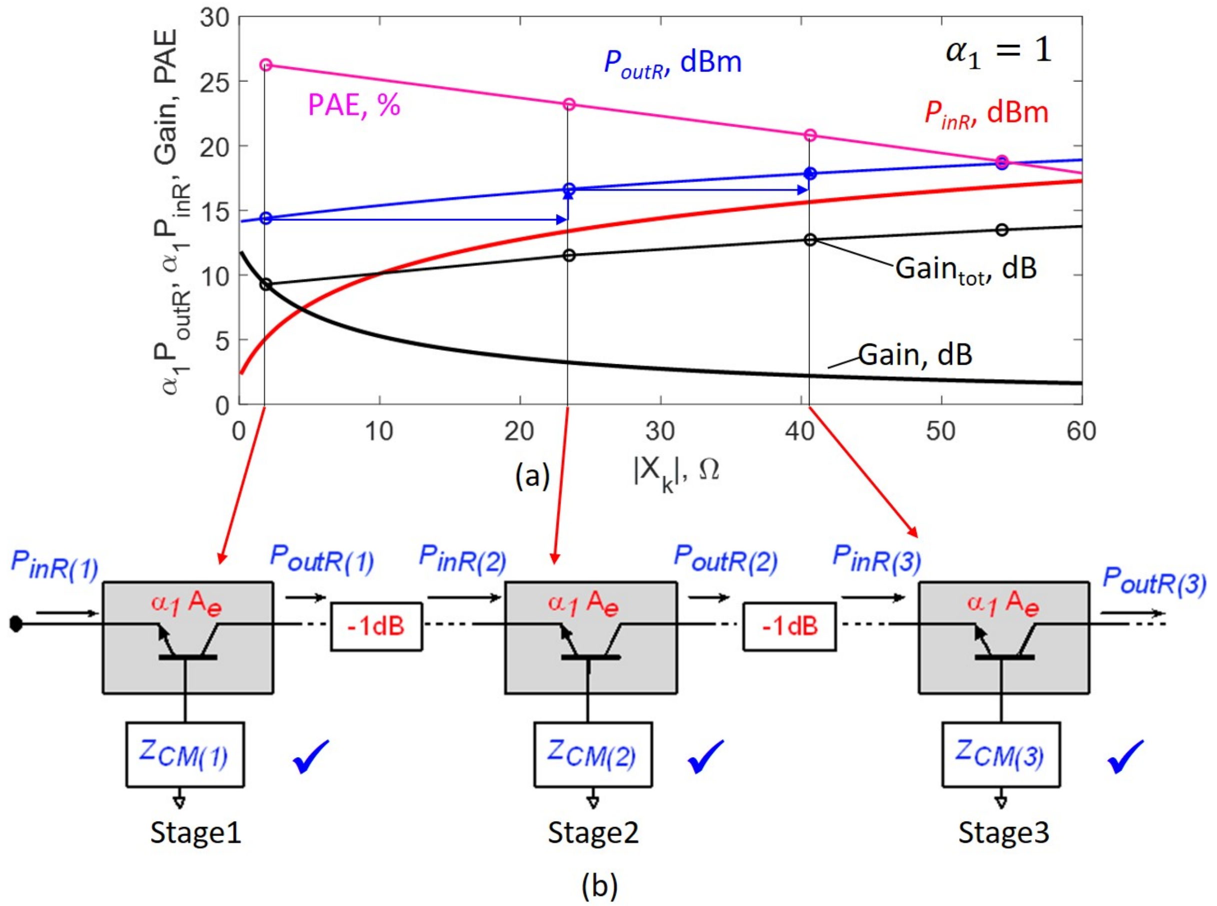


Figure 3.14: a) Real output power, input power, ideal PAE, PAE including loss , gain, and total gain versus the base reactance showing the optimum stack stage location using lossy matching network (1dB per each interstage matching). b) Block diagram for the amplifier.

3.5.10 Example: Three CB Stacked PA

We will show an ADS example to verify the previous procedures. Let's consider designing three CB stages at 140GHz in 250nm InP HBT technology.

1. We run a load-pull simulation for a unit cell with a given area A_e biased at class A. Then we compute the voltages and current complex quantities at 140GHz at a given compression level (for example 1dB). This step is already done in Fig. 3.9.

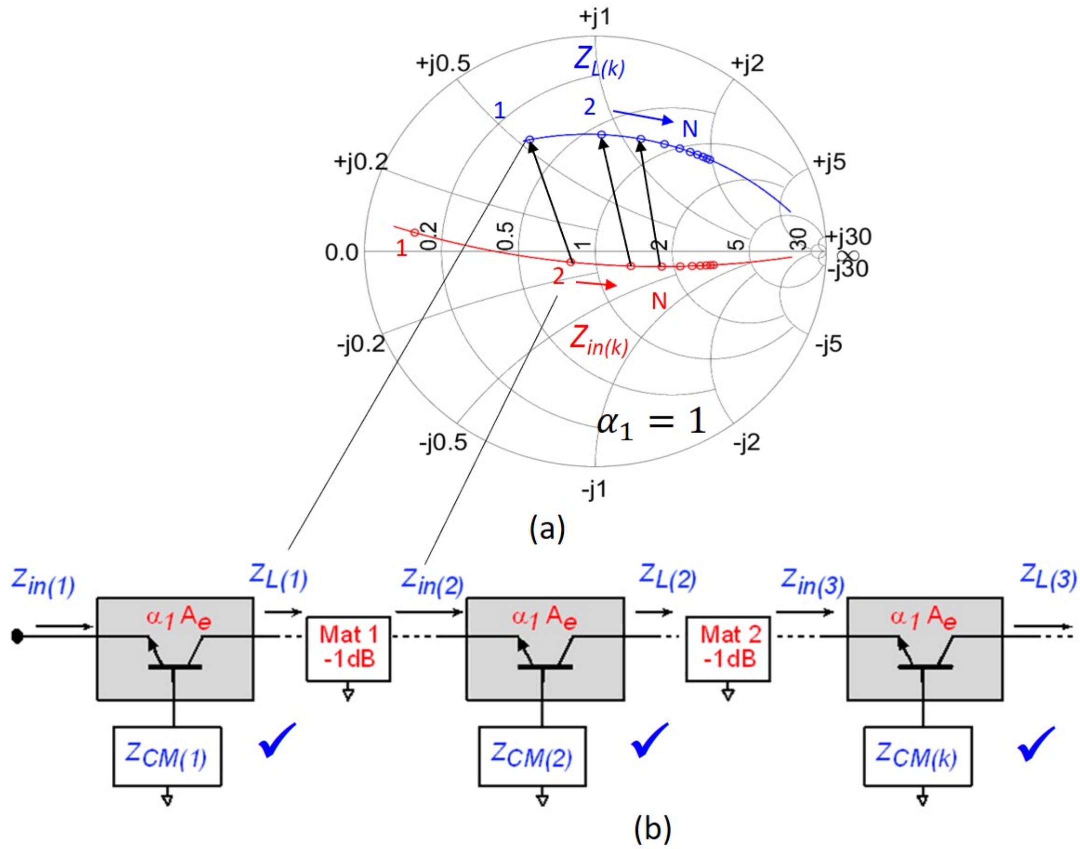


Figure 3.15: a) Required load impedance and actual input impedance contours versus the stack index. The black arrows show the required interstage impedance transformation in lossy network (1dB per each interstage matching) b) Block diagram for the amplifier.

2. We generate the design contours given a certain matching loss. In this example, we assume that we have 1dB loss for each interstage tuning network (we can certainly accommodate different loss models in our procedures). We also generated those contours before in Fig. 3.14

3. We assume that the input power is enough to drive the first stage with the appropriate base reactance. Then we follow the contours (Fig. 3.14) to determine the base impedances for all three stages ($Z_{CM(1)}, Z_{CM(2)}, Z_{CM(3)}$)

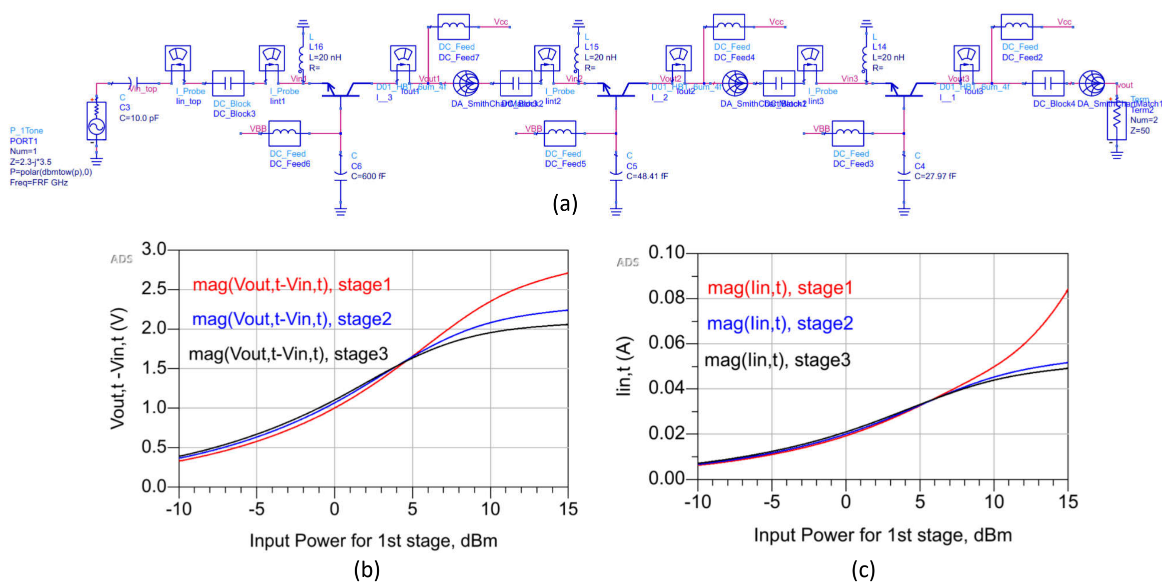


Figure 3.16: CB example: a) schematic diagram of three CB stacked amplifier. b) Magnitudes of the internal voltages ($V_{out,t} - V_{in,t}$) versus the input power for the first stage c) Magnitudes of the internal currents (I_{int}) versus the input power for the first stage

4. We use the impedance chart in Fig. 3.15 to determine the load and input impedance of each stage. Then We use ADS smith matching component to achieve the required transformation assuming 1dB matching loss for each interstage matching network. Then everything is determined in the stack.

To verify that the stack is working properly, we plotted the internal voltages (Fig. 3.16b) and internal current (Fig. 3.16c) for the three stages. According to our first stipulation, all the internal voltages and currents must align to ensure simultaneously clipping and achieve the maximum PAE. We can see that the voltages and currents are matching pretty well up to a certain power level, then begin slightly to deviate. Power amplifiers deal with large signals which drive them in the nonlinear regime. This implicates that all impedances are functions of the input power. We applied our network theory at a particular power level, where there is a perfect agreement. However, as

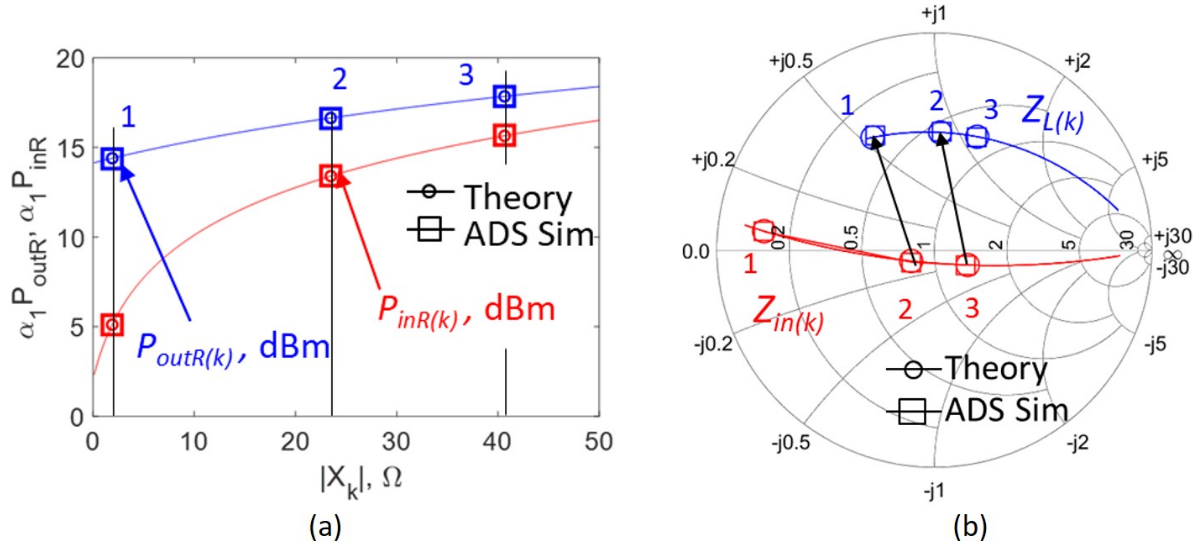


Figure 3.17: CB example: a) Simulated and theoretical stages power are in perfect agreement. b) Simulated and theoretical stages impedances are in perfect agreement.

the power changes, the load and input impedances also change, which demand different matching transformation. So, this discrepancy is coming from the matching limitation since we are using linear matching. We might fix this discrepancy, at least theoretically, if we used nonlinear matching elements.

We also monitored the input and output power for each stage. Fig. 3.17a shows a great agreement between the simulated and theoretically predicted input and output powers for each stage. Similarly, we simulated the input and load impedance for each stage. Fig. 3.17b shows a great agreement between the theory and simulation. Note that in the stack, we do not scale the area, so $\alpha_1 = 1$ in all stack figures.

3.5.11 CE Stack Procedures

We are also proposing a CE stack that could be designed by the network theory. One of the advantages of using network theory is that we do not have to repeat the

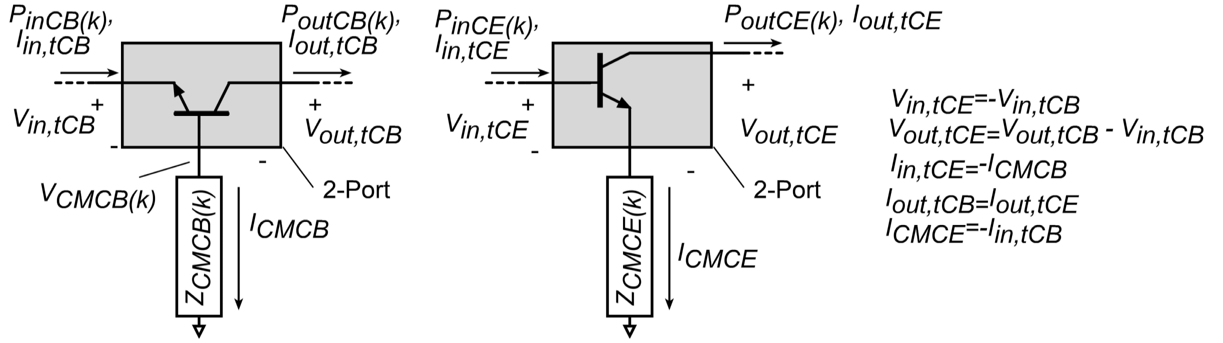


Figure 3.18: Analogy between CB and CE.

derivation. Fig. 3.18 shows the general cell of the CB stack compared to the CE stack cell. We can use the same equations that we derived earlier for the CB case since all the derived equations are functions of the voltage and current distributions and are independent of the circuit details. The other interesting point is that we do not even have to compute the voltage and current distribution for the CE case. We can just map the voltage and current distribution from CB to CE using the equations given in Fig. 3.18. We also proved that the voltages and currents pattern in CB or CE (after using the transformation equations) yields the same PAE. We mapped the voltages and currents from CB to CE then substituted in equations (3.23, and 3.25). Equations 3.26 and 3.27 show that both CB and CE have the same added power.

$$P_{inCER(k)} = 0.5(V_{in,tCE} + Z_{CMCE(k)}(I_{in,tCE} - I_{out,tCE}))I^*_{in,tCE} \tag{3.22}$$

$$P_{inCER(k)} = 0.5(-V_{in,tCB} + Z_{CMCE(k)}(-I_{CMCB} - I_{out,tCB}))(-I^*_{CMCB}) \tag{3.23}$$

Similarly, we can write the complex output power as

$$P_{outRCE(k)} = 0.5(V_{outCE,t} + Z_{CMCE(k)}(I_{CMCE}))I^*_{out,tCE} \tag{3.24}$$

$$P_{outRCE(k)} = 0.5(V_{outCB,t} - V_{inCB,t} + Z_{CMCE(k)}(-I_{in,tCB}))I^*_{out,tCB} \quad (3.25)$$

Then

$$P_{outRCE(k)} - P_{inCE(k)} = 0.5(V_{outCB,t}I^*_{out,tCB} - V_{inCB,t}I^*_{in,tCB} - Z_{CMCE(k)}|I_{in,tCB}|^2) \quad (3.26)$$

We can ignore the reactance power

$$P_{outRCE(k)} - P_{inCE(k)} = P_{outCB(k)} - P_{inCB(k)} \quad (3.27)$$

3.5.12 CE Stack Design Procedure

The CE stack design procedures are similar to the CB one except that the common lead impedance becomes inductor degeneration compared to base impedance in the CB stack. In CE stack, we start with plotting the output power (P_{outR}), input power (P_{inR}), Gain, PAE versus the emitter degeneration reactance ($X_k = \omega L$, where L is the emitter inductance) as shown in Fig. 3.19. We can use an analogy between CB and CE stack concepts. As the emitter reactance increases, we get higher output power, lower gain for the same PAE.

We also computed and plotted the compressed gain and linear gain (computed at very low input power level) in (Fig. 3.20a). The compression level is shown in Fig. 3.20b. As we increase the emitter inductance value, the transistor becomes more linear. This result is consistent with the widely known CE linearization techniques. We will show a CE example in the next section.

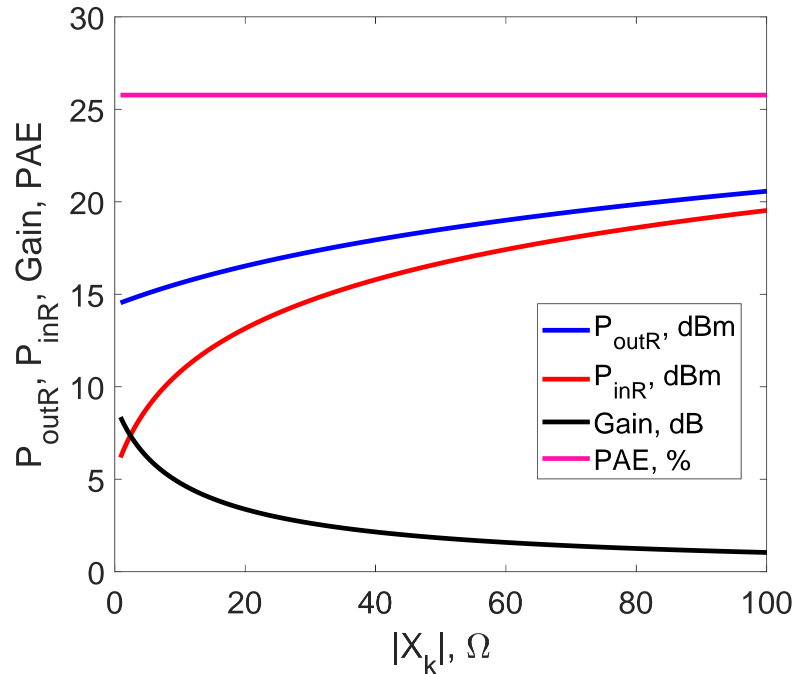


Figure 3.19: Real output power, input power, PAE, and Gain versus the emitter reactance for CE stack.

3.5.13 Example: Three CE Stacked PA

In this example, we design a three CE stack by network theory at 140GHz in 250nm InP HBT technology. The design procedures are similar to the CB one.

1. We run a load-pull simulation for a unit cell with a given area A_e biased at class A. Then we computed the voltages and current complex quantities at 140GHz at a given compression level (for example 1dB). In fact, we did not have to rerun the simulation. We used the same voltages and currents in the CB case and used the equations in Fig. 3.18 to get the proper values for CE.

2. We generate the design contours given a certain matching loss. In this example, we assume that we have 1dB loss for each interstage tuning network. We also generated those contours in Fig. 3.21b. The figure highlights the proper value for

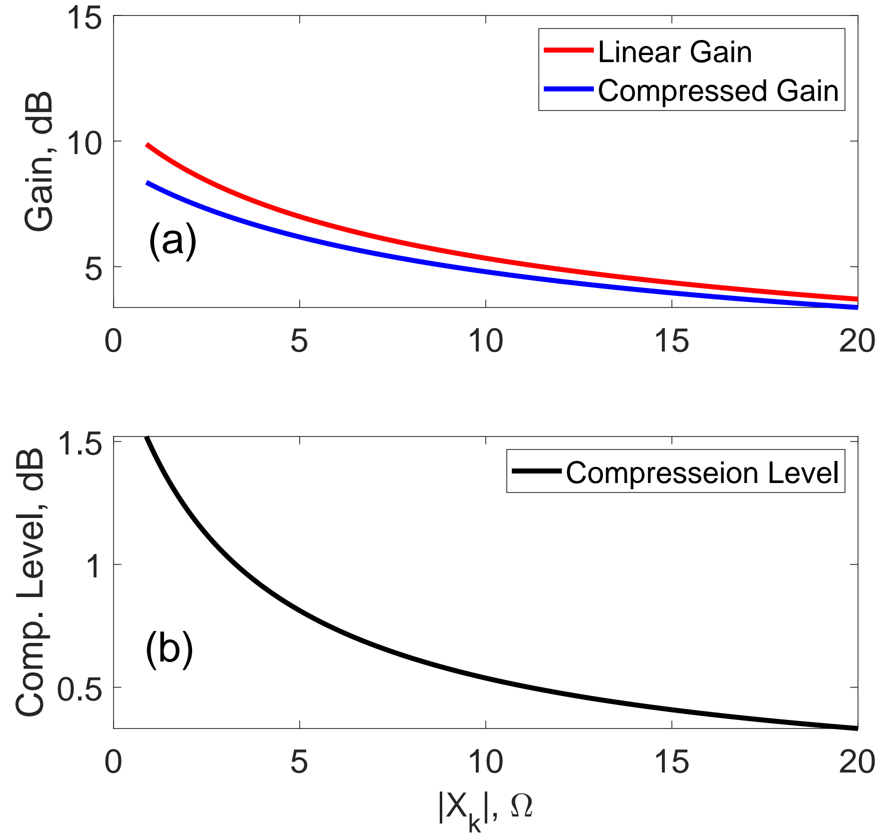


Figure 3.20: a) Compressed Gain, linear gain versus the emitter reactance b) Compression level versus the emitter reactance

the emitter reactance value. We assumed that the input power enough to drive the first stage with $\sim 0\Omega$ emitter reactance. Then we computed emitter impedances for all three stages $(Z_{CM(1)}, Z_{CM(2)}, Z_{CM(3)})$

3. We used the impedance chart in Fig. 3.21c to determine the load and input impedance of each stage. Then We used ADS smith matching component to achieve the required transformation assuming 1dB matching loss for each interstage matching network. Then everything is determined in the stack.

To verify that the stack is working properly, we plotted the internal voltages (Fig. 3.22a) and internal current (Fig. 3.22b) for the three stages. According to our first stipu-

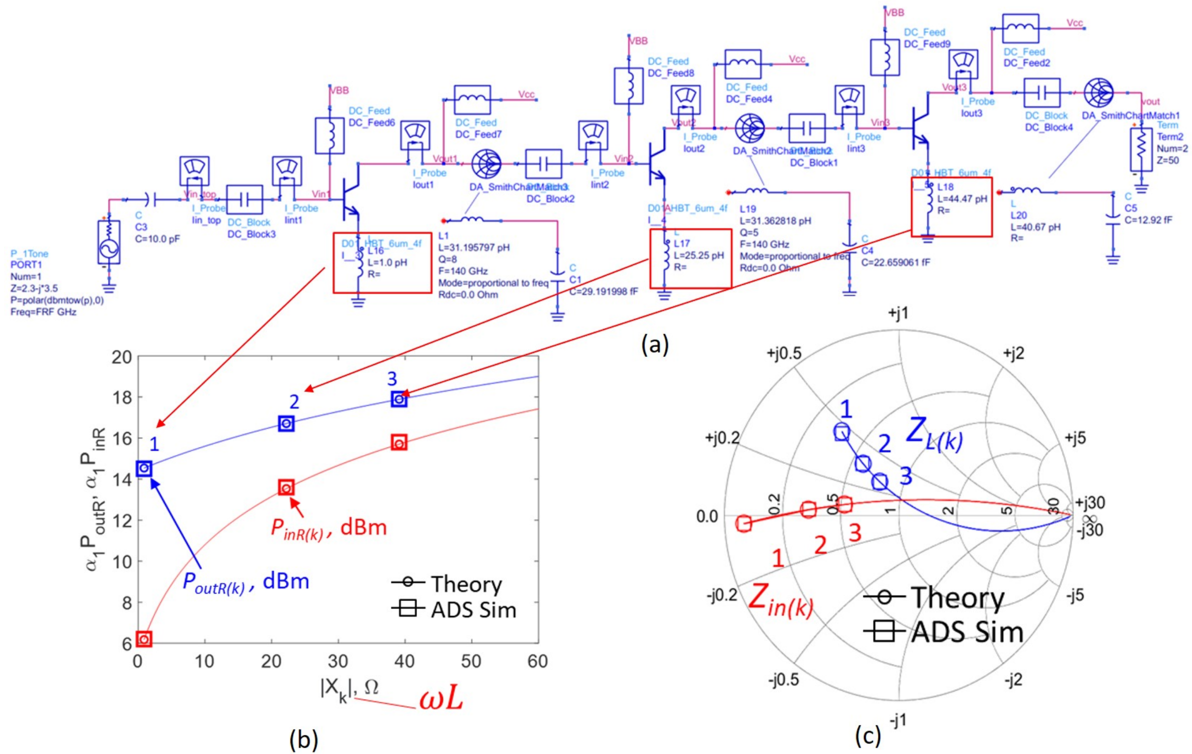


Figure 3.21: CE example: a) Schematic diagram of three CE stacked amplifier. b) Simulated and theoretical stages power showing the location of the proper emitter reactance. c) Simulated and theoretical stages impedances highlighted at the location of the proper emitter reactance value

lation, all the internal voltages and currents must align to ensure simultaneously clipping and achieve the maximum PAE. We also monitored the input and output power for each stage. Fig. 3.21b shows a great agreement between the simulated and theoretically predicted input and output powers for each stage. Similarly, we simulated the input and load impedance for each stage. Fig. 3.21c shows a great agreement between the theory and simulation. Note that in the stack, we do not scale the area, so $\alpha_1 = 1$ in all stack figures.

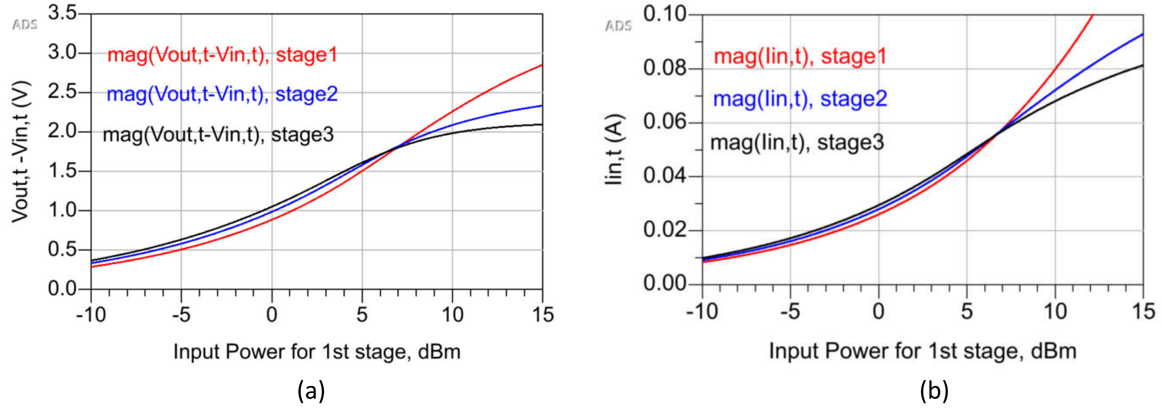


Figure 3.22: CE example: a) Magnitudes of the internal voltages ($V_{out,t} - V_{in,t}$) versus the input power for the first stage b) Magnitudes of the internal currents (I_{int}) versus the input power for the first stage

3.5.14 Example: Neutralization Impact

Using network theory allows us to add more circuit components without re-deriving the design equations from scratch. A clear example of that is the neutralization techniques. In neutralization techniques, we may add feedback elements (Z_{fo}), or (Z_f). We can also add a feedforward element (Z_{fi}). Those techniques are usually used to increase the gain. We will analyze the impact of those components in the vicinity of the stack design. Fig. 3.23a shows the original stack cell, including the different neutralization elements. To use the same design stack equation without re-derivation, we will create a modified two-port network. The transformation equations are shown in Fig. 3.23b. Those equations are derived such that the internal voltages and currents are kept the same as the original stack without neutralization while including the new current contribution from the added elements. So, we created a modified 2-port network that we can use with our old equations.

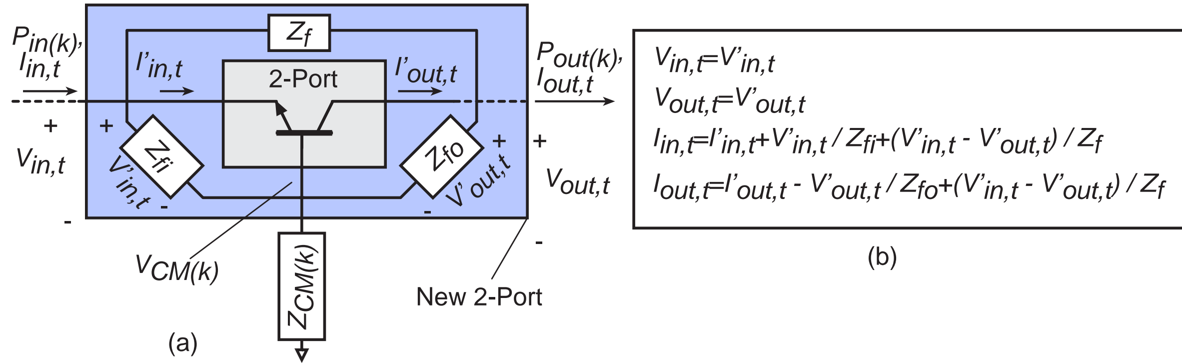


Figure 3.23: General form of neutralization.

To show the impact of the neutralization, we added an ideal -ve C_{CB}=-20f for two cases: 1) assuming that all matching circuits are lossless. Fig. 3.24 shows the output power, gain, and PAE versus the normalized base impedance using the number from the previous example. The neutralization changed the location of the base reactance value with the same PAE. We repeated the same test in Fig. 3.25 assuming 1dB loss per interstage matching. We found that the neutralization increases the PAE in this case. We also can use the same equation to give intuition regarding the impact of the neutralization even if we did not use the stack. For the same base impedance, we can see that the neutralization improves the PAE for a lossy network. This justifies the extensive use of neutralization techniques in mm-wave circuits designed in CMOS technology since the gain is very low and comparable to the matching loss.

3.5.15 General Form of the Equations

We derived all the previous equations assuming a single tune. This is a good approximation since we were focusing on class A power amplifier design, which is already a linear amplifier. We can extend the previous equations and include more harmonics as shown in equations (3.28, 3.29, 3.30, 3.31, 3.32, 3.33, 3.35, and 3.36). Those equations might be a starting point to use the network theory to design amplifiers at different classes such

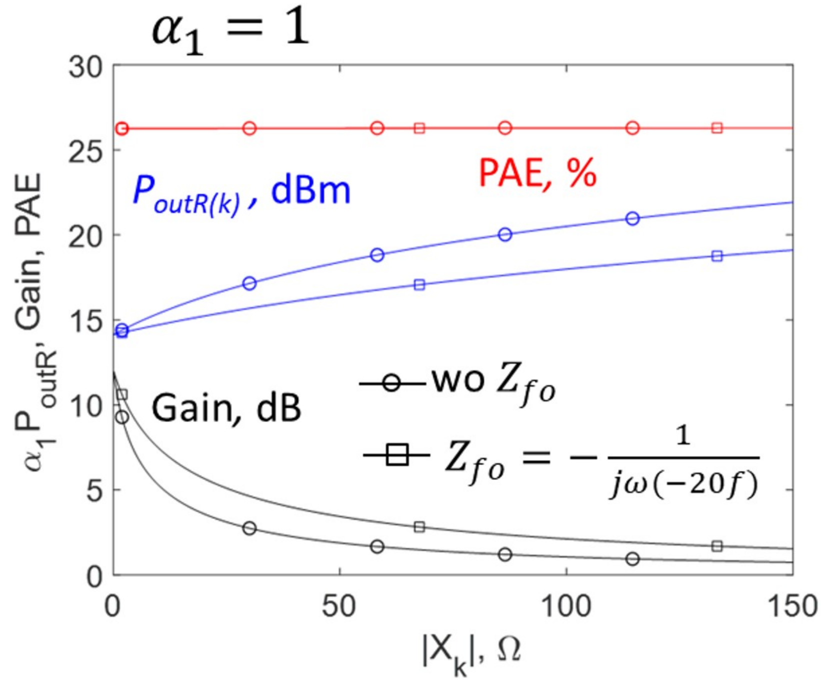


Figure 3.24: Pout, gain, PAE with 20fF C_{CB} neutralization for lossless matching.

as B, C... etc.

We can include all harmonics. The input real power would be:

$$P_{inR(k)}(\omega_o, 2\omega_o, ...) = 0.5|V_{in,t}(\omega_o, 2\omega_o, ...)||I_{in,t}(\omega_o, 2\omega_o, ...)|cos(\angle V_{in,t}(\omega_o, 2\omega_o, ...) - \angle I_{in,t}(\omega_o, 2\omega_o, ...)) - 0.5X_k(\omega_o, 2\omega_o, ...)|I_{in,t}(\omega_o, 2\omega_o, ...)I_{out,t}(\omega_o, 2\omega_o, ...)| (sin(\angle I_{out,t}(\omega_o, 2\omega_o, ...) - \angle I_{in,t}(\omega_o, 2\omega_o, ...)) \quad (3.28)$$

$$P_{outR(k)}(\omega_o, 2\omega_o, ...) = 0.5|V_{out,t}(\omega_o, 2\omega_o, ...)||I_{out,t}(\omega_o, 2\omega_o, ...)|cos(\angle V_{out,t}(\omega_o, 2\omega_o, ...) - \angle I_{out,t}(\omega_o, 2\omega_o, ...)) - 0.5X_k|I_{in,t}(\omega_o, 2\omega_o, ...)I_{out,t}(\omega_o, 2\omega_o, ...)| (sin(\angle I_{out,t}(\omega_o, 2\omega_o, ...) - \angle I_{in,t}(\omega_o, 2\omega_o, ...))) \quad (3.29)$$

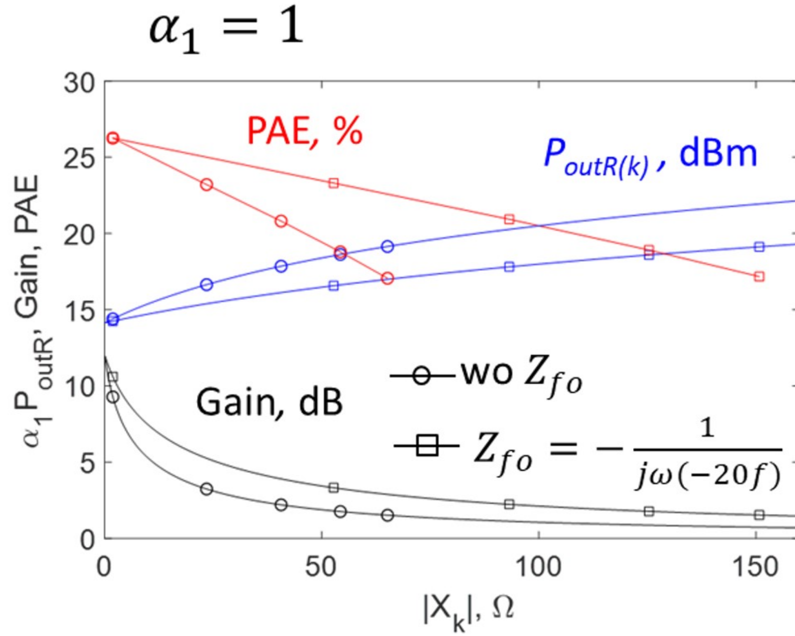


Figure 3.25: P_{outR}, gain, PAE with 20fF C_{CB} neutralization for lossy matching.

The general form of PAE becomes:

$$PAE(\omega_o, 2\omega_o, ...) = \frac{P_{outR(k)}(\omega_o, 2\omega_o, ...) - P_{inR(k)}(\omega_o, 2\omega_o, ...)}{P_{DC}} \tag{3.30}$$

The base impedance will be:

$$X_k(\omega_o, 2\omega_o, ...) = [|V_{in,t}(\omega_o, 2\omega_o, ...)||I_{in,t}(\omega_o, 2\omega_o, ...)|cos(\angle V_{in,t}(\omega_o, 2\omega_o, ...) - \angle I_{in,t}(\omega_o, 2\omega_o, ...)) - 2P_{inR(k)}(\omega_o, 2\omega_o, ...)]/[sin(\angle I_{out,t}(\omega_o, 2\omega_o, ...) - \angle I^*_{in,t}(\omega_o, 2\omega_o, ...))] \tag{3.31}$$

The gain of the generic cell

$$Gain_k(\omega_o, 2\omega_o, ...), mag = \frac{P_{outR}(\omega_o, 2\omega_o, ...)}{P_{inR}(\omega_o, 2\omega_o, ...)} \tag{3.32}$$

$$Gain(k), dB = 10log(P_{outR}(\omega_o, 2\omega_o, ...)) - 10log(P_{inR}(\omega_o, 2\omega_o, ...)) \tag{3.33}$$

$$Gain_{tot}(k), dB = \sum_{m=1}^{k} Gain_m(\omega_o, 2\omega_o, ...), dB \tag{3.34}$$

This is the load impedance ($Z_{L(k)}$) in generic form:

$$Z_{L(k)}(\omega_o, 2\omega_o, ...) = \frac{V_{out,t}(\omega_o, 2\omega_o, ...) + Z_{CM(k)}(\omega_o, 2\omega_o, ...)(I_{in,t}(\omega_o, 2\omega_o, ...) - I_{out,t}(\omega_o, 2\omega_o, ...))}{I_{out,t}(\omega_o, 2\omega_o, ...)} \tag{3.35}$$

Similarly, this is the actual input impedance ($Z_{in(k)}$) in generic form:

$$Z_{in(k)}(\omega_o, 2\omega_o, ...) = \frac{V_{in,t}(\omega_o, 2\omega_o, ...) + Z_{CM(k)}(\omega_o, 2\omega_o, ...)(I_{in,t} - I_{out,t})}{I_{in,t}} \tag{3.36}$$

3.6 Area Progression Techniques (Parallel Combining Techniques)

3.6.1 Motivation

Let's assume that we designed a power cell (Fig. 3.26c). This cell has an area of ($\alpha_1 A_e$) where α_1 is the area progression factor α_1=1 and A_e is the total emitter area (BJT case) based on a certain number of fingers. The cell produces an output power of $P_{outR(1)}$. Since the system requires more output power, why do not we add more of these cells in parallel to get more power, as shown in Fig. 3.26b? This is the basic idea

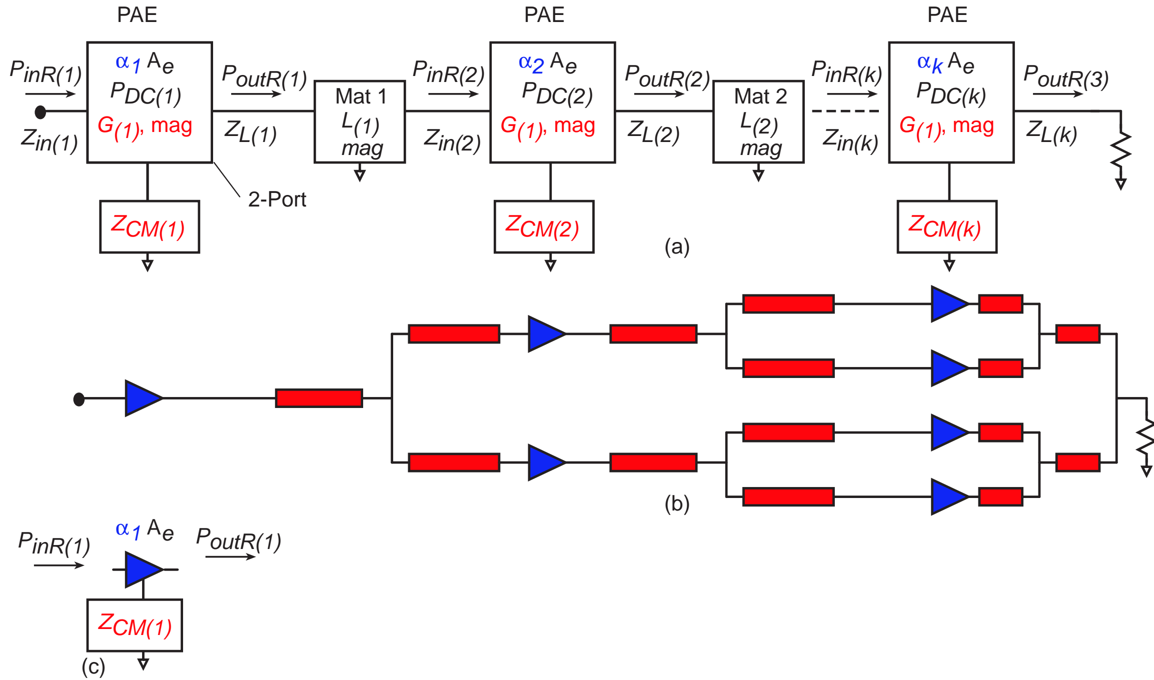


Figure 3.26: Amplifier design using area progression technique: a) Block diagram. b) Visual representation. c) unit cell.

for the parallel combining techniques. We are connecting more cells in parallel to get more output power. In this section, we will discuss the procedures of this approach and the limitations. We will present how to combiner design and the stipulations of the area progression factors, impedances... etc. to achieve the highest PAE.

3.6.2 Analysis of Amplifier Designed by Area Progression Technique

Fig. 3.26a shows a generic amplifier using area progression techniques. In this approach, we assume that the area of each stage is $\alpha_k A_e$. Note that we usually prefer the area progression factor α_k to be 2, 4, 8. This is easier to implement, as will be shown later. Each stage produces a certain amount of power ($P_{outR(k)}$) and requires a certain

amount of power $P_{inR(k)}$. The cell has a base impedance of $Z_{CM(k)}$ according to (3.37). Note that in this approach, we are stipulating that the base impedances of stage k scales with the area progression factor using the first cell base impedance ($Z_{CM(1)}$) as a reference. This implicates that all stages have the same linear gain of ($G_{(1)}$). The stage design is fairly easy. The output power for k^{th} is linearly proportional to the area progression factor (3.40). Similarly, the input power (3.41) and DC power increase with the same factor (3.44). The load (3.42) and input impedances (3.43) are inversely proportional to the scaling factor. The scaling factor depends on the previous stage's gain and interstage loss (L) in linear scales. For maximum PAE, the scaling factor is given by (3.38).

$$Z_{CM(k)} = Z_{CM(1)}/\alpha_k \tag{3.37}$$

$$\alpha_k = \frac{\alpha_{k-1} G_{(k-1)}}{L_{(k-1)}} \tag{3.38}$$

$$G_{(k)} = G_{(1)} \tag{3.39}$$

$$P_{outR(k)} = \alpha_k P_{outR(1)} \tag{3.40}$$

$$P_{inR(k)} = \alpha_k P_{inR(1)} \tag{3.41}$$

$$Z_{L(k)} = \frac{Z_{L(1)}}{\alpha_k} \tag{3.42}$$

$$Z_{in(k)} = \frac{Z_{in(1)}}{\alpha_k} \tag{3.43}$$

$$P_{DC(k)} = \alpha_k P_{DC(1)} \tag{3.44}$$

The design procedures for area progression techniques look straight forward since we know all the stage's impedances so we can design the interstage matching. Yet we should pay attention to the practical implementation of the real implementation for the stage with scaled areas. This is the main limitation of that approach. For example, if the α_k =8, that means that we need to scale the area by this factor. We can use conventional combiners such as Wilkinson to combine those required cells, but they are bulky and lossy. We will review Wilkinson power combiners to provide the necessary background. We will discuss the design procedures, advantages, and limitations. Then we will introduce a general transmission line combiner. Pros and cons will be discussed and compared to conventional Wilkinson combiner.

3.6.3 Wilkinson Power Combiner

Let's consider combining eight power cells (Fig. 3.27). For simplicity, we assume that the transistor parasitics are tuned by reactance elements included in the power cell itself. Thus, each cell requires only real load impedance. Also, we assume that each cell requires 50Ω load impedance. In most cases, the load is typically 50Ω. The 8:1 combiner should transform the load impedance (Z_L) to the required load impedance for each cell, which is 50Ω in this example with the lowest possible loss, highest bandwidth, and smallest die area.

A 2:1 Wilkinson combiner (Fig. 3.29) consists of two $\lambda/4$ transformation sections. The characteristic impedance Z_0 of each section is $50\sqrt{2}$. Quarter wave section (Fig. 3.28) is a well known way to transform impedance. The input impedance (Z_{in}) after the quarter

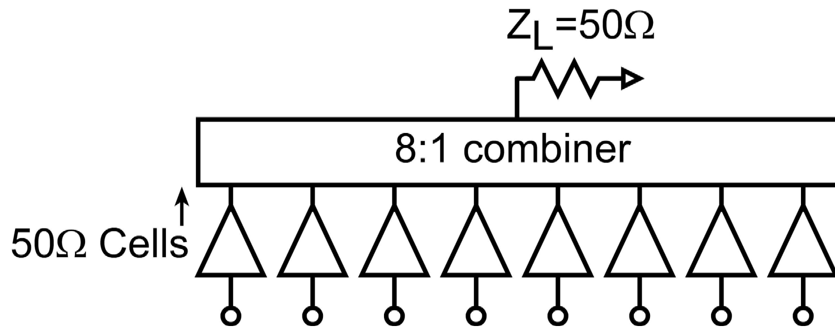


Figure 3.27: Block diagram of eight-50Ω cells.

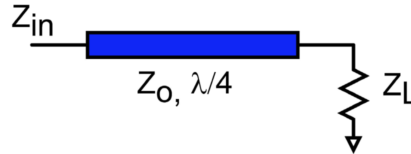


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Figure 3.28: Quarter wave transformation.

wave transformation is (3.46):

$$Z_{in} = \frac{Z_0^2}{Z_L} \tag{3.45}$$

The easy way to analyze Wilkinson is to consider the even and odd mode separately. In even mode (Fig. 3.29 b), the inputs have the same phases. We can draw a symmetry line, and this symmetry line is an open circuit. There is no current flow in the 100Ω resistance. And the load resistance (Z_L) could be split into two parallel resistances $2Z_L$. The even mode impedance (Z_{ine}) becomes

$$Z_{ine} = \frac{Z_0^2}{2Z_L} = 50\Omega \text{ for } Z_0 = 50\sqrt{2} \text{ and } Z_L = 50\Omega \tag{3.46}$$

In the odd mode (Fig. 3.29 c), the inputs are out of phase. This differential operation causes a virtual ground on the symmetry line. The input impedance after the $\lambda/4$ section is ∞. The odd impedance (Z_{ino}) becomes 50Ω.

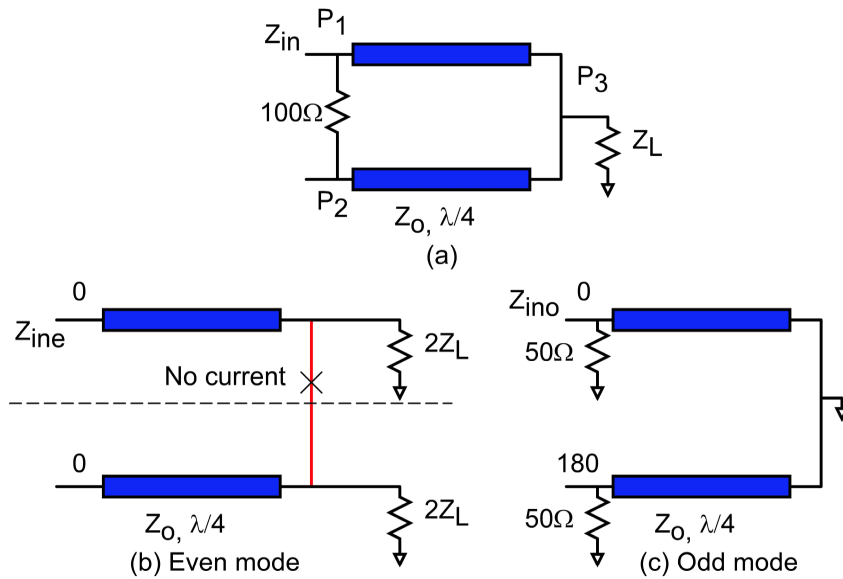

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Figure 3.29: (a) 2:1 Wilkinson combiner. (b) Even mode analysis. (b) Odd mode analysis.

We discussed 2:1 Wilkinson combiner, and we can generalize the concept and add multilevel combining to increase the number of combined cells. Fig. 3.30b shows an 8:1 Wilkinson combiner. The common-mode resistance is removed, so this is a non-isolated Wilkinson combiner. Three combining levels are required to combine eight power cells in a binary fashion. Each level requires $\lambda/4$ section, which means that we need three cascaded $\lambda/4$ sections. This shows how bulky the combiner is.

3.6.4 Pros

Wilkinson is very easy to design and scalable. It requires designing a single section, and this section is repeated everywhere. The other advantage is that Wilkinson has relatively high BW. The impedance is transformed from the load to the power cells in multiple steps.

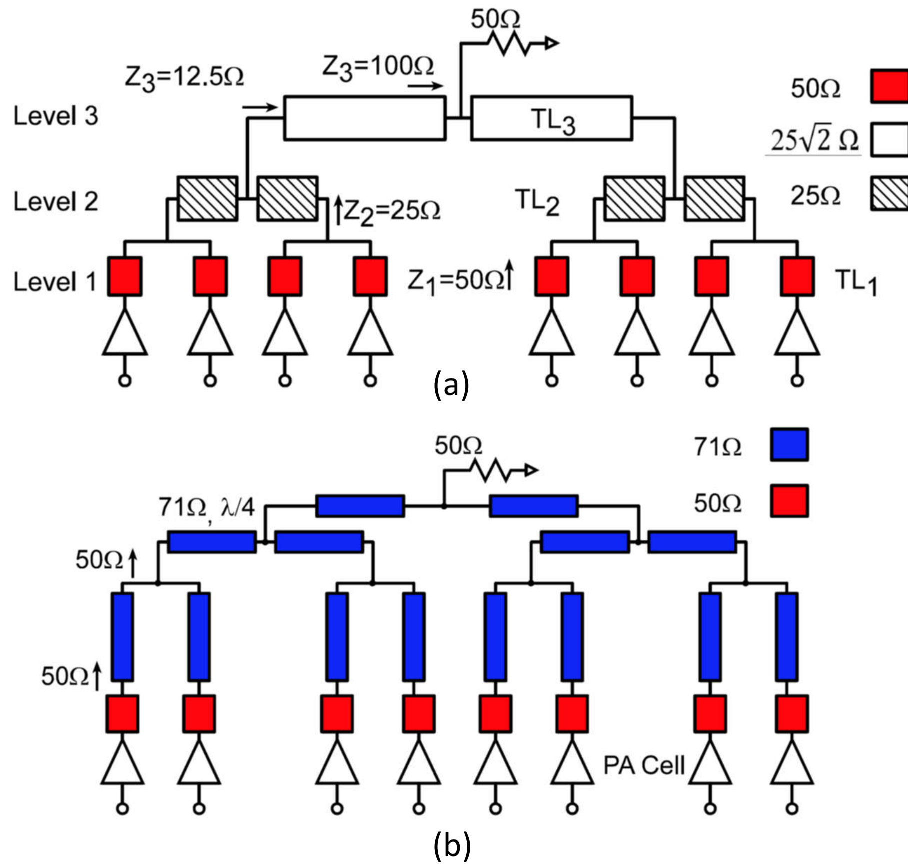

Figure 3.30: a) Proposed 8:1 transmission-line combiner for 50Ω load. b) An 8:1 Wilkinson combiner (with bridging resistors omitted)

3.6.5 Cons

As shown previously, Wilkinson is bulky since each combining level requires $\lambda/4$ section, which consumes expensive die areas. There are zigzag techniques to reduce the area, but there is a penalty for that. The more that we bend the line, the more coupling and higher loss we get. Wilkinson requires $50\sqrt{2}\Omega$ characteristic impedance for all sections. In modern IC technologies, this corresponds to skinny lines. Skinny lines have more losses and limited current capability.

3.6.6 Proposed General Transmission Line Combiner

Wilkinson is a special case for transmission line combiners. In this section, we will present a more generic transmission line approach. Let's consider a simple example as a motivation for the generic approach. Two parallel transmission lines with characteristic impedance Z_o are equivalent to a single transmission line with characteristic impedance $Z_o/2$ and the same electrical length. Lower impedance lines are wider and usually have lower losses. Note that there are non-ideality effects, and wider lines do not necessarily have better losses. There is a maximum line width, and transmission line theory fails, leading to a loss increase.

Let's consider 50Ω power cells. By definition, power cells have small 50Ω transmission line sections at the output. Two parallel transmission lines could be combined using 25Ω lines with arbitrary length. The 25Ω line should be terminated by 25Ω load impedance to get the required load impedance for each power cell. Similarly, we can combine two 25Ω lines into a single 12.5Ω line (any length) with a 12.5Ω load impedance and so on. We can continue this binary tree until we end up with a single output. The impedance transformation is not a function of the length of those lines, but we should use minimum length to reduce the loss.

For proper operation, this approach requires 12.5Ω Z_L for 4:1 combiner and 6.25Ω Z_L for 8:1 combiner. In most cases, Z_L is 50Ω. This means that we still need a $\lambda/4$ transformation between the combiner and Z_L. We can synthesis Z_o of this $\lambda/4$ from (3.46). Fig. 3.30a shows 8:1 combiner using single $\lambda/4$ line.

3.6.7 Pros

Clearly, the proposed combiner is very compact since it uses only a single $\lambda/4$ section. The signal passes through a single $\lambda/4$ section, which results in lower losses compared to Wilkinson. We can also notice that all the sections are low Z_o so, they are wide by necessity. Wide lines have, in general, better losses compared to skinny lines. Additionally, wide lines permit high currents. This is attractive, especially if we want to bias the power cells through the combiner with a minimum IR drop on the lines.

3.6.8 Limitations

The generic combiner requires designing multiple transmission lines with different characteristic impedances, which add a little bit overhead. The other limitation is the bandwidth. We have a smaller number of transformation sections compared to Wilkinson. The more cells that we combine, the smaller the required impedance that we require. Although the BW is smaller than Wilkinson, it is still sufficient for communication systems. Measurement shows more than 40GHz BW at 140GHz. Usually, the BW limitation comes from the packaging design (transition and antenna).

3.6.9 Example for Area Progression Technique: Three-Stage Amplifier

In this section, we provide a design example for a three-stage amplifier designed by area progression technique using lossless matching networks at 140GHz using 250nm InP HBT technology.

Step #1: The first step is similar to the stack design procedure. We run load-pull simulations for different topologies and select the topology with the highest PAE at the

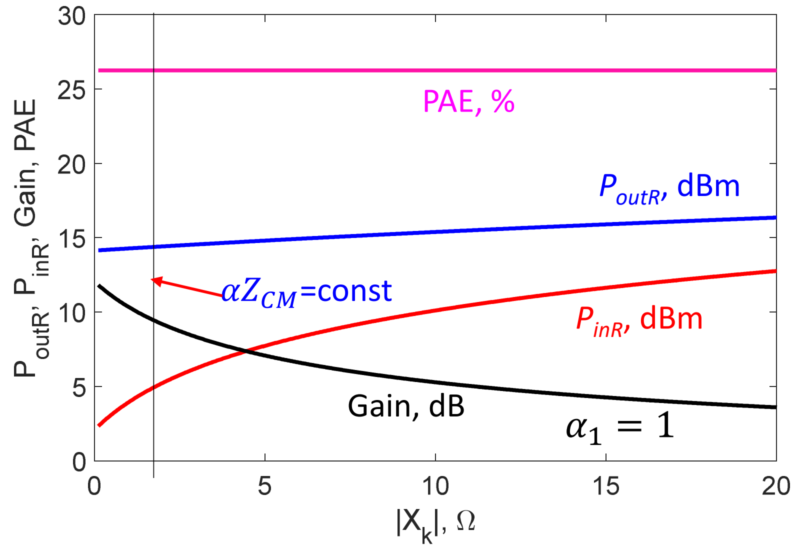

Figure 3.31: Stack design contours at constant normalized base impedance.

required compression level. We can also use the previous stack design contours as a design guide for area progression techniques. Fig. 3.31 shows the stack design contours for CB design at 140GHz. In the area progression technique with constant normalized base impedance, we stipulate that we are working at a constant normalized common lead impedance. This is represented by the vertical line in Fig. 3.31. This vertical line is chosen based on the available input power. This will define all the properties for the first stage (gain, power, and required impedances).

Step #2: We already have derived a relation between generic cell and the first stage using equations (3.38, 3.40, 3.41, 3.42, 3.43, 3.44). Fig. 3.32a shows the input, output powers and gain versus the area progression factor for the three stage amplifier. As a sanity check, we can see that the output power for each stage equals precisely the necessary input power for the following stage which achieve the highest possible PAE. The corresponding block diagram is shown in Fig. 3.32b.

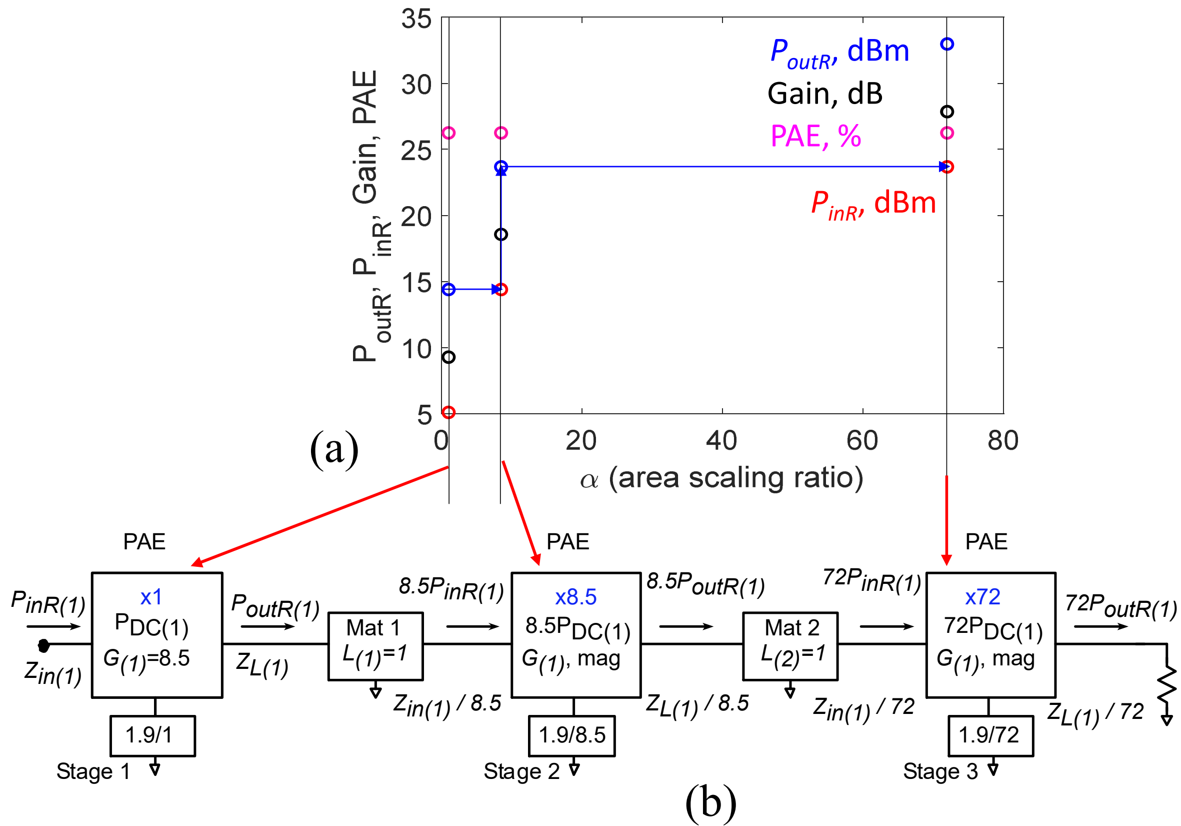

Figure 3.32: a) Output power, input power, gain, and PAE versus the areas scaling factor. b) Amplifier block diagram.

Step #3: The load impedance and input impedances for each stage is precisely defined w.r.t the first stage according to (3.42, 3.43) and they are plotted in Fig. 3.33. We can design the required matching circuit by any of the previous combining technique.

3.6.10 Area Progression Technique Efficiency

We assumed in our previous example that we have lossless matching. Looking at Fig. 3.33, we can notice that the required impedance is getting close to the edge of the smith chart. This means that the more that we add stages, we are getting higher losses. It also looks very ambitious that we can combine ~72 cells at the 3$^{\text{rd}}$ stage. To answer this puzzle, we included a simplified loss model. We assumed that the loss increases by 1dB

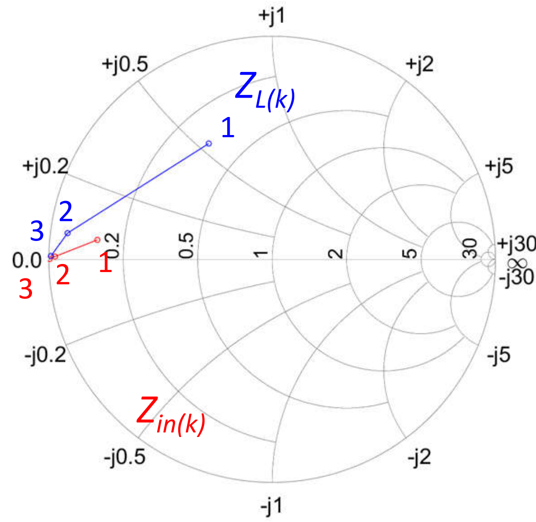

Figure 3.33: Z_L and Z_{in} as a function of the stage index. It shows the required interstage impedance transformation contours

for each area doubling (3.47). This means that we are losing 4dB to combine 16 cells. This is a simplified model since we cannot keep increasing the number of combined cells indefinitely, and at a certain point, the loss becomes unmanageable. Fig. 3.34 shows the proper scaling factor for each stage given our loss model. Now we can see that the number of cells in the 3rd stages reduced significantly to ∼16 after including the loss. Additionally, the PAE drops as we add more stages. The curve shows the efficiency degradation due to area progression technique approaches.

$$L, dB = 1 \ log_2(\alpha_k) \tag{3.47}$$

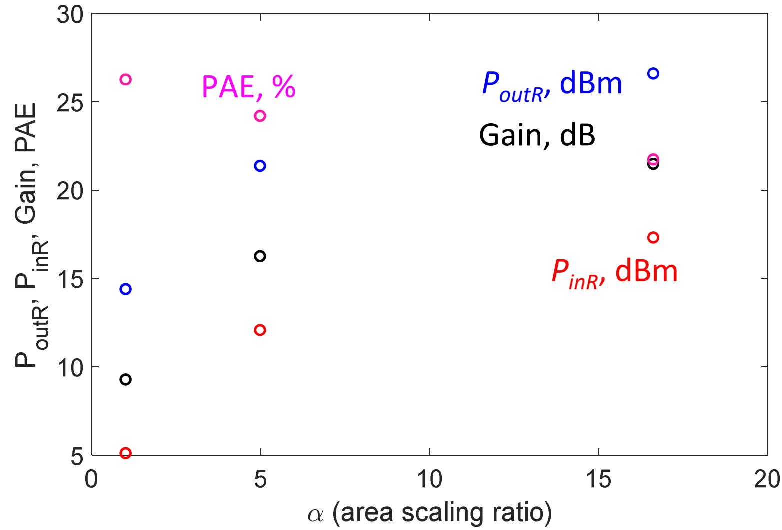

Figure 3.34: P_{outR}, gain, PAE versus the area progression factor including splitter loss.

3.7 Stacked Amplifier with Area Progression

3.7.1 Motivation

So far, we provided the rigorous design procedure for pure stack design in Section 3.5.4 and pure area progression in Section 3.6. The logical progression is to include both techniques to get more degrees of freedom. Fig. 3.36c shows the general form of the amplifier. We can have different area progression factors and different base impedances for each stage. Now, the design becomes challenging since changing the base impedance or the area changes the stage's power, gain, and impedances in different ways. First, we derived the input and output power equations in (3.48) and (3.49). Those equations are simply the output and input power in the stack case (3.14, 3.11) after including the area progression factor (α_k). We can use the same gain equation derived earlier (3.16) in the stack. Note that the base impedance, in this case, is the normalized base impedance, and we should de-normalize it to get the absolute value, as will be shown in the next

example.

$$P_{inR}(X_k, \alpha_k) = \alpha_k(0.5|V_{in,t}||I_{in,t}|cos(\angle V_{in,t} - \angle I_{in,t}) - 0.5X_k|I_{in,t}I_{out,t}|(sin(\angle I_{out,t} - \angle I_{in,t}))) \tag{3.48}$$

The real output power could be written as:

$$P_{outR}(X_k, \alpha_k) = \alpha_k(0.5|V_{out,t}||I_{out,t}|cos(\angle V_{out,t} - \angle I_{out,t}) - 0.5X_k|I_{in,t}I_{out,t}|(sin(\angle I_{out,t} - \angle I_{in,t}))) \tag{3.49}$$

We used the same voltages and current values for our previous 140GHz CB example (Fig. 3.9) in 250nm InP HBT and plotted the output power (3.49) in Fig. 3.35. This is a contour plot for the output power as a function of the normalized base impedance and scaling factor. The power contours show that we can get the same power level by using a constant area progression factor (α_k) and change only the base impedance (stack approach). Or we can keep constant normalized base impedance and scale the area (area progression techniques). Finally, we can change α_k and the base impedance accordingly to get the same power. The latter is a combination of the stacking concept and area progression techniques. Fig. 3.35b shows the gain contours versus the normalized base impedance. We used the same gain equation derived in the stack (3.17), keeping in mind that we are plotting versus the normalized base impedance and not the base impedance only. The figure shows that the gain contours are vertical lines, which means that it is not a function of the scaling factor, and that is consistent with the area progression techniques.

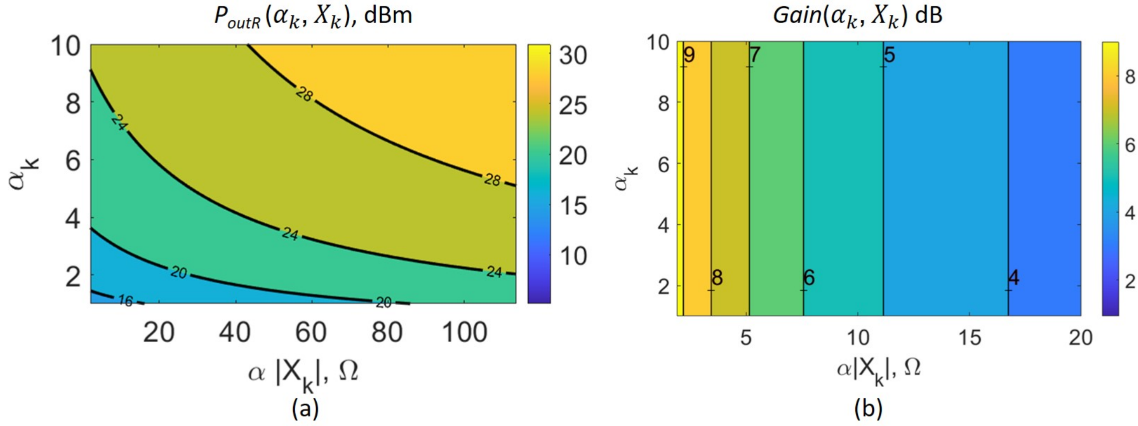

Figure 3.35: a) Contour plots for the output power function of the normalized base impedance and area progression factor. b) Contour plots for the gain function of the normalized base impedance and area progression factor.

Let's consider designing three CB stage (Fig. 3.36)c using stacking and area progression techniques together.

1. The available input power defines the (α_1 and $Z_{CM(1)}$) for the first stage. In this example the output power from the first stage ($P_{outR(1)}$) is 14.4dBm.

2. Assuming a lossless matching the output power from the first stage must equal the necessary power for the second stage ($P_{outR(1)}$=$P_{inR(2)}$). Looking at Fig. 3.36b, we can see that there is a contour for a constant power ($P_{inR(2)}$=14.4dBm) that can satisfy the highest PAE. For the sake of demonstration, we picked α_2=2 and $Z_{CM(2)}$=14Ω. Once we select α_2 and $Z_{CM(2)}$, we can substitute in Fig. 3.37a to get the output power for the second stage ($P_{outR(2)}$)

3. Similarly we can design the third stage. The output power for the second stage ($P_{outR(2)}$) defines a contour for all possible combinations (α_3 and $Z_{CM(3)}$) as shown in Fig. 3.37.

4. Now we computed all (α_k and $Z_{CM(k)}$) for all stages. The next step is to design

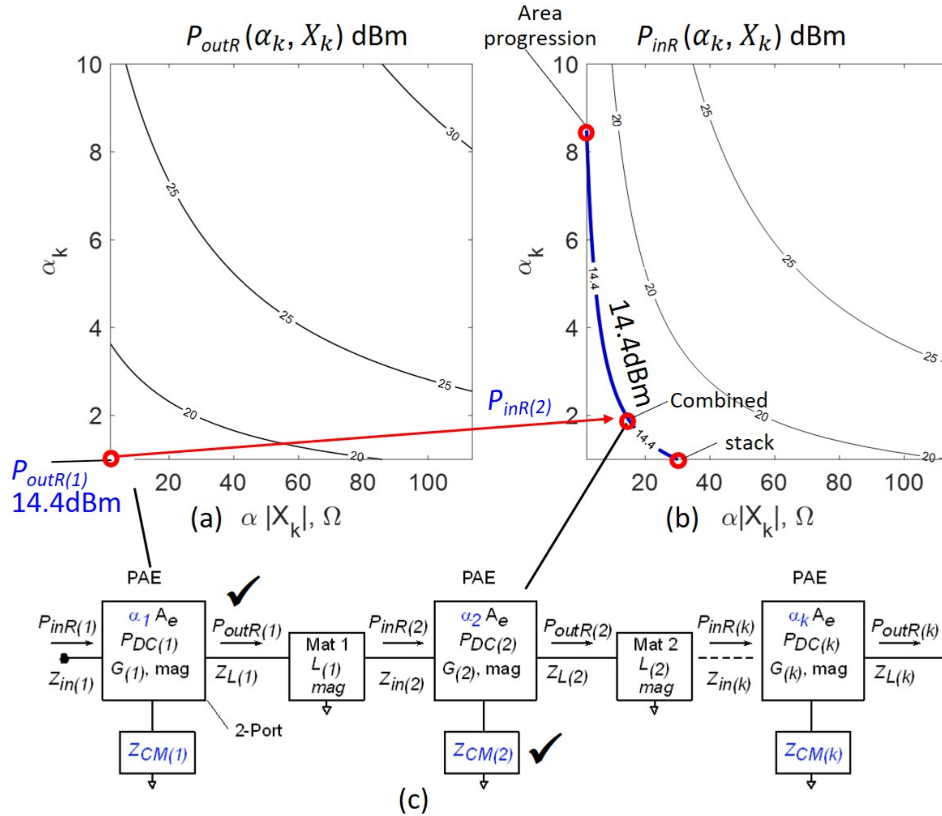

Figure 3.36: a) Output power contours showing the power of the first stage's power. b) Contour for the input power highlighting the design contour for the second stage. c) General amplifier form considering impedance and area progression techniques.

the interstage tuning network. Fig. 3.38a shows the load and input impedance function of the normalized base impedance that we already computed. According to the scaling factor for each stage, we can de-normalize the impedances to get the absolute values, as shown in Fig. 3.38b.

5. We used all the (α_k and $Z_{CM(k)}$) and used ideal matching circuits using smith chart components in Fig. 3.39a. We monitored the simulated output and input power for each stage and compared them to calculated from the theory in Fig. 3.39b, and there is a good agreement. As a sanity check, we also simulated the internal voltages (Fig. 3.39). They are clipping simultaneously which indicates that the

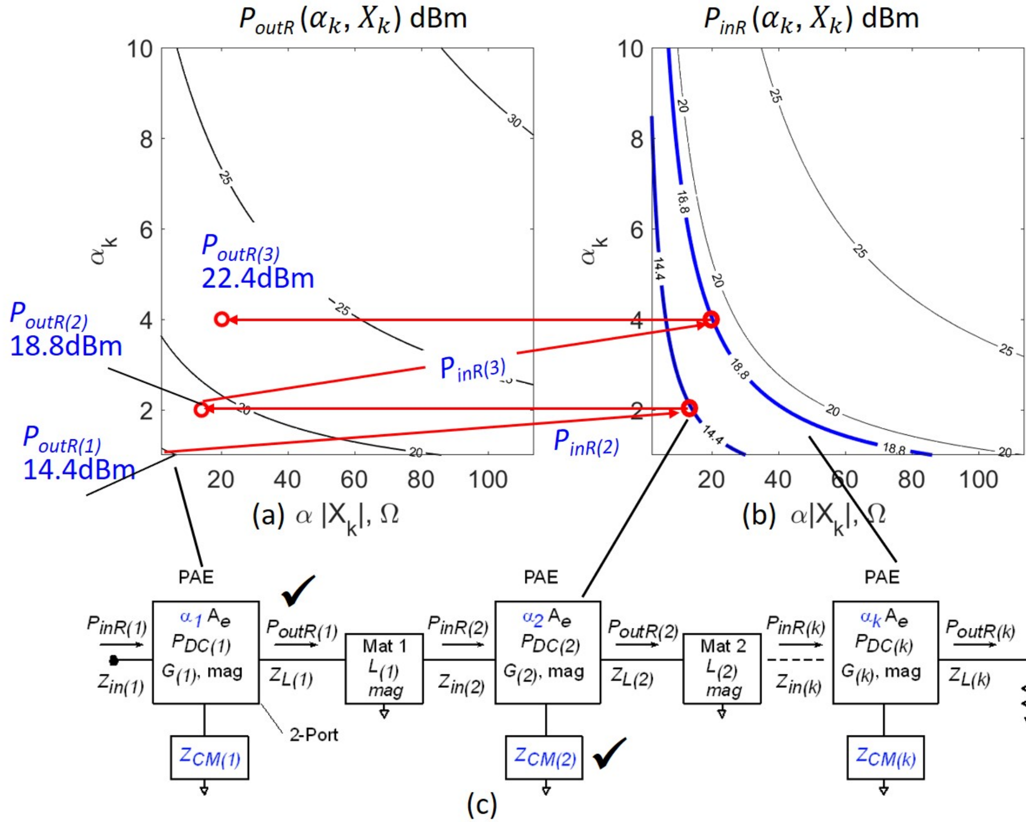

Figure 3.37: a) Output power contours showing the design procedures. b) Contour for the input power highlighting the design contours. c) Block diagram for amplifier designed with area and stacking techniques.

amplifier has the highest PAE.

3.8 Design Guide for Amplifier Design

This section summarizes and provides a design sequence for the amplifier design with the highest PAE. We start with a given input power source, and the objective is to reach a certain power level with the highest possible PAE. The first stage is quite easy to define. There are multiple options for the following stages (Fig. 3.40). We can use stacking techniques (case1), area progression techniques (case2), or stacking with area progression (case3). The more stages that we add, the more options and degrees of

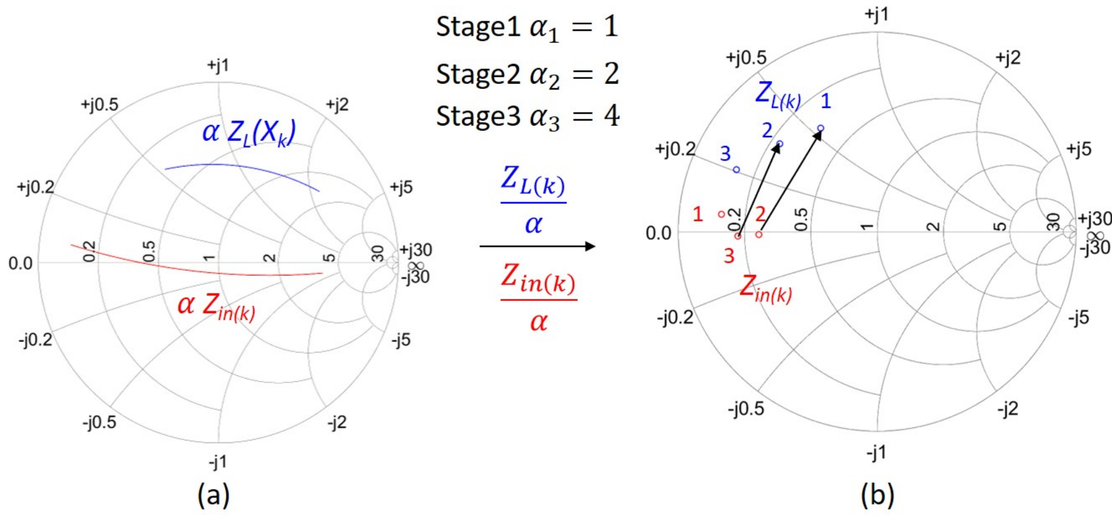

Figure 3.38: a) Impedance chart showing the load and input impedance versus the normalized base impedance. b) Impedance values for the amplifier after applying the proper scaling factor.

freedom we get. We also may consider the biasing for each stage as another degree of freedom. Additionally, some technologies offer different types of transistors. All those degrees of freedom increase the design options.

For lossless matching networks, all the design techniques result in the same PAE level. However, for lossy networks, the PAE could vary for each technique. Each technique requires a different implementation. It is possible that parallel power combining gives better losses compared to the series power combining or vice versa. The rigorous way is to automate those design steps and try all the possible combinations. However, experience helps in reducing those enormous amounts of options resulting in the highest PAE.

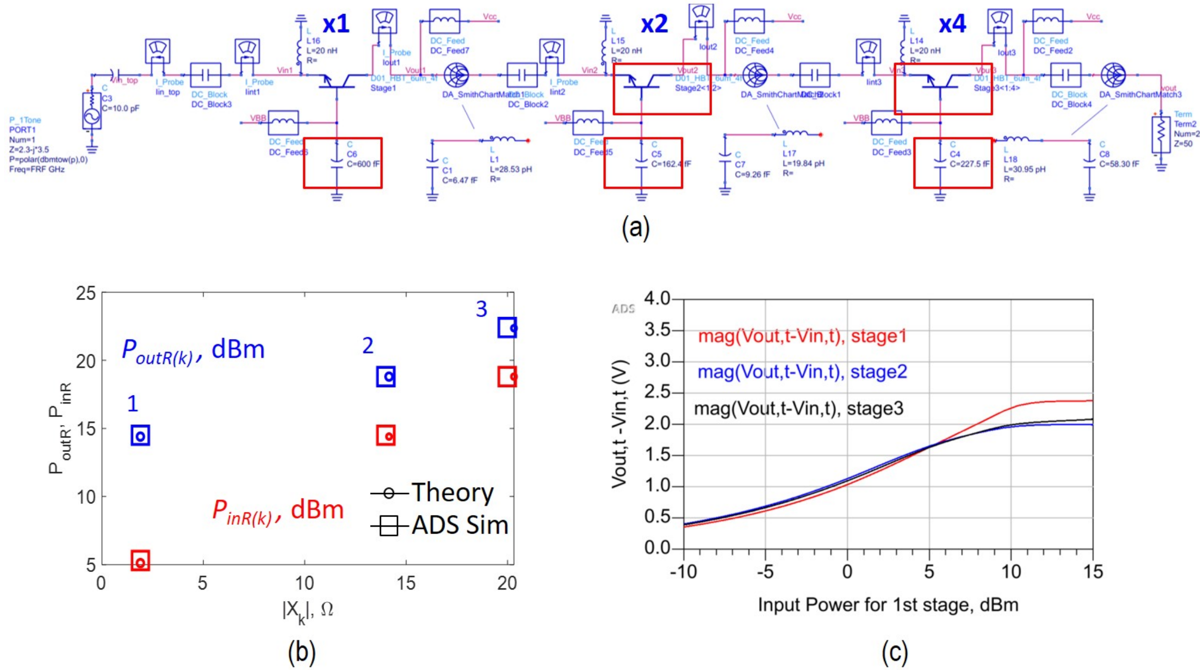

Figure 3.39: CB example using stacking and area progression techniques: a) Schematic diagram. b) Simulated and theoretical stages power showing the location of the proper base reactance. c) Simulated and theoretical stages impedances highlighted at the location of the proper base reactance value.

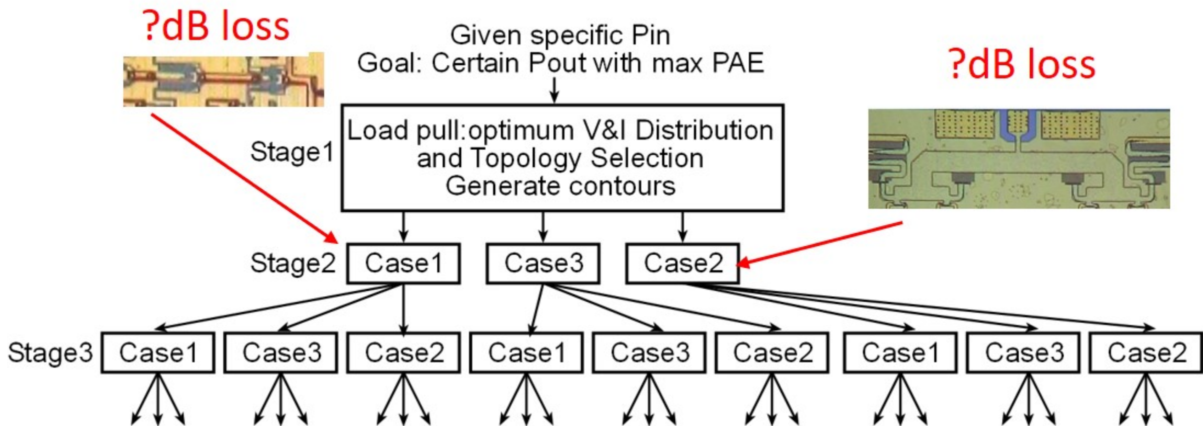

Figure 3.40: Amplifier design guideline.

Chapter 4

Experimental Verifications for High-Efficiency Power Amplifiers ($\sim$140GHz, 210GHz, and 300GHz)

4.1 Introduction

We have reviewed the power amplifier fundamentals in Chapter 2 and presented guideline for optimum amplifier design in Chapter 3. Here we will focus on the experimental verification. Several power amplifier designs are presented at 140GHz, 210GHz, and 340GHz in 250nm InP HBT technology and 130nm InP HBT technology [2]. Those amplifiers can serve in the massive MIMO demos, which demonstrate a very high data rate and long-range communications. We can use other low-cost technologies such as CMOS to build the whole transmitter in CMOS and use it as a driver for the InP amplifiers.

We designed a 140GHz, 20.5dBm amplifier [28] with a record 20.8% PAE and 15dB associated large signal gain. The key features in the design are a low-loss 4 to 1

transmission-line power-combining network, a common base architecture, and driver scaling to sustain good PAE. The amplifier has a peak measured small-signal gain of 20.3dB at 140GHz with a 3dB BW of 43GHz. The 140GHz OP_{1dB} is 17dBm with 9.7%PAE. Over a 125-150GHz bandwidth, the saturated output power is within 2dB of its 140GHz maximum, with an associated PAE greater than 14.3%. The amplifier demonstrates low DC power dissipation of 0.52W and a compact area of 0.69mm^2.

The second D-band amplifier design combines eight cells producing higher output power. The amplifier uses a compact, low loss 8:1 power combiner, and capacitively linearized common-base power and driver cells. At 140GHz, the amplifier has 22.8dBm saturated output power with 16.7% PAE and 16.1dB associated gain. At 140GHz and 1dB gain compression, the output power is 20.2dBm with 9.4% PAE and 20.3dB associated gain. The peak saturated output power is 23dBm with 16.5dB associated gain and 17.8% PAE at 131GHz. Over 127-151GHz, the saturated output power is greater than 22.3 dBm with greater than 15% associated PAE. The amplifier consumes 1.1W DC power, and the die area is 1.34mm^2.

We are also presenting experimental verification for the mm-wave stacked power amplifier above 220GHz and 340GHz. We proved the theoretical analysis in Chapter 3 at 220GHz [13] and 340GHz [29]. The amplifiers were designed using the two-port synthesis procedure that computes the required transistor input, load, and common-lead impedances from the available input power and from the transistor two-port terminal voltages and currents required for efficient large-signal operation. The first 220GHz PA using a 3:1 series connection, with one gain-matched and two power-matched transistors, produced 11.7 dB large signal gain and 15.1 dBm saturated output power at 204 GHz. A second 220GHz PA consists of two-unit cells, with input and output 2:1 transmission-line

power-combiners, plus a pre-driver stage. This design produced 16.5 dB large signal gain and 18 dBm output power at 204 GHz.

We introduce similar series-connected amplifiers operating at 325 GHz [29]. The first design (the unit cell) connects two transistors in series and produces 9.4 dBm saturated output power with 2.2% PAE and 4.3 dB compressed gain at 243 mW DC power consumption. It has a 10 dB small-signal gain, and the 3-dB bandwidth extends from 311-325 GHz. The saturated output power is at least 4 mW over a 323-340 GHz bandwidth. In the second amplifier, a transmission-line network combines two of these cells, and two further cells serve as driver stages. This PA produces 11.4 dBm saturated output power with 1.09% PAE at 9.4 dB gain driven. The 3-dB bandwidth extends from 316 GHz to 325 GHz.

4.2 250nm and 130nm InP HBT technology

This section describes the technologies used in the following amplifiers. The amplifiers are designed in either 250nm or 130nm InP HBT technology from Teledyne. Fig. 4.1b shows a cross-section view in 250nm InP technology [2]. The technology offers four Au interconnect layers, 0.3fF/μm2 MIM capacitors, and 50Ω/square thin-film resistors. The HBT has a maximum 650GHz power gain cut-off frequency (f_{max}), a maximum of 3mA/μm current density, and the 4.5V $\mathrm{VB_{CEO}}$.

The 130nm InP HBT technology [2] (cross section in Fig. 4.1a) has a 1.1 THz power-gain cutoff frequency ($\mathrm{f_{max}}$), a 3.5 V breakdown, and a maximum ∼3 mA current per μm emitter finger length. The Au interconnect stack has three layers, with 1 μm Benzocyclobutene (BCB) (ϵ_r=2.7) between metal 1 and metal 2, and 5 μm BCB between metal 2 and metal 3. 50Ω microstrip lines between metal 1 and metal 3 have 1.4 dB/mm

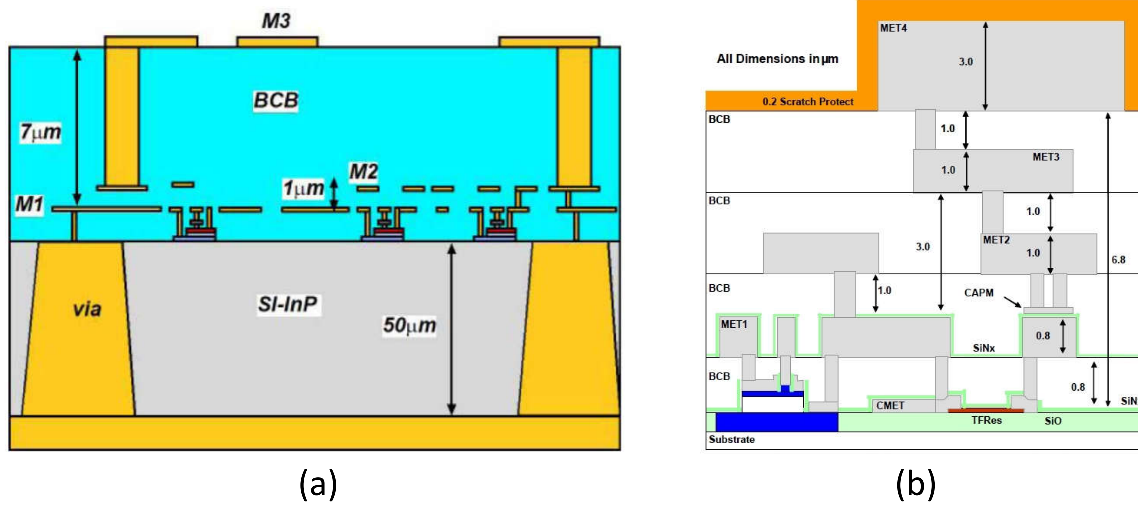

Figure 4.1: Schematic cross section of a) 130nm InP HBT. b) 250nm InP HBT technologies[2].

loss (0.9 dB per guide wavelength) at 300GHz. There are 0.3fF/μm^2 MIM capacitors and 50Ω/square thin-film resistors.

4.3 140GHz Power Amplifier with 20.8%PAE and 20.5dBm Output Power

4.3.1 Amplifier Design

This is a high-efficiency D-band power amplifier in 250nm InP HBT technology. The design has three common-base stages and a low-loss 4:1 transmission-line output power combiner. The amplifier has 20.5 dBm peak saturated output power with 20.8% PAE and 15dB associated large-signal gain at 140GHz. At 1dB gain compression, the output power is 17dBm with 9.7% PAE. The amplifiers peak small-signal gain is 20.3dB at 140GHz, and the small-signal 3-dB bandwidth is 120-163GHz. Over a 125-150GHz bandwidth, the saturated output power is within 2dB of its 140GHz maximum, with an associated

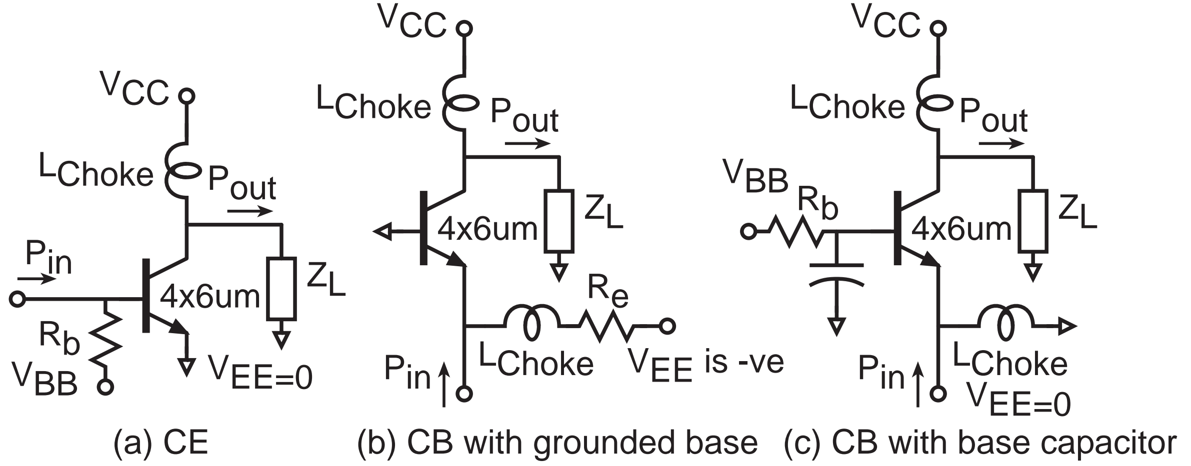

Figure 4.2: Schematic diagram of: (a) CE. (b) CB with grounded base. (c) CB with 600fF base capacitor.

PAE greater than 14.3%. The amplifier consumes 0.52W DC power and occupies an area of 0.69mm^2. This result improves the state-of-the-art peak PAE at 140GHz by 1.6:1 for amplifiers of comparable saturated output power. The IC was fabricated in the Teledyne 250nm InP technology [2], which is described in Section 4.2

4.3.2 Unit Cell design

Both common emitter (CE) and common-base (CB) designs were considered. In power amplifiers, the output tuning network is designed for maximum saturated output power, not for maximum small-signal gain [8]. Large-signal simulations for CE (Fig. 4.2a), CB with a grounded base (Fig. 4.2b), and CB with a finite base capacitance (Fig. 4.2c) are performed under loading for maximum saturated output power, for a device having 4 emitter fingers each of 6μm length, biased at 1.4mA/μm and V_{CE}=2.5V. The CB stage with a grounded base (Fig. 4.3) has ∼2.4dB greater gain than CE, but biasing requires a negative supply V_{EE} and system efficiency is degraded by the voltage drop across the necessary emitter bias stabilization resistor R_e or DC current source. We instead use a

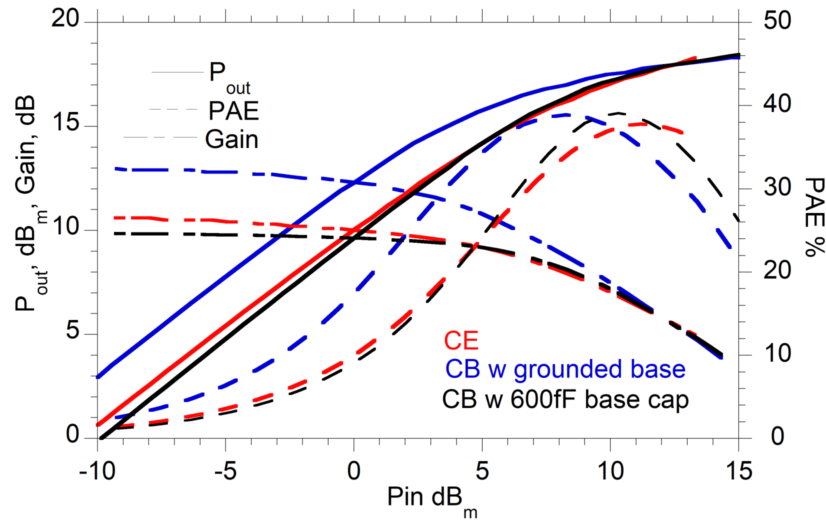

Figure 4.3: P_{out}, gain, and PAE for CE, grounded CB, and CB with base capacitor.

CB stage with a base bypass capacitor (Fig. 4.2c). The base resistor R_b provides stable control of I_C; DC power wasted in R_b is small because I_B is much smaller than I_C. The maximum base capacitance is limited by physical layout and the resulting self-resonance. The capacitor's impedance is nonzero, there is a significant AC base voltage swing and the gain is reduced. However, the PAE is almost constant despite this gain reduction (Fig. 4.2d). The CB stage with a finite base capacitance, coupled with its driver stage, can be analyzed as a generalized series-power- combined stage [13],[29], and [25] with the output power being the sum of power contributed by the output transistor and input power from the driver stage.

Though the CE and capacitively-bypassed CB stages show similar saturated PAE, the capacitively-bypassed CB stage was selected because the latter shows greater PAE at the 1dB gain compression point. This is a consequence of gain linearization provided by the impedance presented to the base. The OP_{1dB} for CB with a 600fF base capacitance is 15.2dBm with 29.7% PAE compared to 12dBm with 15.4% PAE in CE and 13.5dBm

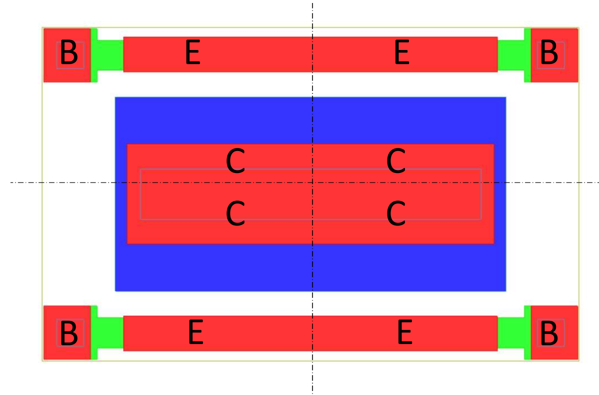

Figure 4.4: Transistor footprint for compact 4 fingers connected together. Each is 6μm emitter length. Total emitter periphery is 24μm

with 22.4% PAE for the grounded-base CB stage. OP_{1dB} is highest for the finite-base-capacitance CB stage simply because of the contribution of the driver stage power.

We are using compact 4-finger CB layout (Fig. 4.4) which presented smaller parasitic interconnect impedances than did the 4-finger CE design, providing larger gain once electromagnetic analysis of the multifinger layout parasitics were included in the simulations. Multifinger transistor layout design is critical in mm-wave power amplifiers. The transistor footprint (Fig. 4.4) is similar to [30], except that the bases are grounded through a 426fF MIM capacitor.

The power unit cell (schematic in Fig. 4.5a and corresponding layout in Fig. 4.5b) has 2 emitter fingers, each 12μm length, with base contacts at each end; in terms of parasitic base metal inductance and resistance, this layout is equivalent to 4 fingers each 6μm emitter length. The transistor collector capacitance (Fig. 4.5) is tuned by a shunt inductive transmission-line section, terminated by a bypass capacitor. This network also supplies the collector DC bias. The base DC bias is routed between cells using the transistor collector contact metallization layer, which lies below the metal-1 ground plane, reducing coupling between DC and RF signal lines. The microstrip lines use a metal-1

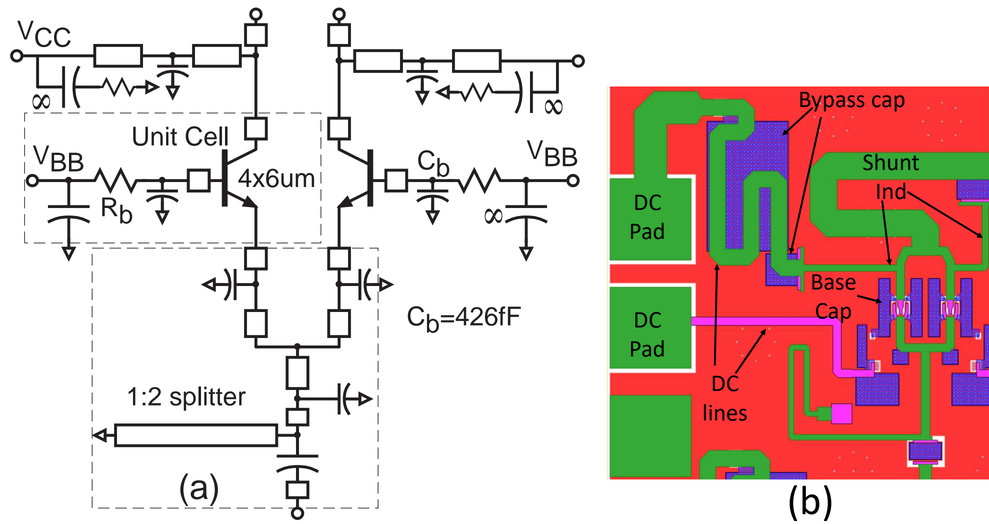

Figure 4.5: (a) Schematic diagram of two combined power amplifier cells driven by a single driver cell. (b) Corresponding layout.

ground plane and metal-4 RF conductor. The inputs of two-unit cells are combined and matched to the driver optimum load impedance by L-C sections. Staggered matching provides wideband operation. Input shunt stubs provide both RF impedance tuning and a DC path for the emitter current. DC bias is isolated between stages using series MIM coupling. ADS momentum and HFSS tools are used to simulate all routing and matching circuits.

4.3.3 Driver design

Two driver stages are added to increase the gain. Their architecture (Fig. 4.6) is similar to the PA cell. The base capacitance is increased to 603fF, increasing the gain to ∼7dB. The driver output power is sufficient for one driver cell to drive two PA output cells. The driver's input and output impedances are matched close to 50Ω. The matching network tuning is staggered to increase the bandwidth. The transistor base bias is distributed on the collector contact metal layer, while DC collector bias is distributed on metal 4. All DC bias lines are bypassed using MIM capacitors with 10Ω

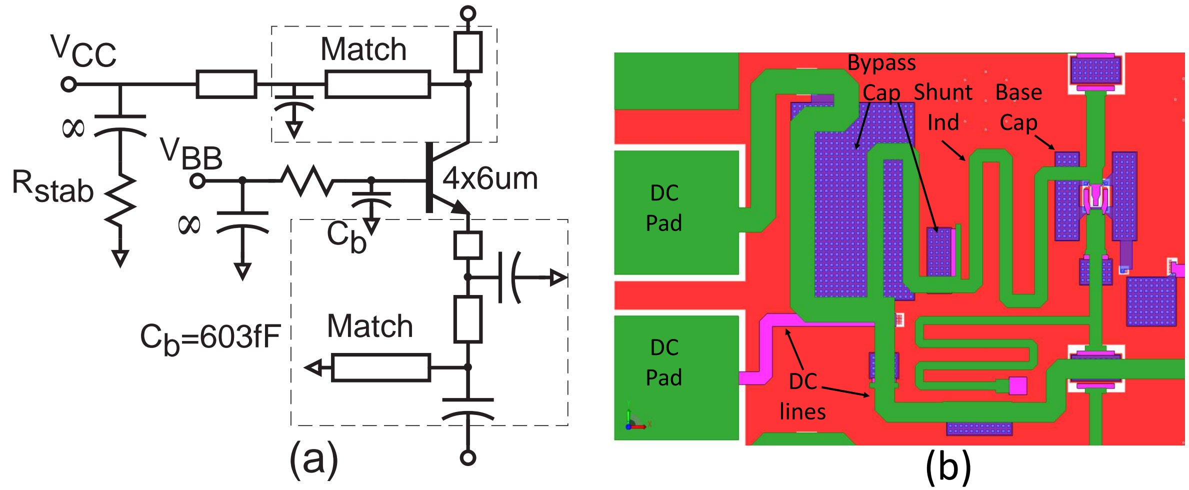

Figure 4.6: Schematic diagram of: (a) Driver stage with input/output matching circuits. (b) Driver layout.

series damping resistors. The first driver stage uses the same transistor size as the 2nd driver stage, but uses reduced DC bias, V_{CC3} and V_{BB3}, for higher PAE.

4.3.4 Combiner design

Four 50Ω power cells are combined to achieve the required power. For 50 Ω load, cascaded Wilkinson combiners (Fig. 4.7b) can provide 4:1 combining. However, this requires two cascaded $\lambda/4$ sections and results in a simulated 0.66dB loss at 140GHz and large die area. The proposed combiner (Fig. 4.7a), similar to ([22], [31]), uses only one $\lambda/4$ section, which is more compact and has 0.48dB simulated losses at 140GHz for a 50Ω load. Two 50Ω cells are combined using transmission line sections with Z_1 =50Ω. The length of Z_1 is kept small for minimum loss but the length does not impact the impedance transformation. The required load impedance for the two combined cells is 25Ω. This is achieved by the $\lambda/4$ section, Z_2, which transforms the 100Ω present at its load to 25Ω.

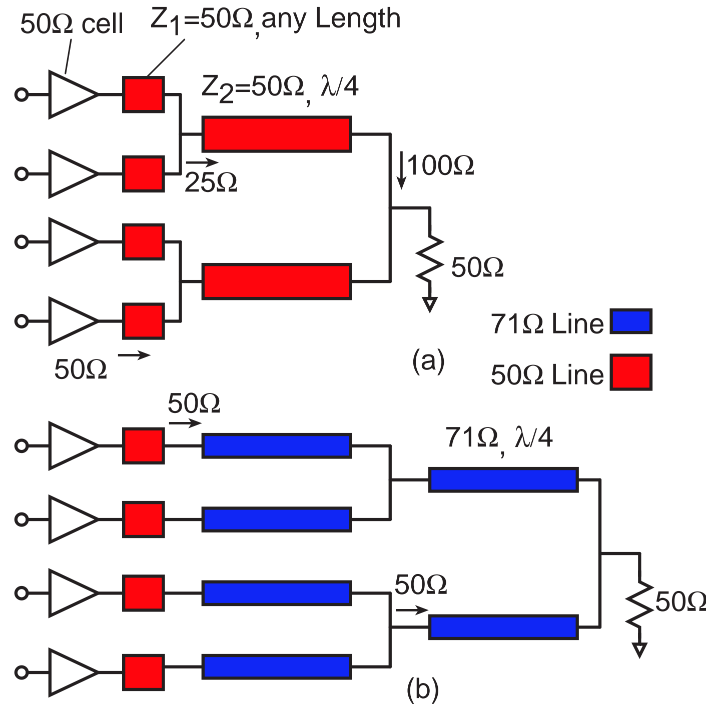

Figure 4.7: Schematic diagram (a) 4:1 low loss transmission line combiner for 50Ω load. (b) 4:1 Wilkinson power combiner (with bridging resistors omitted) for 50Ω load.

The amplifier is designed for packaging. The IC uses a dense array of through-substrate vias (TSVs) to connect the chip and backside ground planes and to suppress substrate modes. The RF I/O pads are relatively large, 55μmx57.5μm, to be compatible with wirebonds. To tune the resulting pad capacitance, Z_2 is adjusted to 31 Ω. This increases the 4:1 combiner loss to 0.93dB (including the shunt inductive tuning elements and without the pad losses). The simulated pad loss is ∼0.32dB at 140GHz.

4.3.5 S-Parameters measurements

Fig. 4.8a shows the IC micrograph and Fig. 4.8b shows the IC block diagram. S-parameters are measured using an HP network analyzer with VDI 110-170GHz frequency extenders and 140- 220GHz GGB wafer probes with WR-5 to WR-6 waveguide adapters.

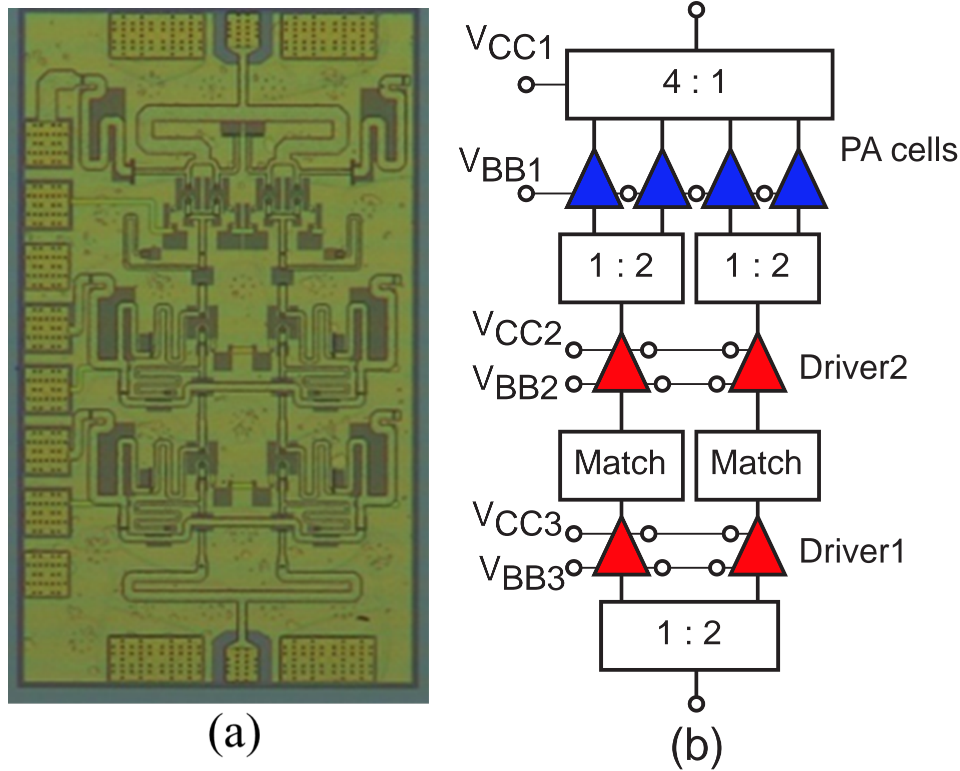

Figure 4.8: (a) Chip micrograph of the power amplifiers. The area is 1.08mm 0.63mm including the pads. (b) Amplifier block diagram.

Probe-tip calibration is done using SOLT standards on an external CS-15 calibration substrate. Table 4.1 summarizes the DC biases. The DC biases of the drivers are optimized to improve the PAE; the IC dissipates 0.52W.

The IC has 20.3dB peak measured small-signal gain (Fig. 4.9) at 140GHz. The agreement between the measurement and simulation results is best when the foundry-

Table 4.1: DC biases for S-parameters

$\mathbf{V_{CC1}}$	$\mathbf{V_{CC2}}$	$\mathbf{V_{CC3}}$	$\mathbf{V_{BB1}}$	$\mathbf{V_{BB2}}$	$\mathbf{V_{BB3}}$
2.5V	2.5V	1.5V	1.94V	1.36V	1.1V
$\mathbf{I_{CC1}}$	$\mathbf{I_{CC2}}$	$\mathbf{I_{CC3}}$	$\mathbf{I_{BB1}}$	$\mathbf{I_{BB2}}$	$\mathbf{I_{BB3}}$
121mA	52mA	31.8mA	4.1mA	1.7mA	0.95mA

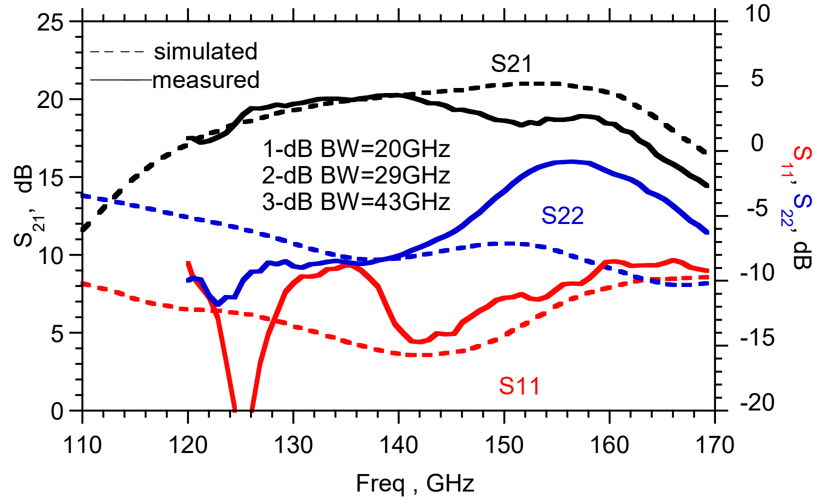

Figure 4.9: Measured (solid) and simulated (dashed) S-parameters.

recommended base inductance is neglected. As the impedance presented to the HBT base involves a series combination of this inductance and the MIM base bypass capacitance, we believe that this disparity is due to small errors in modeling the MIM base capacitance.

The gain S_{21} is flat to within 1dB between 126-146GHz and to within 3dB gain between 120-163GHz. The input reflection coefficient S_{11} is better than -10dB from 138GHz to 157GHz and better than -8.4dB from 120 to 170GHz. As the output is tuned for maximum saturated output power, S_{22} is necessarily poor, but is better than -6dB from 120-145GHz.

4.3.6 Power Measurements

Power was measured on the 3-mil die without bonding to a heat sink. A 110-170GHz VDI frequency extension module with an added output attenuator delivers up to ∼10dBm, sufficient for power measurements (setup in Fig. 4.10). 140-220GHz wafer probes were used with WR6 to WR5 adapters. An Erickson meter measured the output power. Probe losses were measured to move the power reference plane to the probe tips.

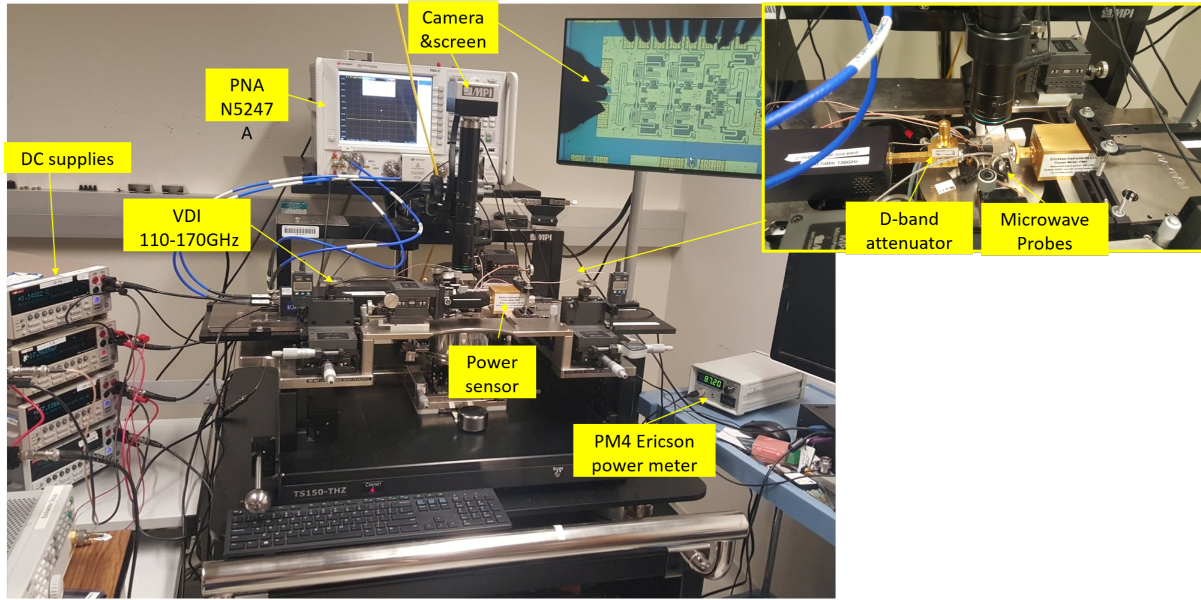

Figure 4.10: Power measurement setup.

Table 4.2: DC biases for power measurements.

$\mathbf{V_{CC1}}$	$\mathbf{V_{CC2}}$	$\mathbf{V_{CC3}}$	$\mathbf{V_{BB1}}$	$\mathbf{V_{BB2}}$	$\mathbf{V_{BB3}}$
2.5V	2.5V	1.5V	1.95V	1.4V	1.1V
$\mathbf{I_{CC1}}$	$\mathbf{I_{CC2}}$	$\mathbf{I_{CC3}}$	$\mathbf{I_{BB1}}$	$\mathbf{I_{BB2}}$	$\mathbf{I_{BB3}}$
130mA	56mA	34mA	5mA	2mA	1mA

Table 4.2 summarizes the DC bias condition. The RF input signal changes slightly the bias current and the base voltage is adjusted at each power sweep to keep a constant current. The output stage is biased at 130mA and 2.5V for V_{CC1}. Bias for the first stage was reduced (V_{CC3}=1.5V, I_{CC3}=32mA) for increased PAE. Fig. 4.11 shows the large-signal power measurements and simulation results. There is a good agreement between measurements and simulations. At 140GHz, the amplifier has a peak saturated output power of 20.5dBm with 20.8% PAE and 15dB associated gain. At 1-dB gain compression, the amplifier has 17dBm output power and 9.7% PAE. Over a 125-150GHz bandwidth, the saturated output power is within 2dB of its 140GHz maximum, with an associated PAE greater than 14.3% as shown in Fig. 4.12.

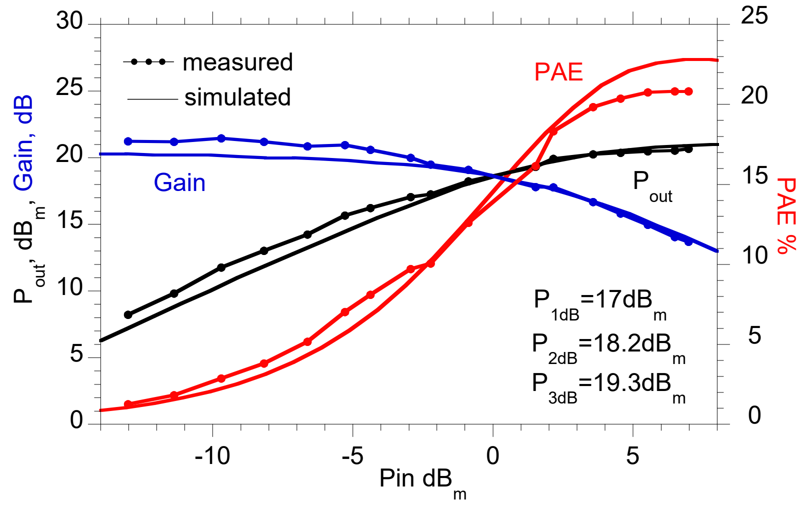

Figure 4.11: Measured and simulated output power, PAE, and gain versus the input power at 140GHz.

4.3.7 Summary

A high-efficiency D-band power amplifier has been demonstrated in 250nm InP HBT technology. The compact amplifier utilizes 3 gain stages and a low-loss output power combiner. Capacitive grounding linearizes the common-base stages, providing increased efficiency at the 1dB gain-compression point, yet this linearized stage design maintains gain comparable to a common emitter stage. The amplifier shows 112mW saturated output power with 20.8% PAE. The amplifier provides wideband operation with 43GHz small-signal BW and low DC power consumption. Table 4.3 compares the performance of the proposed amplifiers to the state-of-the-art D-band amplifiers: PAE is improved 1.6:1 for amplifiers of comparable saturated output power. There is other work showing high efficiency [32] but the power and gain are limited.

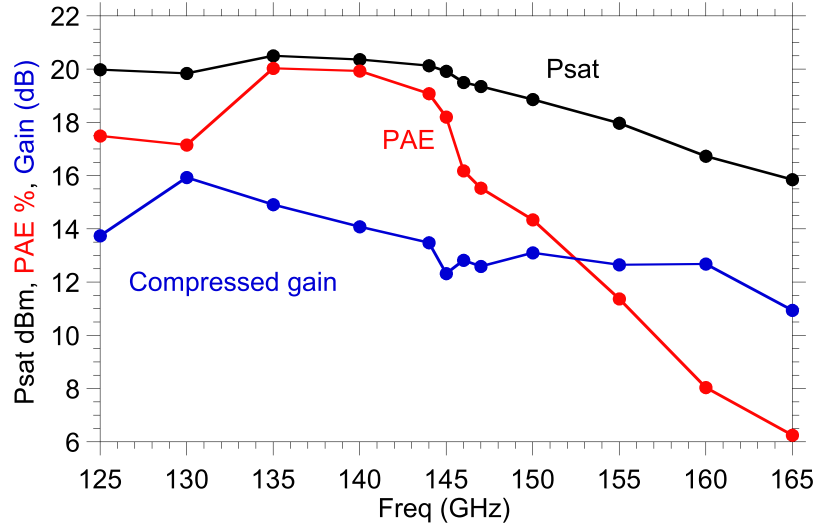

Figure 4.12: Measured saturated output power, PAE and the compressed gain versus frequency.

Table 4.3: Comparison between state-of-the-art D-band amplifiers.

Ref	Tech.	Freq (GHz)	P_{sat} (dBm)	BW_{3dB} GHz	Gain at P_{sat} (dB)	Peak PAE %	P_{sat}/Area mW/P mm^2
[33]	40nm CMOS	140	14.8	17	13	8.9	88.8
[34]	130-nm SiGe HBT	155-180	18.0	25	23.5	4.0	74.2
[35]	130-nm SiGe HBT	112-142	17	16	29	13	47.2
[36]	130-nm SiGe HBT	131-180	14	49	22	5.7	52.3
[24]	250-nm InP HBT	110-150	23.2-24.0	32.7	14-16	5.8-7.0	134
[37]	250-nm InP HBT	115-150	21-21.8	34.8	15-17.5	8.2-10.5	205
This work	250-nm InP HBT	125-150	18.9-20.5	43	12.3-15.9	14.3-20.8	162

4.4 131GHz Power Amplifier with 17.8%PAE and 200mW Output Power

In this design, we report a compact and high-efficiency D-band power amplifier in 250nm InP HBT technology. A compact and low loss 8:1 transmission line power combiner is demonstrated. The three-stage power amplifier combines 8 capacitively linearized common-base power cells. The amplifier has 23dBm peak power with 17.8% power added efficiency (PAE) and 16.5dB associated large-signal gain at 131GHz. At 131GHz, the small-signal gain is 21.9dB. The small-signal 3dB-bandwidth is 125.8-145.8GHz. Over the 127-151GHz bandwidth, the saturated output power is greater than 22.3dBm with greater than 15% associated PAE. The amplifier occupies 1.34mm^2 die area and consumes 1.1W DC power. This result demonstrates a record PAE.

4.4.1 Power and Driver Cells Design

Fig. 4.13 shows the block diagram of the power amplifier. The amplifier has three stages. The output stage combines eight power cells. Each two power cells are combined and driven by a single driver stage. We did not scale the second driver for design reuse.

In Section 4.3, we did a design comparison between the common emitter (CE) and capacitively degenerated common base (CB) stages [28], the latter using a significant capacitive reactance between the base and ground, reducing the gain (Fig. 4.14a). Under optimum load termination for maximum saturated output power, and independent of the value of the base capacitive reactance, the saturated (peak) PAE of the CB stage is identical to that of the CE stage [28]. However, decreasing the base capacitance of the CB reduces the fractional variation of the input impedance $Z_{in} \cong kT/qI_E + (\tau_b + \tau_c)/C_E$ with variations of the emitter current I_E over the RF signal cycle. This linearizes the

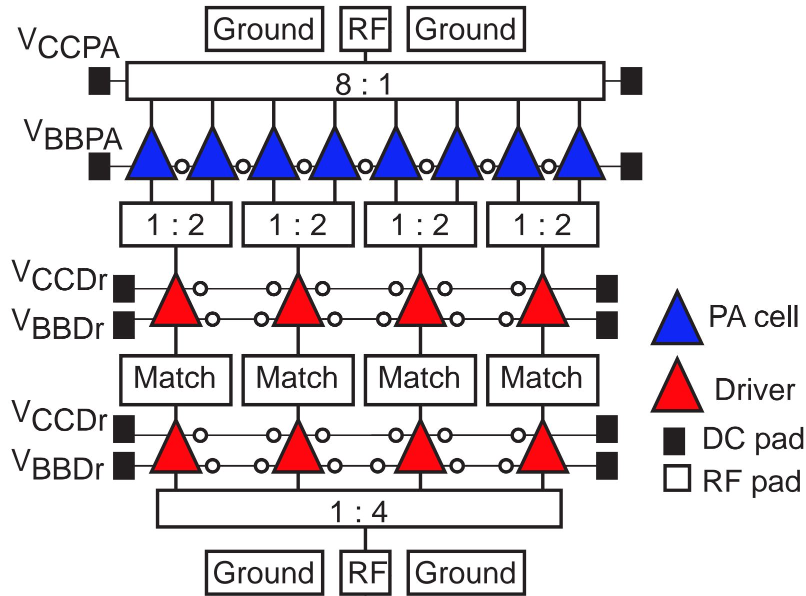

Figure 4.13: Amplifier block diagram.

stage and thus increases the output power and PAE at 1dB gain compression. The base capacitive reactance also improves the CB stability factor. The external base resistance provides stable control of the DC collector bias current with only a slight increase in DC power. The driver and power cells are similar to [28]; two power cells, each having 4 emitter fingers of 6μm length, share a common shunt inductor that tunes the transistor collector-base capacitances. Once C_{CB} is shunt-tuned, each 4x6μm cell requires a 50Ω load for optimum PAE. To sustain high PAE, each pair of output stages is driven by a stage having 4 emitter fingers of 6μm length.

The two cascaded driver stages (Fig. 4.14b) have a similar design. The input and output tuning networks are stagger-tuned to broaden the amplifier bandwidth. For increased gain, these stages use a larger base capacitance than the output stage. To reduce design effort, the first stage uses the same 4x6μm transistor cell as the second stage; overall amplifier PAE could have been slightly improved by using smaller transistors, with

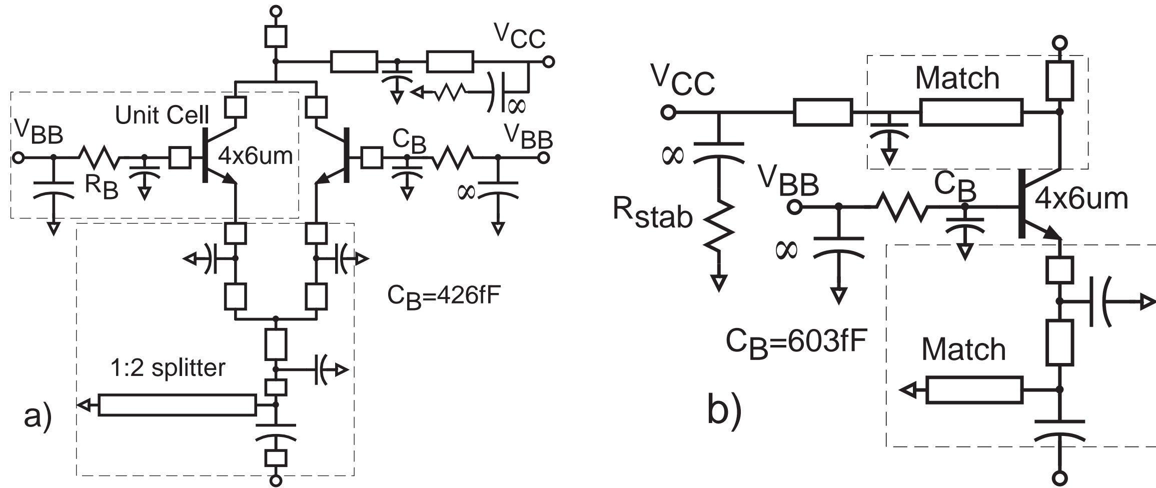

Figure 4.14: Schematic diagram of: a) Two combined power amplifier cells. The pair of power cells are driven by a single driver cell. b) Driver cell with input and output matching networks.

a correspondingly smaller DC bias current, in the first stage. MIM capacitors isolate DC bias between stages. All matching circuits and interconnects are simulated by ADS momentum and verified by HFSS.

4.4.2 Low Loss Transmission Line Combiner

The output power combiner must have a low loss for high PAE while being compact for small die areas. Wilkinson combiners [24] are broadband, but an 8:1 Wilkinson combiner requires 14 transmission-lines, each having $\lambda/4$ length and Z_0=71Ω. This requires a substantial die area. The high-impedance lines are narrow, limiting the maximum current. Losses are high because the signal must propagate through three cascaded narrow and hence lossy $\lambda/4$ lines. At the expense of narrower bandwidth, abandoning the Wilkinson design permits the transmission-line combiner to be designed for less loss and a smaller die. In [28], we demonstrated a 4:1 combiner with a low simulated loss of 0.92dB including shunt inductive tuning of C_{CB} but not including probe pad losses. Here, the combining

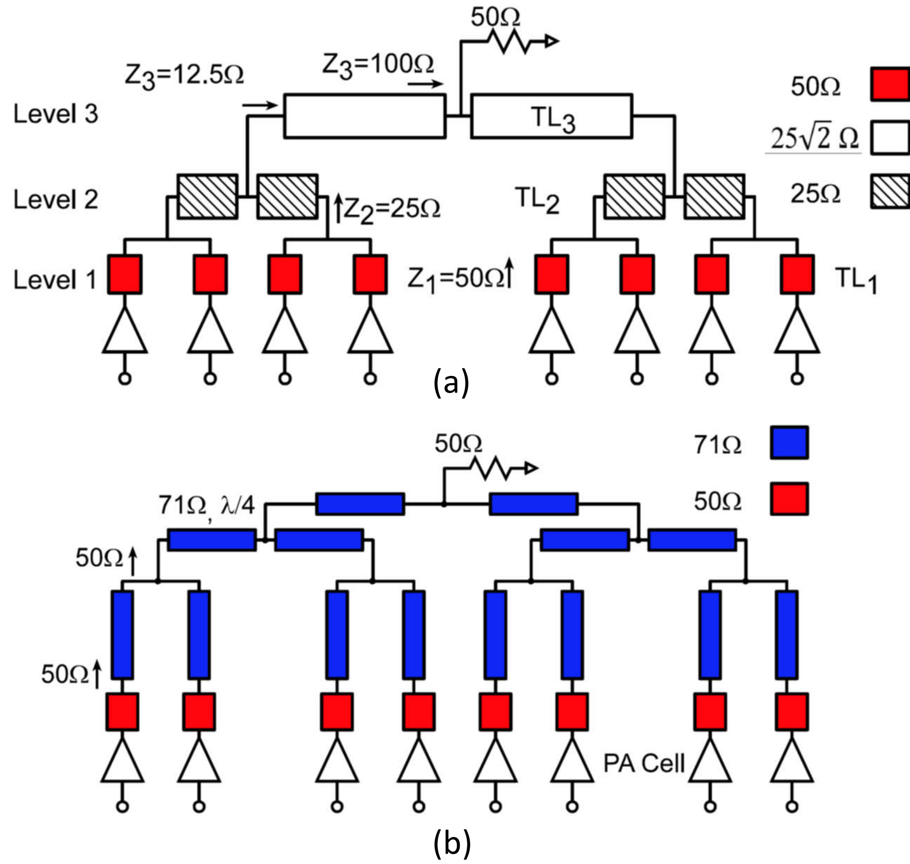

Figure 4.15: a) Proposed 8:1 transmission-line combiner for 50Ω load. b) an 8:1 Wilkinson combiner (with bridging resistors omitted).

ratio is increased to 8:1, yet low loss is maintained, 0.98dB simulated including shunt inductive tuning of C_{CB} but without probe pad losses. The resulting amplifier has nearly 2:1 greater output power than [28] yet maintains a similar high PAE.

Fig. 4.15a shows the combiner designed for 50Ω load without including the shunt inductive lines tuning C_{CB}. For the first combining level, short 50Ω transmission line sections (TL_1) combine the outputs of two 4x6μm cells. The required load impedance for each cell (Z_1) is 50Ω while the required load impedance (Z_2) for two parallel cells combined by TL_1 is 25Ω. The impedance transformation does not depend on the lengths

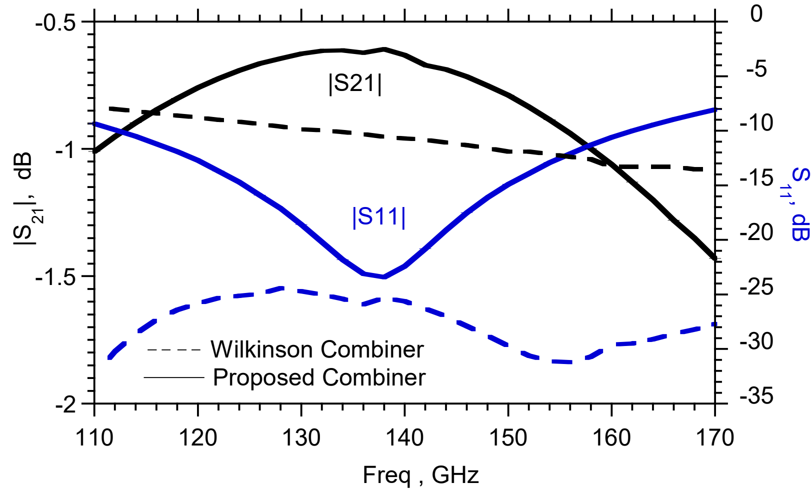

Figure 4.16: Simulations comparing the insertion losses and input reflection coefficients of the two designs.

of TL_1 and TL_2, hence these lengths are minimized for the smallest losses. Four combined cells require a load impedance (Z_3) of 12.5Ω, this is achieved by a $\lambda/4$ transmission line (TL_3) having $25\sqrt{2}\Omega$ characteristic impedance. Die area is reduced because only two $\lambda/4$ lines are required. Losses are reduced because TL_3 is wide, and because the signal passes through only a single $\lambda/4$ line, though these improvements are slightly offset by the increased loss associated with the high VSWR on TL_3. The wide lines permit high currents. In simulations (Fig. 4.16), the proposed 8:1 combiner designed for 50Ω load, without shunt elements, has a loss of 0.63dB at 140GHz, compared to 0.96dB for the 8:1 Wilkinson combiner, without shunt elements (Fig. 4.15b). The loss remains smaller than that of the Wilkinson over a 47.5GHz bandwidth.

The power amplifier is designed to be packaged. A dense array of through-substrate vias (TSVs) provides a low inductance connection between the ground planes on the top and bottom surfaces of the IC substrate, as only the latter connects to the package ground system. The TSVs also suppress dielectric substrate modes. The RF I/O pads are

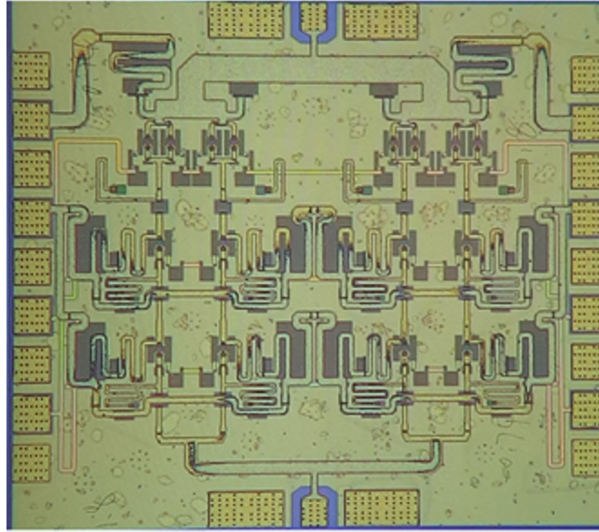

Figure 4.17: Chip micrograph of the PA (1.23mm 1.09mm) including the pads.

relatively large, 55μmx57.5μm, and use all wiring planes to improve pad adhesion during wire bonding. The pad impedance was simulated in HFSS and the line parameters of the output combiner were then adjusted to compensate for the pad parasitics. The final combiner parameters are: TL_1 (61Ω, 7.2^o), TL_2 (23Ω, 17°), and TL_3 (17Ω, 90°). The total combiner loss including the pad is 1.3dB (0.98dB for series TL and shunt tuning inductors, and 0.32dB for the pad).

4.4.3 S-parameters Measurements

Fig. 4.17 shows the IC micrograph and S-parameters are measured using an HP network analyzer with VDI 110-170GHz frequency extenders and 140-220GHz GGB wafer probes with WR-5 to WR-6 waveguide adapters (setup in Fig. 4.18). To avoid driving the amplifier into gain compression, an attenuator is added to port 1 of the frequency extender output. This attenuation degrades the network analyzer directivity, producing the small ripples observed in the $| S_{11}|$ measurement.

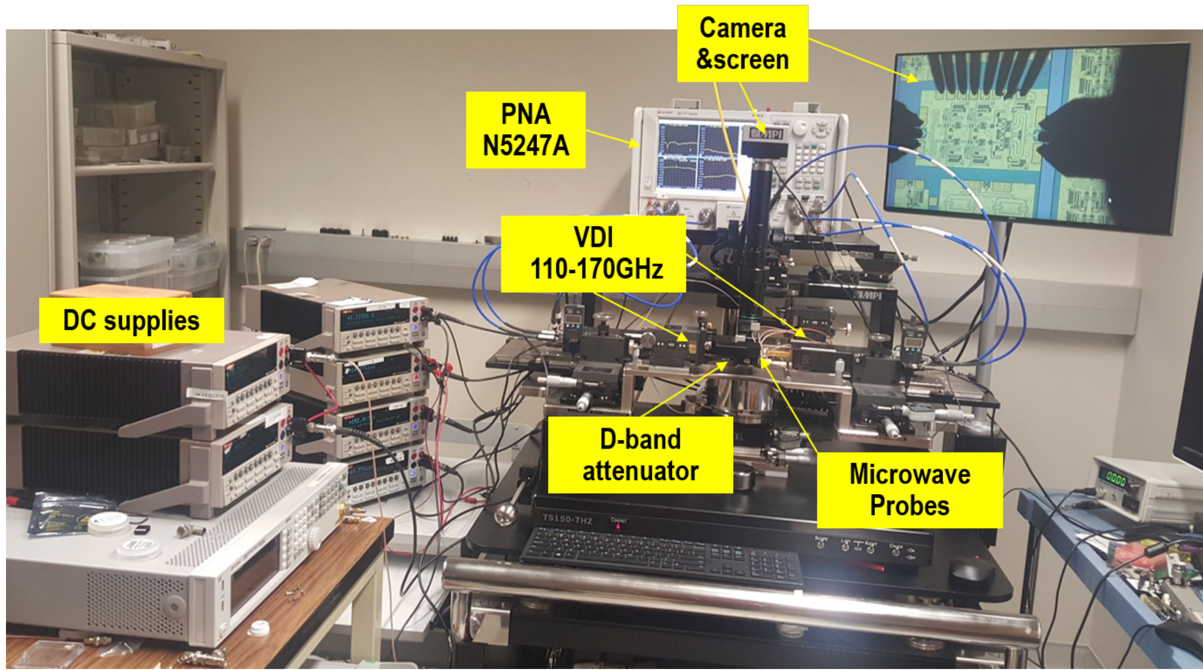

Figure 4.18: S-parameters measurements setup.

The analyzer was calibrated to the probe tips using SOLT standards on an external CS-15 calibration substrate. DC bias was provided to the DC pads on both sides of the IC die to minimize IR drops. The DC probes have bypass capacitors mounted near the probe tips to suppress supply-induced oscillations. Identical bias conditions are set for the two driver stages (V_{CCDr}=2.43V, and V_{BBDr}=1.5V, I_{CCDr}=221mA, I_{BBDr}=8.6mA) while the output stage is separately biased at (V_{CCPA}=2.43V, V_{BBPA}=1.5V, I_{CCPA}=221mA, and I_{BBPA}=9mA). The peak small signal gain (Fig. 4.19) is 22.8dB at 128.3GHz while $|S_{21}|$ is flat within 3dB between 125.8-145.8GHz. The amplifier is designed for maximum saturated output power which differs, by necessity, from gain matching, resulting in poor $|S_{22}|$.

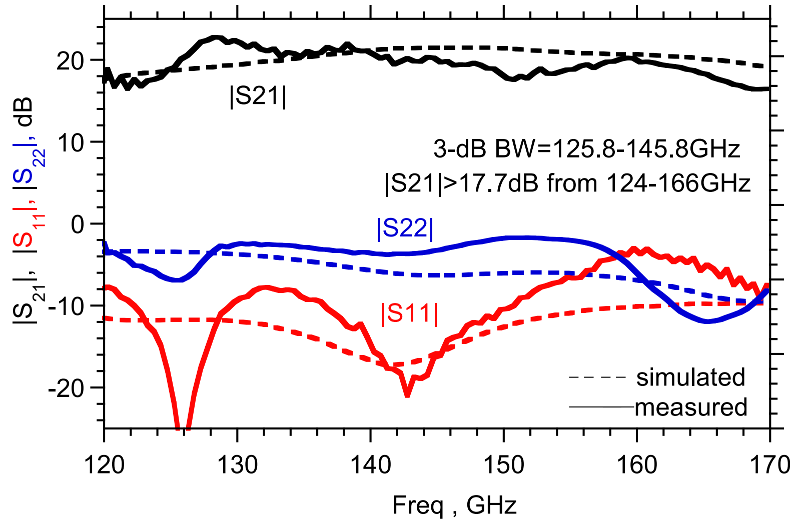

Figure 4.19: Measured (solid) and simulated (dashed) S-parameters.

4.4.4 Power Measurements

Large-signal power characteristics were measured on the 3-mil-thick die without any external cooling (setup in Fig. 4.18). The input signal source is a 110-170GHz VDI frequency extender, with ∼10dBm output power, followed by a variable attenuator. The output is measured by an Erickson power meter. Losses of the D-band probes were separately measured, and the reported data is corrected for the probe losses.

The driver stages have V_{CCDr}=2.43V, V_{BBDr}=1.41V, the total driver collector current I_{CCDr}=212mA, and the total driver base current is I_{BBDr}= 7.7mA. The output stage is biased separately, with V_{CCPA}=2.65V, V_{BBPA}=1.41V, the total collector current I_{CCPA}=219mA and the total base current I_{BBPA}=8mA. Fig. 4.21a shows the power measurements at 140GHz. At each RF drive level, the base bias voltages are adjusted to keep the collector bias currents constant, with values as stated above. At 140GHz, the saturated output power is 22.8dBm with 16.1dB associated gain and 16.7% PAE. The amplifier OP_{1dB} is 20.2dBm with PAE=9.4% and 20.3dB associated gain. Fig. 4.21b

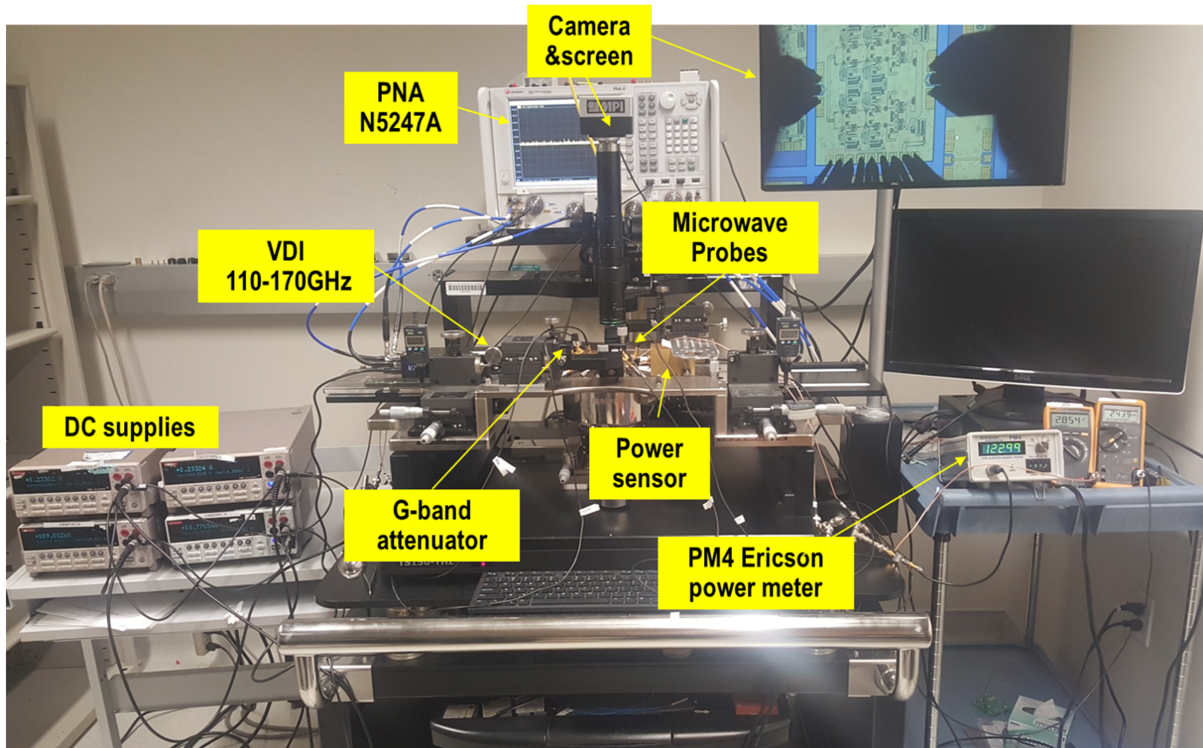

Figure 4.20: Power measurement setup.

shows the power measurement at different frequencies and Fig. 4.22 shows the peak PAE, the associated gain, and output power versus frequency. Over 127-165GHz, the saturated output power is within its 3dB of its maximum at 131GHz.

4.4.5 Summary

A high-efficiency and compact D-band power amplifier has been demonstrated in 250nm InP HBT technology. Eight power cells are combined with a compact and low-loss transmission line network. The number of power cells is doubled compared to [28], resulting in almost twice the output power while maintaining almost the same PAE. Capacitive grounding linearizes the common-base stages, providing increased efficiency at the 1dB gain-compression point. The three-stage amplifier shows 200mW saturated output power with 17.5% PAE at 130GHz. The saturated output power is 20-23dBm

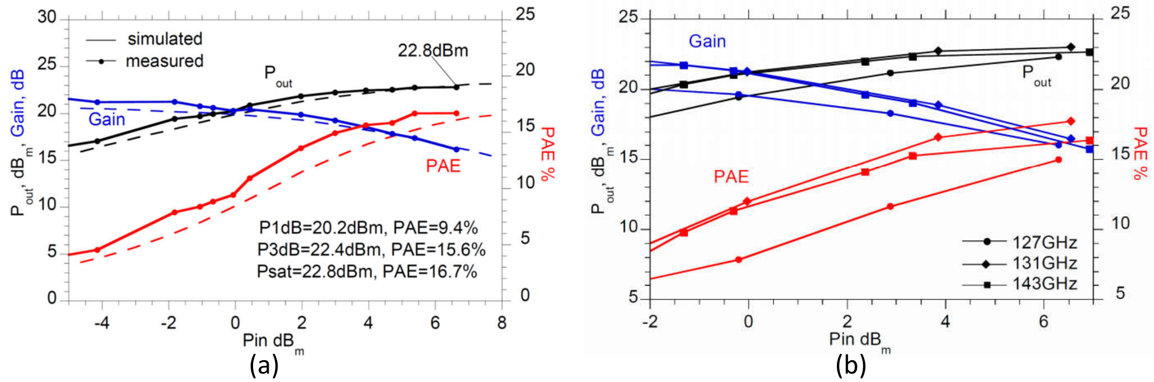

Figure 4.21: a) Measured and simulated output power, PAE, and gain versus the input power at 140GHz. b) Measured P_{out}, PAE, and gain versus the input power at 127, 131, and 143GHz.

Table 4.4: Comparison between state-of-the-art 130-140GHz amplifiers.

Ref	[38]	[39]	[24]	[28]	This work
Tech.	GaN	90-nm SiGe	250-nm InP HBT		
Freq, GHz	135	130	131	130	131
P_{sat}, dBm	23.7	21	23.8	19.8	23
BW_{3dB}, GHz	18	35	32.7	43	20
Gain at P_{sat} (dB)	25	-	16	15.9	16.5
Peak, PAE %	5.3%	-	6.9	17.1	17.8
Size (mm^2)	7.5	0.62	1.89	0.69	1.34
P_{DC} (W)	-	2.2	3.46	0.52	1.1
P_{sat}/Area mW/mm^2	31.2	202.9	126.4	138	149

from 125-165GHz. Drivers share the same V_{CC} and V_{BB} to reduce the number of pads. However, the PAE will increase by controlling each drivers supply independently or scaling the first driver. Table 4.4 shows the state-of-the-art 130GHz-140GHz band amplifiers and we compared the amplifiers' results around 131GHz. This work demonstrated a record PAE.

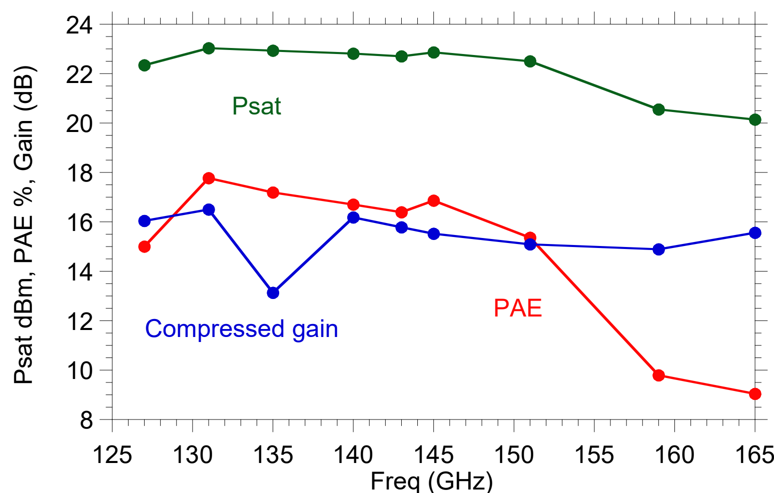

Figure 4.22: Measured saturated output power, PAE and the compressed gain versus frequency.

4.5 204GHz Stacked-Power Amplifiers

Here, we report stacked mm-wave power amplifiers designed by the 2-port technique presented in Chapter 3. Two power amplifiers are designed in 130-nm InP HBT to verify the technique. The first design (unit cell) biased at 436mW P_{DC} produces 34.6mW saturated output power with 5.8% PAE at 204GHz. The amplifier has a 13.9dB peak small-signal gain at 236GHz and 27 GHz 3-dB bandwidth. The chip size is 0.63mmx0.54mm including the pads. The second design combines two cells in parallel with an additional gain stage. The design consumes 1.18W P_{DC} and shows a 63mW saturated output power with 4.8%PAE at 204GHz. The amplifier has a 22.7dB peak small-signal gain at 230GHz and larger than 25GHz 3-dB bandwidth. The chip size is 0.7mmx1.3mm including the pads.

4.5.1 Two Cell Amplifier Design

Fig. 4.23a show the schematic of a 204 GHz design (Design 1) using a 3:1 stack. In this design, all the transistors (Q_1, Q_2, and Q_3) are divided into two clusters each is 4

fingers with 5μm emitter length. This will simplify the matching circuits and ballast resistors could be added to each cluster or less to prevent thermal stability problems. The input transistor is tuned for maximum gain, and the upper two transistors are tuned for maximum saturated output power. We followed the design procedures presented in Chapter 3. From the transistor design kit model, a large signal CB load-pull simulation was first performed to determine the required transistor terminal voltages and currents under efficient large-signal operation. The input, load, and common-lead impedances Z_{in}, Z_L, and Z_{common} were computed. Then we designed the interstage tuning network designs. The interstage matching circuits are designed by series TLs and shunt MIM caps. The output matching circuit is achieved by a shunt TL and series TL. Small value resistors are usually added in series with the bypass caps to avoid out-of-band instability. However, this resistance will degrade the output power significantly. In this design, a large resistance (R_{stab}) is added in parallel to the bypass cap. At lower frequencies, the resistance damps any out-of-band instability. However, the impedance of the cap dominates at the operating frequencies and the effect of the stability resistance is negligible on the output power. Unfortunately, this resistance draws a lot of DC power consumption lowering the PAE but without any impact on the output power.

4.5.2 Four-Cells Amplifier Design

Design 2 (schematic not shown) uses a transmission-line network to combine two cells of the 204 GHz Design-1 stages into a higher-power amplifier. Design 2 also includes one more cell acting as a driver stage. Therefore, less than 10mW is required to drive the amplifier into saturation. Wiggling in the routing between the driver and the amplifier stage is done for a compact area design.

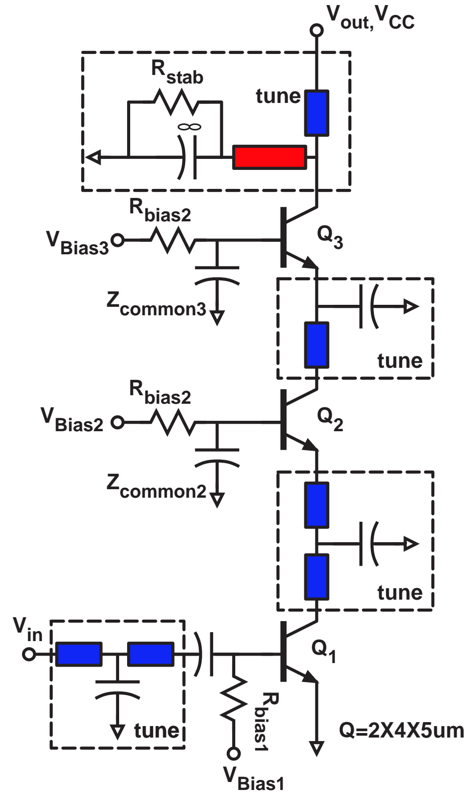

Figure 4.23: Simplified schematic diagrams of a 204GHz, 3:1 series-connected stack with gain-matching on Q_1 and power-matching on Q_2 and Q_3.

4.5.3 S-Parameters Measurements

Fig. 4.24 shows IC photographs. S-parameters were measured using an HP vector network analyzer with Oleson 220-325GHz frequency extenders and GGB wafer probes. Calibration used LRRM standards on an external substrate. Design 1 (Fig. 4.25a) shows 13.9 dB peak gain at 236 GHz and the 3-dB BW extends from 220GHz up to 247GHz. S_{11} is better than -10dB across the whole band. S_{22} is better than 6dB from 220GHz up to 240GHz. The reverse isolation (S_{12}) is better than -34dB across the whole band. It is noted that the small-signal gains of the measured designs are higher than the simulations. It means that the common lead impedances (Z_{common}) have more parasitic capacitances after the fabrication. This can be justified by the limited accuracy of the EM

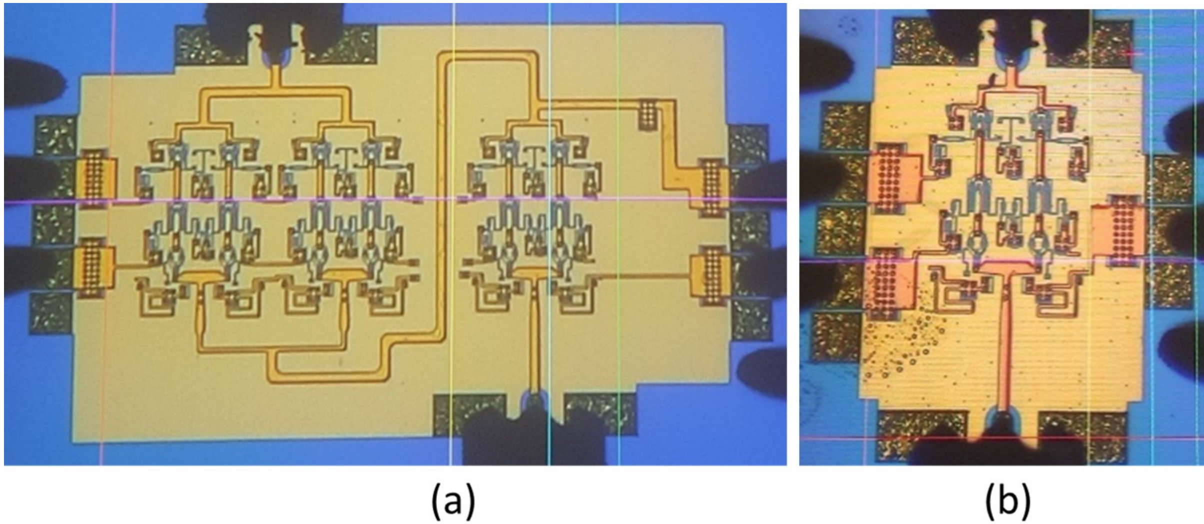

Figure 4.24: (a) Die photo of design 1, and (b) Design 2, with 2:1 transmission-line combining. The die areas are 0.63 mm × 0.54 mm, and 0.7 mm × 1.3 mm respectively.

simulation or the transistor model misses some parasitic inductance. Stacked transistors with parasitic capacitances at their bases show a higher small-signal gain at the expense of the maximum saturated power. Design 2 (Fig. 4.25b) has a 22.7 dB peak gain at 230 GHz and the 3-dB BW extends from below 220GHz up to 245GHz. S_{11} is better than -10dB across the whole band. S_{22} is better than -6dB below 236GHz. The reverse isolation (S_{12}) is better than -42dB while the simulated one (not shown) is better than -85dB. The reverse isolation is critical in high gain amplifiers to avoid stability problems.

4.5.4 Power Measurements

Large signal PA saturation characteristics were measured on-wafer using VDI ∼204GHz frequency multipliers, driven by microwave synthesizers, GGB 220-330GHz probes, and an Erickson THz power meter. For the 204GHz measurements, the probe losses were determined by a probe-probe through measurement.

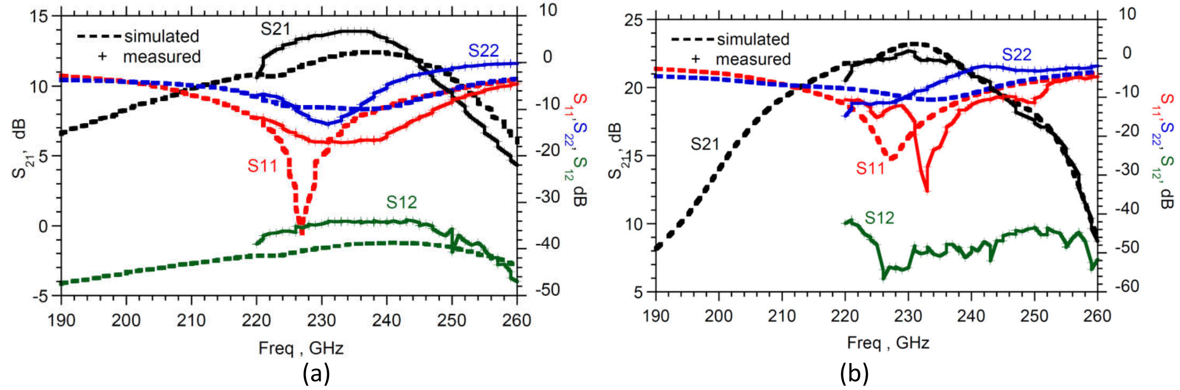

Figure 4.25: Measured and simulated S-parameters of a) Design 1 a) Design 2.

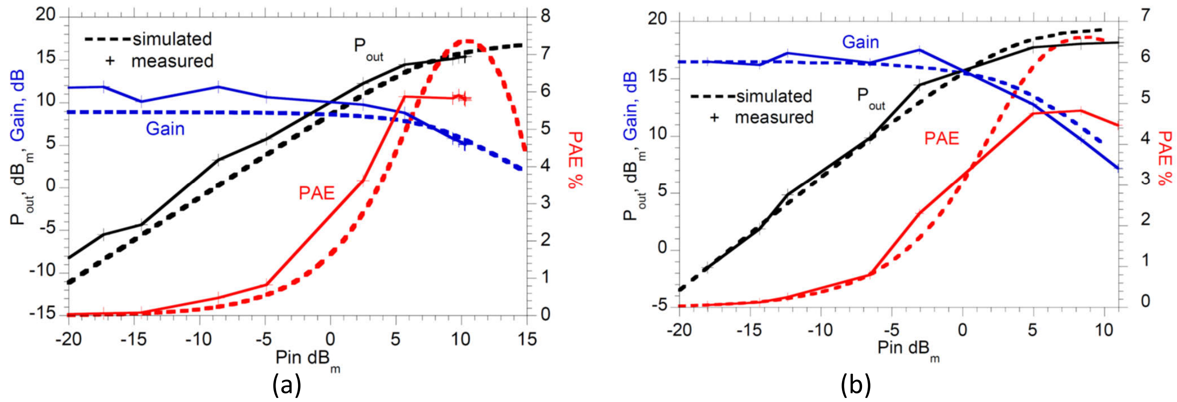

Figure 4.26: a) Measured and simulated output power, PAE, and gain for Design 1. b) Measured and simulated output power, PAE, and gain for Design 2.

Power testing bias conditions for Design 1, were V_{CC}=5.9 V, V_{Bias3}=4.9 V, and V_{Bias2}=2.5 V. The collector current is 65mA where the total I_C current (including the base currents) is 74 mA. For Design 2, V_{CC}=5.9 V, V_{Bias3}=4.9 V, and V_{Bias2} = 2.5 V, and the total collector for single cell is 61mA. The total I_C current is 210mA for the three cells where two of them are connected in parallel and another one acts as a pre-driver stage.

For Design 1 (Fig. 4.26a), at 204GHz, the saturated output power is 15.1 dBm, less than 1 dB below simulation. The DC currents are monitored at each sweep point to

report any DC power increase due to the RF input power signal. However, it is noted that there is less than 1% increase in the DC power. The amplifier has a peak PAE of 5.8% at 15.1dBm and 5.8dB compressed gain.

For Design 2 (Fig. 4.26b), the saturated output power is 18 dBm at 9.7dB compressed gain, and it matches the simulation well (less than 1dB difference). The DC currents are also recorded at each sweep point with less than 1% variations. The amplifier shows a 4.8% maximum PAE. The DC power of the driver is included in PAE calculations.

4.6 325GHz Stacked Power Amplifier with 8.6-13.6 mW Output Power

Desiging amplifiers working above 300GHz is quite challenging. Ref [40], [41], [42], [43], [44] show some of the amplifiers working above 300GHz. Here we present two 325 GHz series-connected power amplifiers (PAs) using 130 nm InP HBT technology. The unit cell, using two series-connected transistors, produces 8.6 mW at 325 GHz and consumes 243 mW DC power. The PA has a 4.3 dB compressed gain and 2.2% power added efficiency (PAE). Two of these cells are then power-combined, and two further cells are used as driver stages, to form the second design, which produces 11.36 mW at 325 GHz with 9.4 dB compressed gain and 1.09% PAE. The peak small-signal gain is 16.6 dB at 325 GHz, and the 3-dB bandwidth is 9 GHz. The total power consumed is 1.12 W and the dimensions including the pads are 0.98 mm x 0.98 mm.

4.6.1 Single Cell Power Amplifier Design

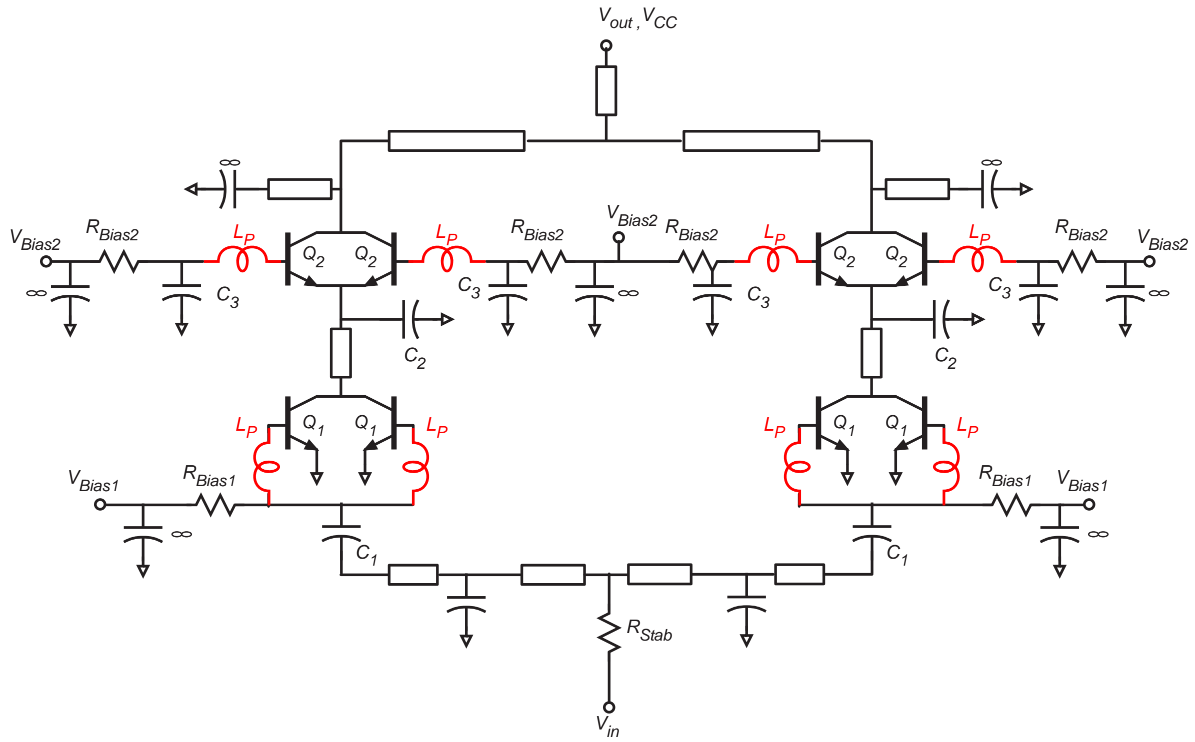

Figure 4.27: PA unit cell (two stacked HBTs with matching circuits). Q_1 and Q_2 are two finger transistors each 5μm emitter length. The inductors (red) are added to represent the base inductance model and are not real inductors.

The amplifier is designed using 130 nm InP HBT technology (Section. 4.2). The amplifier unit cell (Fig. 4.27) has two stacked 8-finger transistors, each of 5 μm emitter finger length. The transistors are biased at 1.3 mA/μm, with current under RF drive then varying from zero to 2.6 mA/μm. Microstrip lines serve as interconnects and for impedance-matching; these use a metal 1 ground plane and metal 3 signal lines.

The power cell has input matching to 50Ω, output tuning providing the optimum large-signal loadline to Q_2 given an external 50Ω load, a capacitor C_3 controlling the RF voltage distribution between the two transistors, and an interstage network ensuring equal RF currents in the two transistors. Resistors provide out-of-band stabilization. Amplifiers are designed according to the procedures of Chapter 3. Interconnects, matching, power

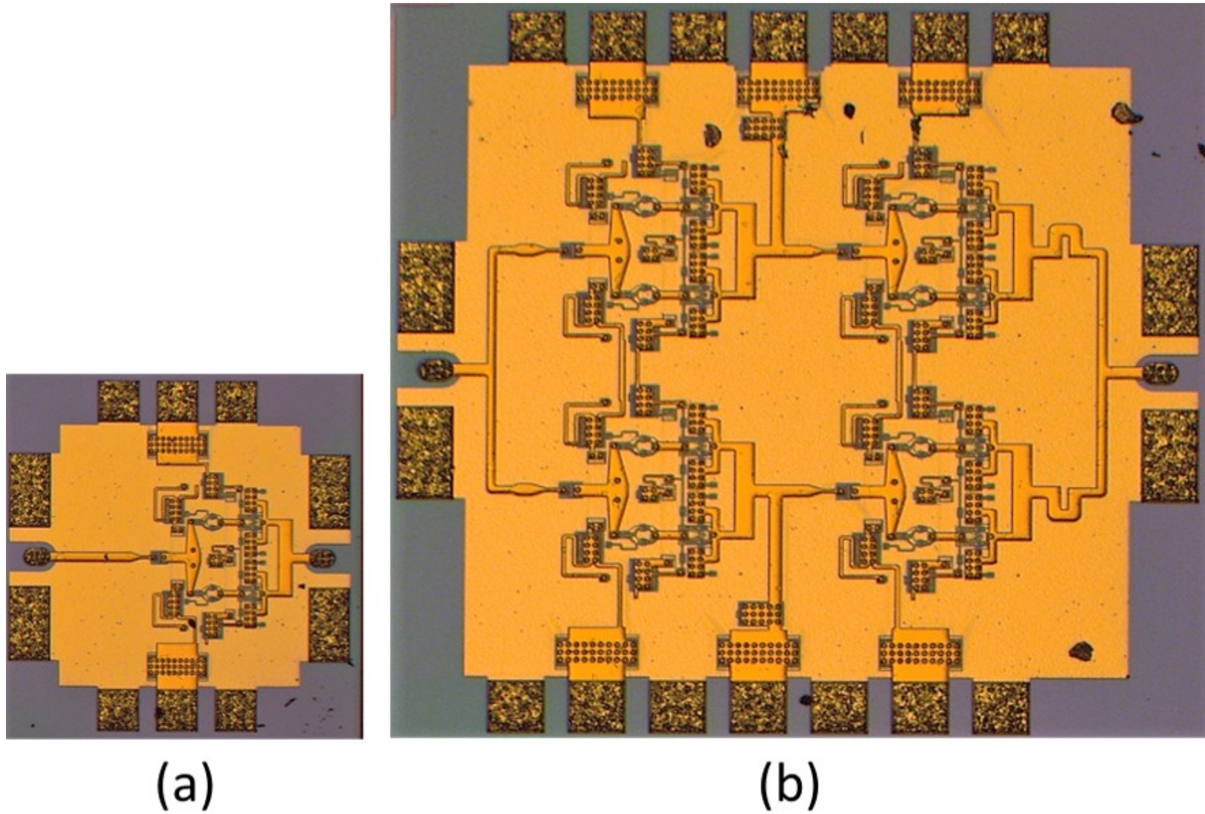

Figure 4.28: PA unit cell (Chip micrograph of the power amplifiers: a) Design #1 (dimensions = 600 μm 585 μm). b) Design #2 (dimensions = 0.98 mm 1 mm).

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supply lines, and MIM capacitors are simulated using ADS momentum, a 2.5D tool.

4.6.2 2:1 Power Combined Design

For increased output power, transmission-lines combine the outputs of two-unit cells and match these to 50Ω (Fig. 4.28 b). Two additional unit cells serve as predrivers. These increase the IC gain and provide the necessary input power for the final stage, at the expense of increasing the total power dissipation. Quarter wave transmission lines provide DC bias to the driver stages; DC bias pads have RC bypass networks to prevent resonance with external probe inductances.

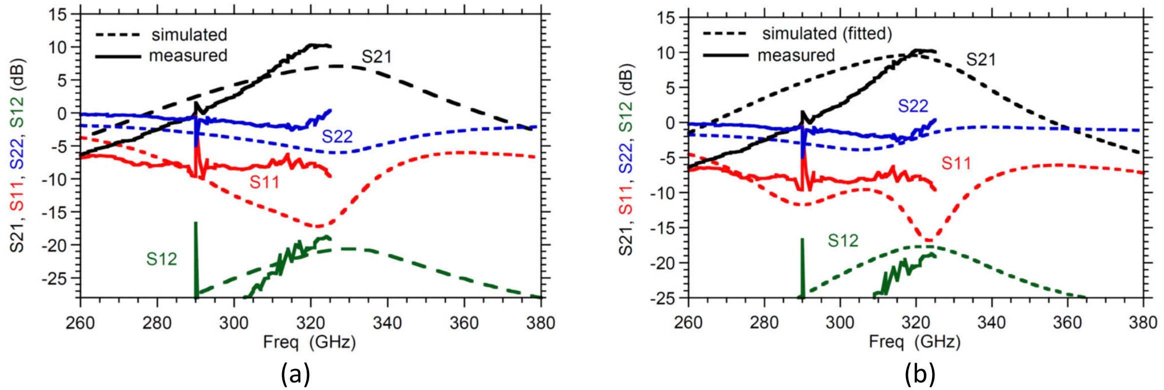

Figure 4.29: PA unit cell (a) Simulated and measured s-parameters of the unit-cell design. b) Comparison of measured and resimulated s-parameters of the unit-cell design assuming an additional 3.5 pH base feed inductance per two-finger each 5 μm emitter length HBT.

4.6.3 Measurement Results

Fig. 4.28 shows the IC photographs. The output (V_{CC}) is biased at 3.6V and the DC collector current, equal to the total I_C DC current, is 68mA. The base bias voltage of the Q_2 is 2.3V. The collector to emitter voltage (V_{CE}) of Q_1 is smaller than the V_{CE} of the common base transistors (Q_2) to reduce the total power dissipation and optimize the PAE. Separate bias resistors are provided to the two parallel common emitter transistors, preventing thermal competition for the DC bias current. 220-325 GHz S-parameters are measured using an HP vector network analyzer with Oleson mm-wave frequency extenders and waveguide-coupled wafer probes. Calibration is to the probe tips using an external LRRM calibration standard substrate. Fig. 4.29a compares the simulated and measured S-parameters of the unit cell. The measured peak gain is 10 dB at 325 GHz while the simulated peak gain is 5.5 dB at 330 GHz. The spikes at ∼290GHz occur due to the frequency extension modules and they are not related to the circuit itself.

For power measurements, a 330 GHz VDI frequency multiplier generates the input signal, and an Erickson THz power meter measures the output power. Wafer probe

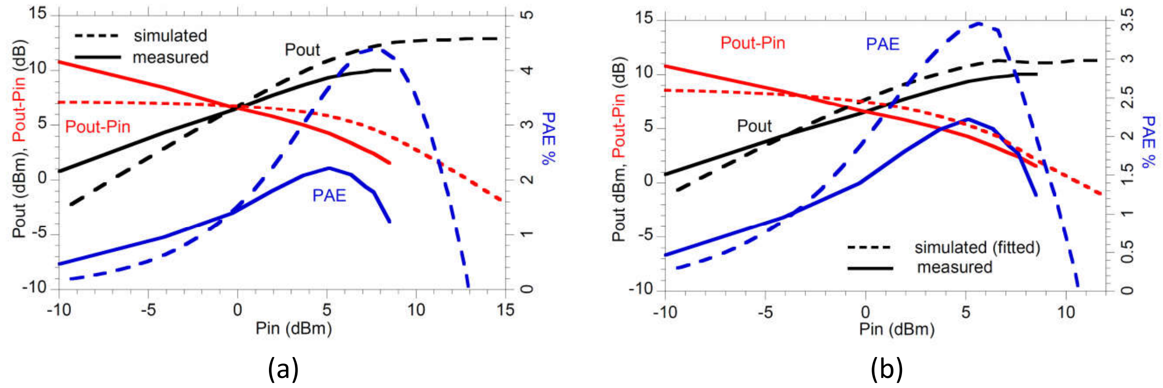

Figure 4.30: a) Simulated and measured power transfer characteristics at 325GHz of the unit-cell design. b) Comparison of measured and resimulated power transfer characteristics at 325GHz of the unit-cell design assuming an additional 3.5 pH base feed inductance per two-finger each 5 μm emitter length HBT.

losses were determined by a through measurement and were de-embedded from the power measurements. Fig. 4.30a shows the simulated and measured output power, the PAE, and the gain, as a function of the input power at 325 GHz. The PA has 9.4 dBm saturated output power at 4.3 dB compressed gain and 2.2% PAE.

There is a considerable discrepancy between the simulated and measured small-signal and power characteristics of the unit cell power amplifier. The HBT model, established from RF characterization of single-finger devices, includes 2.7pH per 5 μm emitter finger. In a 2-finger power cell, the aggregate inductance of the base feed network is considerably larger. Although the base feed network and its parasitics were modeled during design, this is a complex network without an underlying ground plane providing a clear path for the ground-return currents; modeling of the interconnect inductance within the multifinger HBT is therefore difficult. To attempt to resolve the difference between measurement and simulation, the amplifier was re-simulated with a variable base feed inductance for all multifinger HBTs. A 3.5 pH (L_P in Fig. 4.27) inductance provides the best fit between measurement and simulation for both the small-signal (Fig. 4.29b) and power data (Fig.

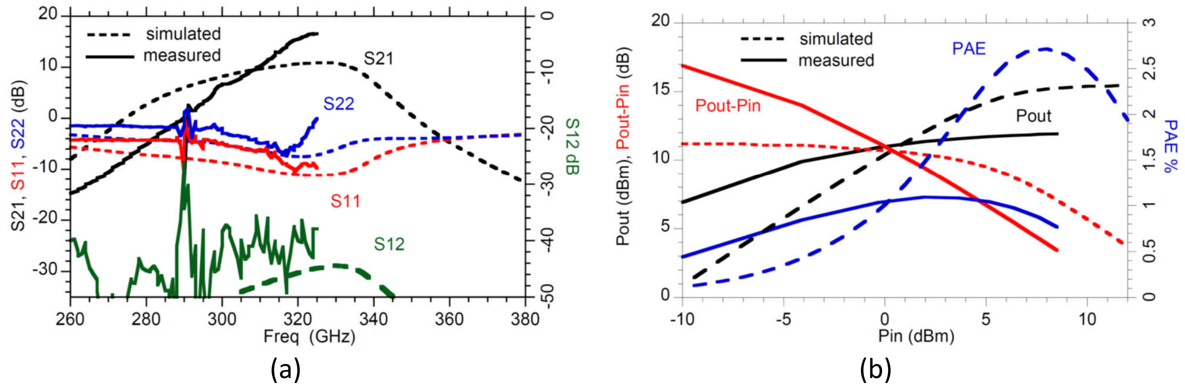

Figure 4.31: a) Simulated and measured s-parameters of the 2:1 power-combined design. b) Simulated and measured power transfer characteristics of the 2:1 power–combined design.

4.30b). This inductance is approximately that of a 5 μm length conductor.

Fig. 4.28b shows the micrograph of the second design. The PA combines two-unit cells using transmission lines. The bias conditions of all the cells are identical and similar to design 1 (V_{CC}=3.6 V, V_{Bias2}=2.3 V) and the total DC current is 290 mA. Fig. 4.31a shows the measured and simulated S-parameters. The measured peak small-signal gain is 16.6dB at 325 GHz, while the simulated peak gain is 8.25 dB at 330 GHz. The measured 3-dB bandwidth extends from 316 GHz to beyond the 325 GHz measurement limit of the network analyzer's frequency converters. Fig. 4.31b shows the power transfer characteristics at 325GHz. The amplifier has a 11.4 dBm saturated output power at 9.4 dB associated gain and 1.09% PAE. The input-output power characteristics are measured at different frequencies for the single-cell (Fig. 4.32a) and the 2:1 power combined amplifiers (Fig. 4.32b).

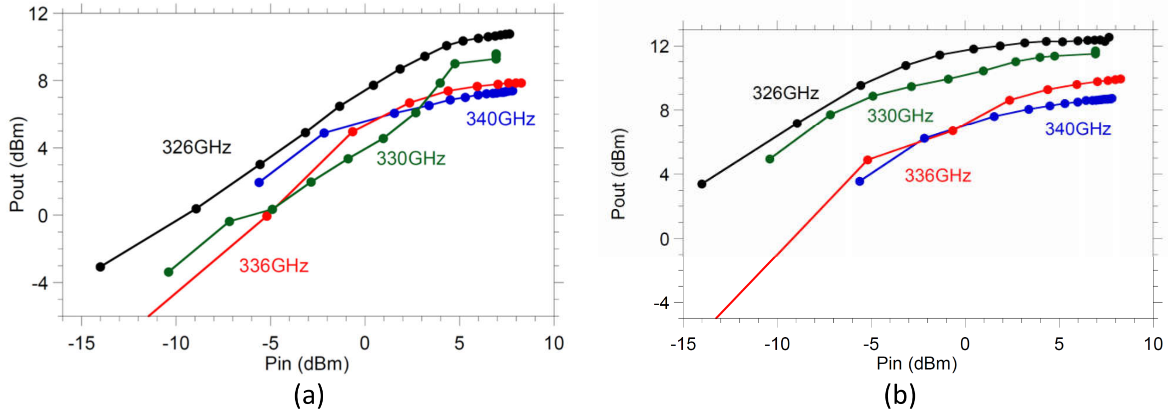

Figure 4.32: a) Measured output power at different frequencies versus the input power for design#1. b) Measured output power at different frequencies versus the input power for design#2.

4.7 Summary and Conclusion

This chapter demonstrated many mm-wave amplifiers (140GHz, 220GHz, and 325GHz) designed in InP HBT technologies (130nm and 250nm). The amplifiers demonstrated record efficiency with moderate output power. Designing millimeter-wave power amplifiers demand a tremendous amount of careful EM simulations and understanding the impact of the parasitics. Amplifier design has lots of degrees of freedom from unit cell selection, power combining technique, or biasing... etc. Analyzing the available solution and making the right selection is the key factor for the record results. Modern technologies with higher f_{max}, such as InP, definitely help in pushing the limit and work at higher frequencies.

Chapter 5

210GHz Transmitter for MIMO Demonstration

5.1 Motivation

As we mentioned in Chapter 1, there is an increasing demand for high data rate communication systems. We can achieve a high data rate by exploiting higher frequency bands. The other way is to build MIMO arrays to support multiple beams and increase the data rate. Here, we are considering the transmitter design that could be used in those MIMO arrays.

There are several techniques to design transmitters above 200GHz based on the f_{max} of the used technology. Technologies with a low f_{max} usually use frequency-multiplier-based transmitters since it is challenging to build power amplifiers at high frequencies [45] and [46]. The main limitation of this approach is that the output powers are very limited, which severely limits the communication transmission range. Recent CMOS work shows decent output power [47] at 200GHz using 65nm CMOS technologies. However, it is

still a discrete amplifier and has not been integrated into a full transmitter yet. SiGe technologies offer higher f_{max}, which makes the power amplifier design feasible. Ref [48], [49], and [50] show packaged transmitters above 200GHz with moderate output powers. InP technologies offer superior power amplifiers above 200GHz [13], [31], and [51]. This permits designing integrated systems with moderate output power at mm-wave frequencies [2], [52], and [53].

In this chapter, we will present 210GHz transmitters designed in 250nm InP HBT technology. We will present different variants for the transmitter design: 1) A 210GHz transmitter with ∼2dBm output power. 2) A similar 210GHz transmitter with a simulated ∼18dBm output power.3) A 2x2 210GHz transmitter array with a Quartz antenna. We will briefly present the transmitter's key components with a great emphasis on the power amplifier design.

5.2 210GHz Transmitter with ∼ 2dBm Output Power

Fig. 5.1 shows the transmitter[1] layout, chip micrograph, and block diagram. An inverted microstrip technique is used in the transmitter. That is why the chip micrograph does not show the circuit details. This is a single channel phased array transmitter element with a fully differential operation. The transmitter uses a direct conversion technique where the IF signal is upconverted to 210GHz by an active mixer. A frequency multiplier chain is used for the local oscillator. The output of the chain goes to a phase shifter to generate the proper phase. Then the phase shifter's output goes to a 90° coupler, drivers, and IQ mixer. To reduce the risk, this transmitter version does not include a high output power amplifier.

[1]Prof. Munkyo Seo is the design leader for this transmitter.

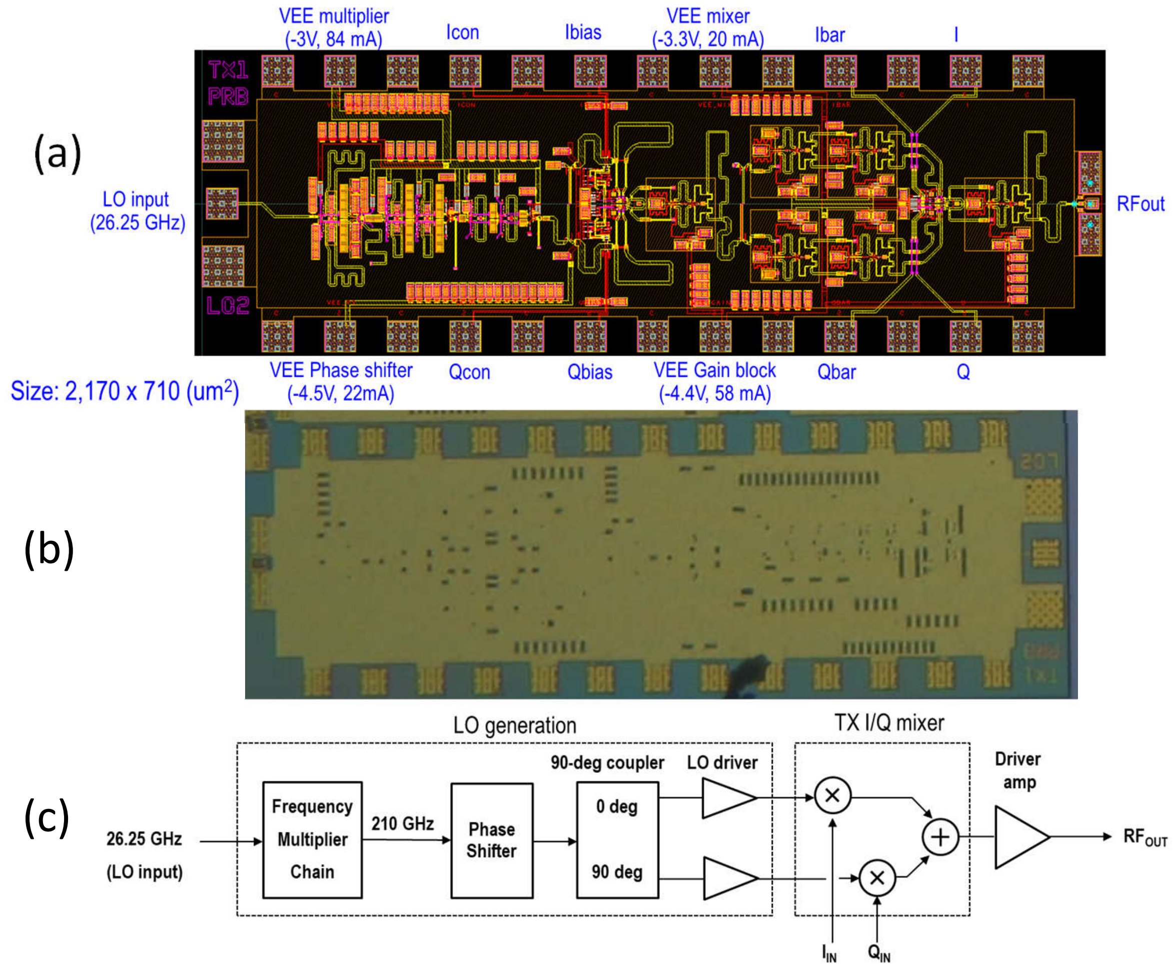

Figure 5.1: 210GHz transmitter with a ∼2dBm output power (Courtesy of Munkyo Seo).

Munkyo did preliminary measurements for the transmitter. Over 200-220GHz frequency range, the transmitter has a 10-12dB conversion gain (Fig. 5.2a). The transmitter has a ∼2dBm output power at 210GHz (Fig.5.2b), which closely matches the simulation results.

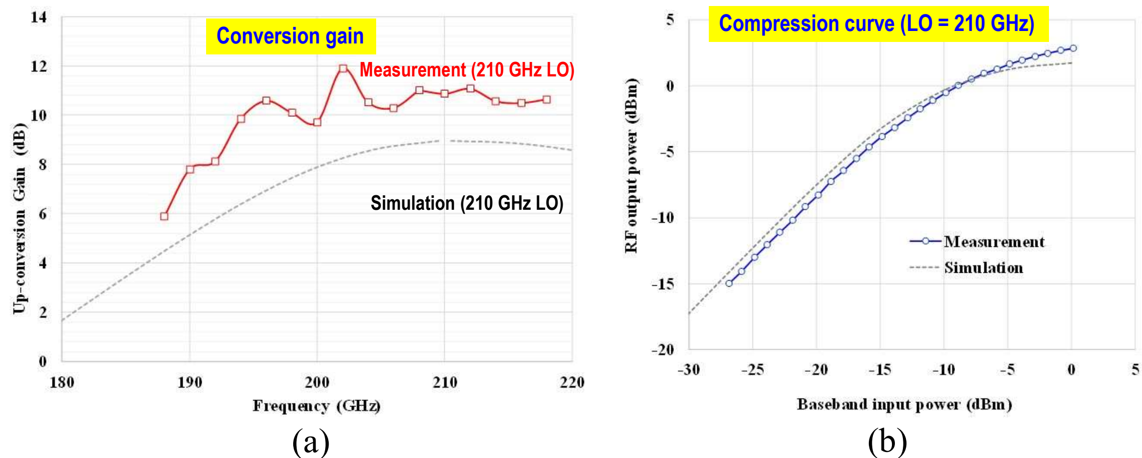

Figure 5.2: Measured and simulated results for the 210GHz transmitter with 2dBm output power. a) Conversion gain. b) Output power versus the baseband input power (Courtesy of Munkyo Seo).

5.3 210GHz Transmitter with a simulated ∼ 18dBm Output Power

The transmitter is designed in 250nm InP HBT technology (f_{max} ∼650GHz). In this transmitter variant, a high-efficiency power amplifier (presented in this section) is integrated with the transmitter presented in Section 5.2. This significantly increases the transmitter's power and efficiency.

5.3.1 210GHz Amplifier Design with ∼18dBm output power and 8% PAE

Power amplifiers are the key components in the transmitter. The amplifier's output power determines the maximum link range that the transmitter can cover. Additionally, the amplifier's efficiency dominates the efficiency of the whole transmitter since the amplifier consumes most of the transmitter's DC power. Here we report a high-

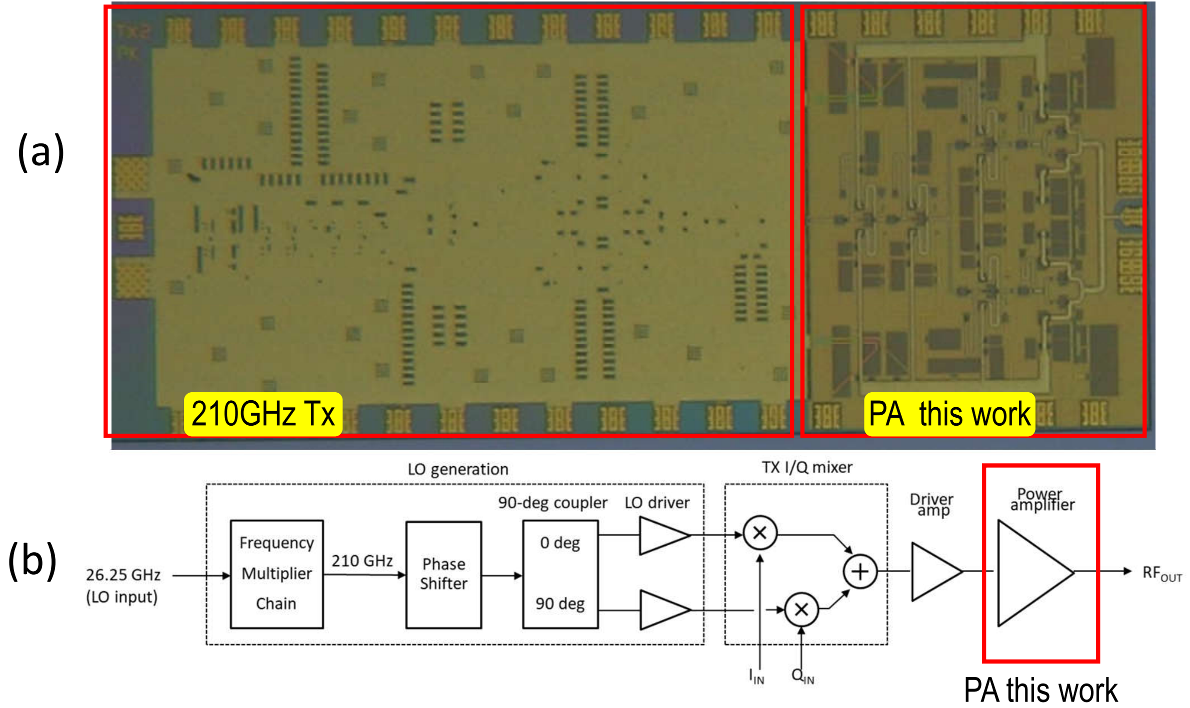

Figure 5.3: 210GHz transmitter with simulated ∼18dBm output power.

efficiency G-band power amplifier in 250nm InP HBT technology. The amplifier has four capacitively linearized common base stages. Four power cells are combined by a low loss 4:1 corporate combiner. The drivers are scaled to sustain high power added efficiency (PAE). At 202GHz operation, the amplifier has 18.3dBm saturated output power with 7.9% PAE. Over 190-210GHz, the saturated power is 17.7-18.5dBm with 6.9-8.5% PAE. The peak small-signal gain is 23.5dB at 204GHz with more than 19GHz 3dB bandwidth. The amplifier has a low DC power consumption of 858mW and a compact area of 1.2mmx0.95mm.

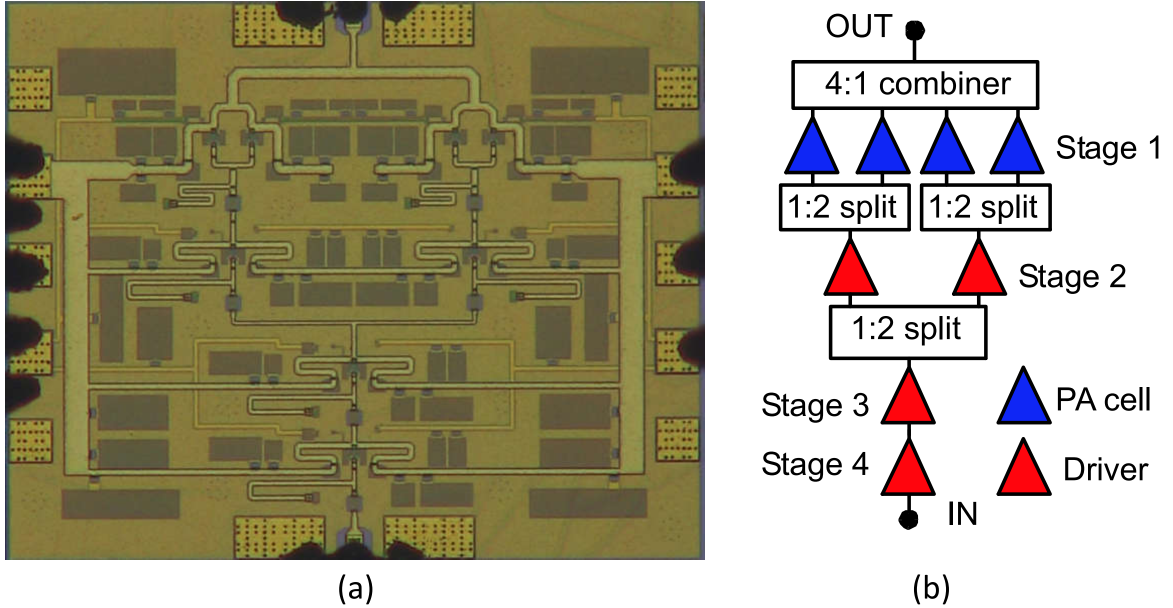

Figure 5.4: a) Die photo, area is 1.2mmx0.95mm. b) Amplifier block diagram.

5.3.2 Amplifier Design

IC was fabricated in the Teledyne 250nm InP technology [2]. The amplifier (Fig. 5.4b) has four common base stages. Four power cells, stage1, are combined by a low loss corporate transmission line. Each two power cells are combined and driven by a single driver (stage2). Similarly, two drivers are combined and driven by a single cell (stage3). Finally, another cell (stage4) is added without scaling to get the required gain.

We used the same design conclusion reported in [28] where we did a design study for different unit cells and proposed a low loss 4:1 corporate power combiner at 140GHz. Here, we follow the same design procedure. At high frequencies, the capacitively linearized common base shows superior performance compared to the common emitter or grounded common base; the linearized cell has the highest output power and efficiency at 1-dB gain compression. The base resistance ensures stable collector current control

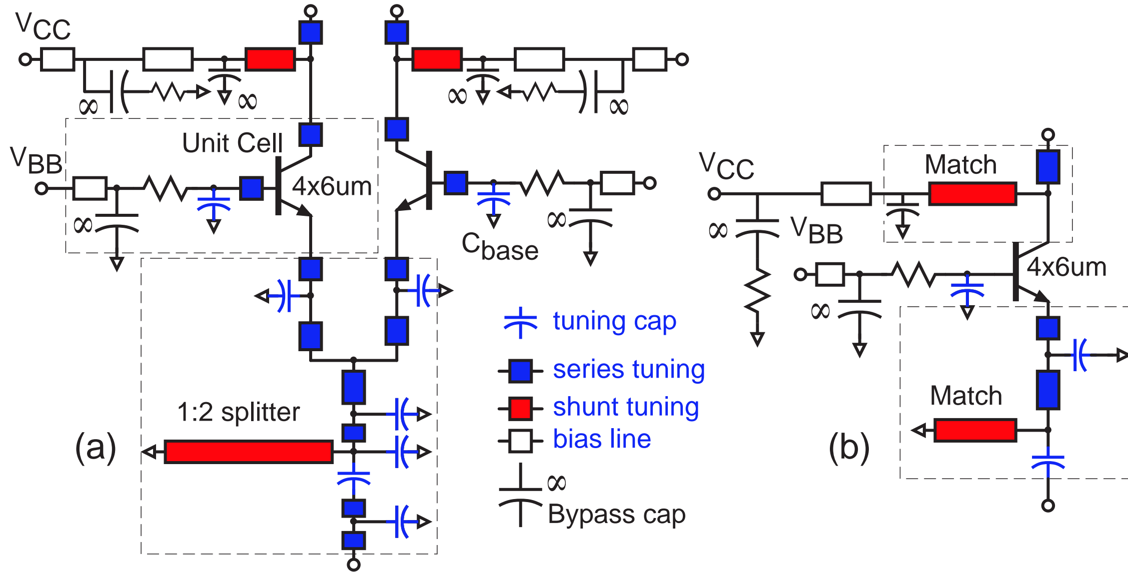

Figure 5.5: Schematic diagram of: a) Two combined power amplifier cells. b) Driver cell.

with minimum efficiency drop.

The same transistor size (4x6μm) is used for all cells. Power cells (Fig. 5.5a) are matched for maximum power added efficiency (PAE). Shunt inductive transmission lines tune the transistor parasitics. Then a transmission line network, similar to [28], uses a single quarter-wave section to transform the 50Ohm load impedance to the necessary impedance for each power cell. The output stage has a 96-μm HBT periphery. Drivers are optimized to deliver the necessary input power for the following stages. We have done conservative drivers scaling (48-μm, 24-μm, 24-μm HBT periphery) to avoid the soft compression operation. Only two independent DC supplies are used to reduce bias complexity: one to bias all stages collectors and the other to bias the stages bases. A considerate amount of the bypass capacitor with small series resistances are distributed along the bias lines to damp out-of-band oscillations. Ansys HFSS, 3-D EM simulation, is used to model all the parasitics and matching circuits.

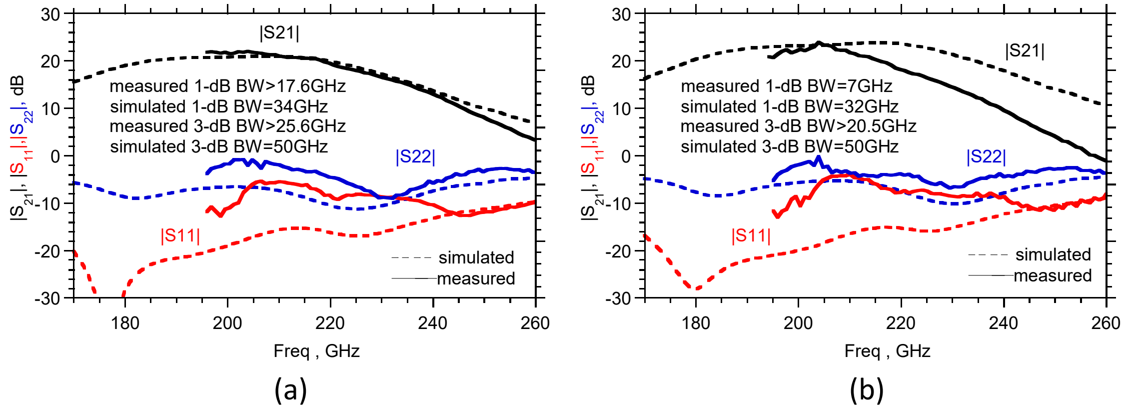

Figure 5.6: Measured (solid) and simulated (dashed) S-parameters at different bias conditions a) DC power (445mW). b) DC power (858mW).

5.3.3 Measurement Results

Fig. 5.4a shows the chip micrograph. The measurement is performed on a 3-mil thinned die mounted on a copper heatsink. S-parameters are measured using Keysight network analyzer with Oleson frequency extender modules and GGB wafer probes. LRRM standard calibration on an external substrate moves the reference plane to the probe tips. Fig. 5.6 shows a very good agreement between the measured and simulated s-parameters at (V_{CC}=1.9V, V_{BB}=1.6V, I_{CC}=226mA, and I_{BB}=9.9mA). The peak measured small-signal gain, $|S_{21}|$, is 21.8dB at 204GHz. The measured 1dB-BW and the 3dB-BW are more than 17.6GHz and 25.6GHz, respectively. We could not measure the lower frequency band due to equipment limitations. However, simulations show 34GHz 1-dB BW and 50GHz 3-dB BW. Bias is further increased (Fig. 5.6b) to (V_{CC}=2.5V, V_{BB}=2.2V, I_{CC}=327.5mA, and I_{BB}=17.7mA). The peak measured gain still matches the simulations. However, a frequency shift or BW shrinkage has been observed. It is believed that this discrepancy may be due to the thermal effects. The measured 3dB-BW is more than 20.5GHz, and simulations show 50GHz.

Fig. 5.7 shows the power measurement setup. A signal generator feeds a x8 VDI multiplier to provide the required amplifier input power at ∼200GHz. The amplifier input power is changed by varying the signal generator power feeding the VDI multiplier. A G-band 20-dB directional coupler is added after the VDI output to continuously monitor the VDI output power. The coupled port goes to a 20dB attenuator and a G-band harmonic mixer which is connected to a spectrum analyzer. The spectrum analyzer reading represents the power in the thru port by adding the appropriate calibration factor. In the calibration phase, a power sensor is connected directly to the thru port (Fig. 5.7a) then we record the Erickson power meter and spectrum analyzer reading at each frequency. The power ratio represents the calibration factor that should be used in the power amplifier measurement (Fig. 5.7b).

The measurement is performed on the 3-mil thinned part mounted on a copper heatsink. At zero RF input signal, the DC biases are (V_{CC}=2.5V, V_{BB}=2.2V, I_{CC}=327.5mA or 1.7mA/um, and I_{BB}=17.7mA). This is a conservative bias condition and could be increased further to get higher output power. The output power, P_{DC}, gain, and PAE are recorded at many points at different power levels and frequencies to verify the functionally. We have not seen any indications for oscillations. At 194GHz operation (Fig. 5.8b), the amplifier has a measured 18.5dBm saturated power with 8.5%PAE and 14.6dB associated gain. The amplifier demonstrates wideband large-signal operation. Over 190-210GHz (Fig. 5.8a), P_{sat} varies between 17.7-18.5dBm with more than 6.9% PAE.

5.3.4 Transmitter Simulation Results

The high-power transmitter (∼19dBm) measurement is in progress. Here we are presenting the simulation results. Fig. 5.9a shows the simulated upconversion gain. The transmitter has a peak gain of ∼38dB at 210GHz with 35GHz 3dB BW. The large

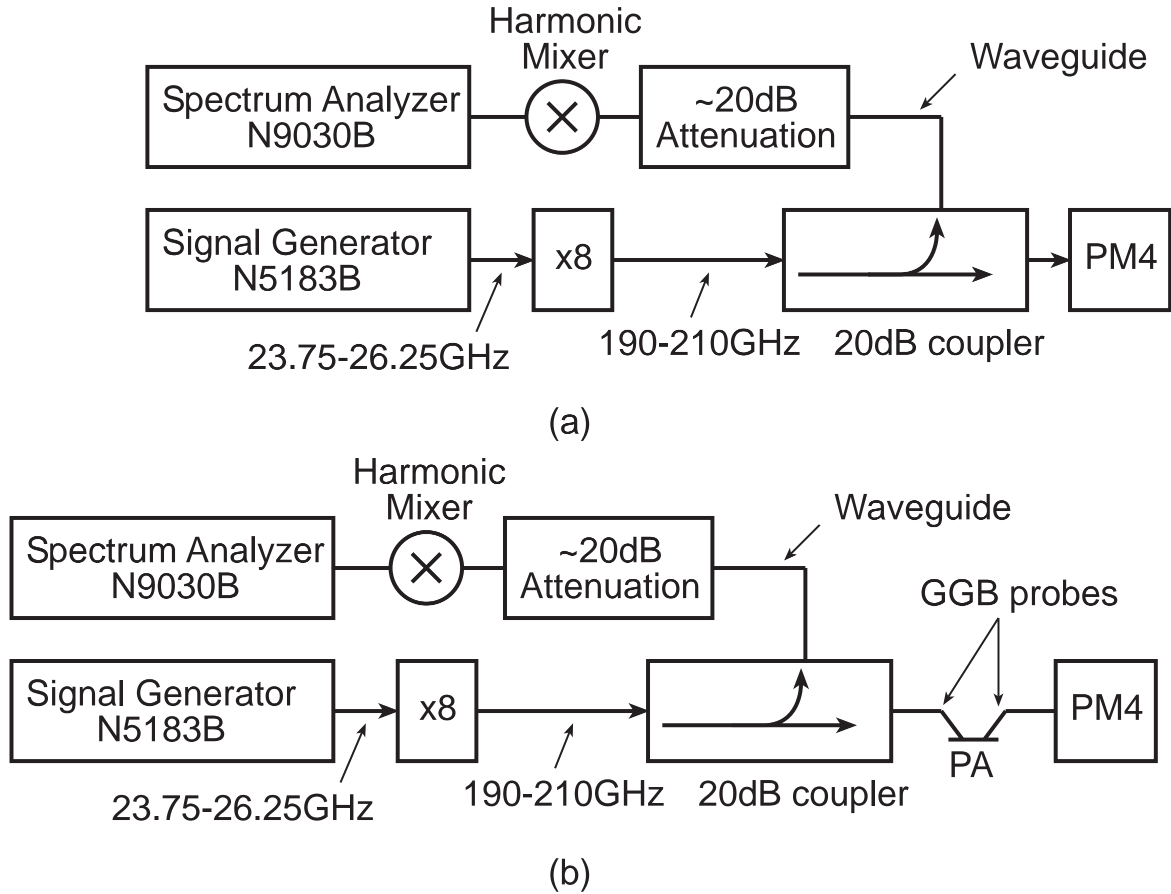

Figure 5.7: Power measurement setup: a) calibration mode. b) measuring the PA.

signal characteristic is shown in Fig. 5.9b. The transmitter has a simulated power of ∼18-19dBm while the OP_{1dB} is 13dBm.

5.4 Comparison of the State-of-the-Art Amplifiers

InP technology demonstrated lots of amplifiers working at G-band. Table 5.1 summarizes the amplifiers with high efficiency working at G-band. This work shows a significant improvement in the efficiency.

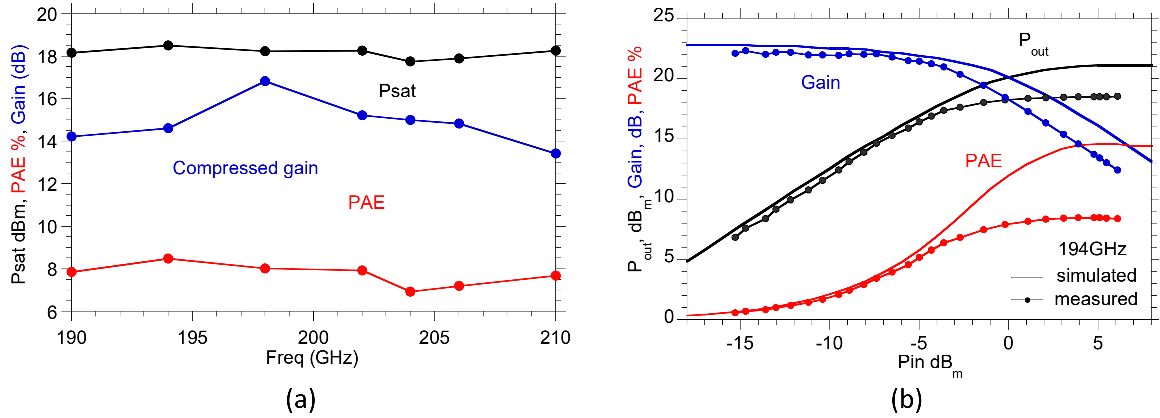

Figure 5.8: Power measurement setup: a) Measured output power with associated PAE and compressed gain versus the frequency reported at saturated output power. b) Measured and output power, PAE, and gain versus the input power at 194GHz.

5.5 Packaging Options for 210GHz Transmitter

As we will show in Chapter 6, mm-wave packaging is one of the most challenging parts of the design. Since it is mainly determined by the available assembly facilities. We will discuss the potential packaging options with the design tradeoffs.

1. **Wirebond**: This is the conventional method for the interconnect. However, the wirebond impedance becomes very hard to match at high frequency, as shown in Chapter 6. We can do some tricks to reduce the wirebond by mounting the PA in a cavity, but this requires advanced assembly techniques and more precision. Wirebonding techniques require a minimum chip pad size. The transmitter's output has a big pad, which induced lots of parasitics. The pad impedance is not compensated on the chip level and should be matched in the packaging design.

2. **Adding gold bumps**: Given that we have only bare dies, we had some attempts to place any sort of bumps. We did not have good success with a particular assembly house since they peeled the pad metals. Different manufacturers should be considered to see if they can succeed. Even if we succeed with adding the bumps,

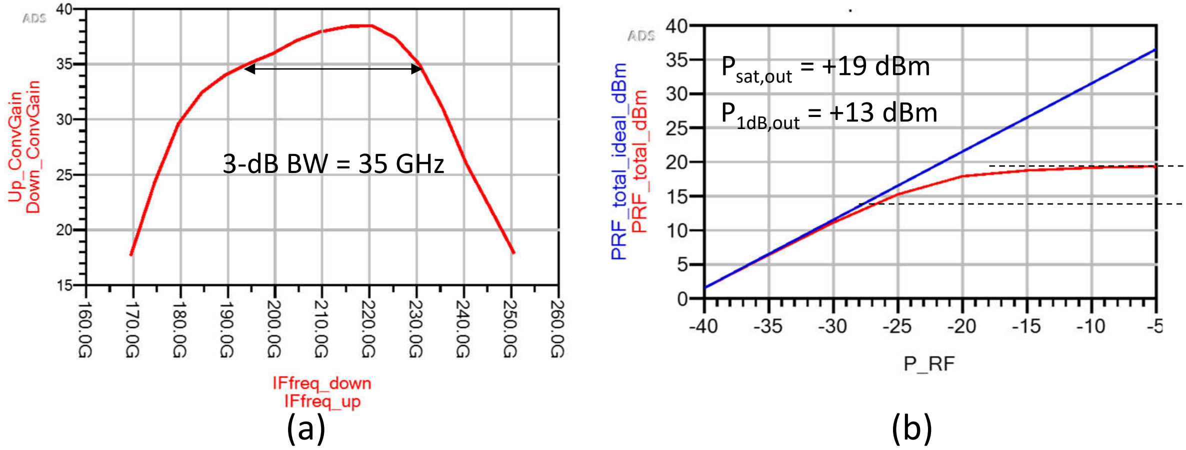

Figure 5.9: Simulation results for 210GHz transmitter with ∼19dBm. a) Up conversion gain. b) Large signal characteristic.

we still have a thermal challenge. The best heat dissipation occurs when the chip is directly attached by a high thermal conductivity material to a piece of copper. However, if the chip is flipped, that means that the heat is dissipated through the bonding balls and from the top. We should run thermal simulations to evaluate the validity of this approach.

3. **Antenna superstrate**: This approach will be discussed in the next section.

5.6 2x2 Transmitter with Quartz Antenna

Our goal in this design is to build a 2x2 packaged array that can be used for a 210GHz point to point demo. The transmitter has more optimized versions of its building blocks compared to the one presented in Section 5.2. A two-cell power amplifier is presented with ∼18dBm saturated output power. The transmitter uses a superstrate packaging technique where the antenna is designed on Quartz.

Table 5.1: State-of-the-art High-Efficiency G-Band Amplifiers

Freq, GHz	Tech	Gain at P_{sat}	BW,	P_{sat}, dBm	PAE_{sat}, %	P_{sat}/Area, mW/mm^2	Ref
190.8-244	250nm InP	19-22	53	16.2-18.9	3.3-6.1	50.6	[54]
205-235	250nm InP	4-6	-	17.8-20.4	2-5.1	79	[55]
190-260	250nm InP	13-17.5	18	17.5-21.5	5.1	78	[51]
185-255	250nm InP	12.2-17	-	20-23.9	4.1	73	[56]
204	130nm InP	∼7	27	15.4	5.8	102	This work
204	130nm InP	∼12	>25	18	4.8	69	This work
190-210	250nm InP	14-16.5	>20.5	17.7-18.5	6.9-8.5	62	This work
210	250nm InP	∼20	>41	18	13	98.7	This work Sim

5.6.1 Two Cells Amplifier Design

Previously, we added a large amount of bypass capacitance in the four-cell amplifier. This increased the amplifier width to 1.2mm. However, the width was not a limiting factor for a single transmitter channel. The problem arises when we move to build an array. Our objective is to construct a 2x2 array with $\lambda/2$ pitch. This means that we have to fit the 210GHz amplifier in ∼0.7mm width. That is why we designed another two cells amplifier with only 0.58mm width.

Fig. 5.10a shows the amplifier layout and the corresponding block diagram is shown in Fig. 5.10b. The amplifier has four linearized common base stages. The power and driver cell designs (not shown) are similar to the four-cell version with more optimizations. Two 50Ω power cells are combined by a low loss 2:1 TL line combiner. We are using this TL combiner with the impedance transformation in the PA breakout only. Since the load

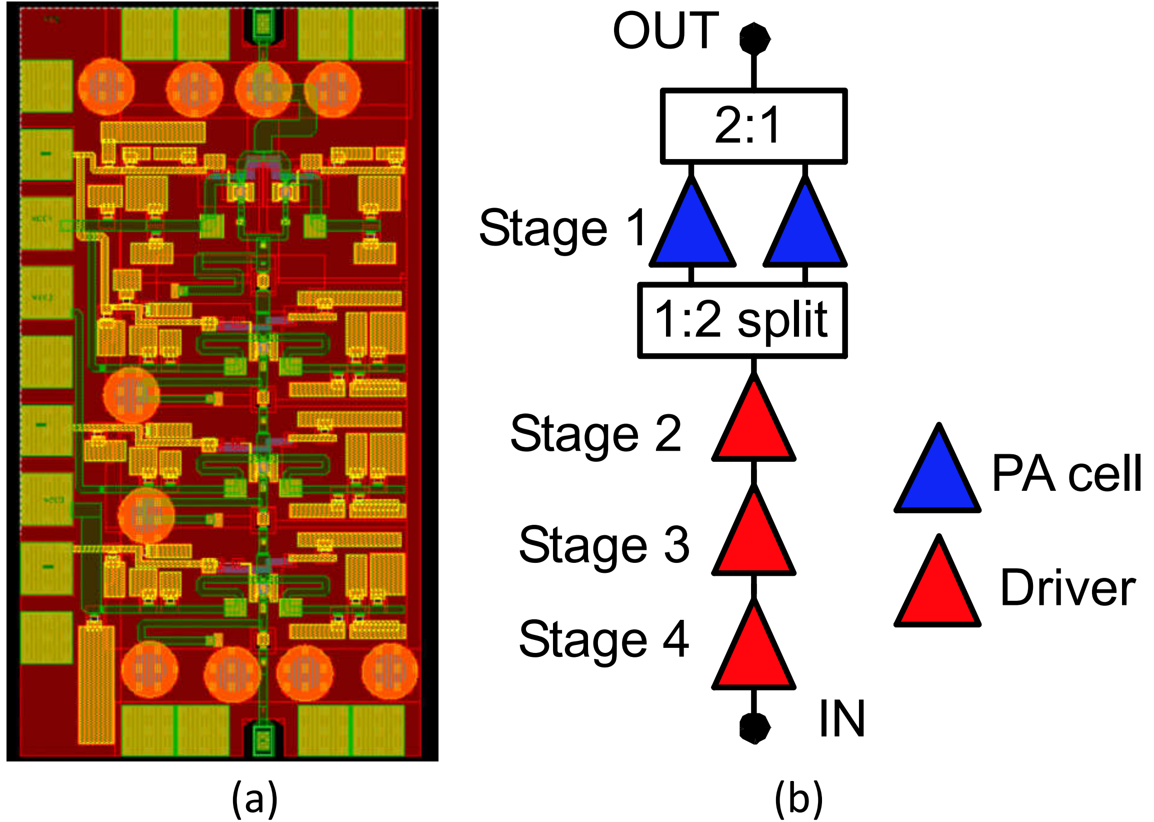

Figure 5.10: a) Die photo, area is 0.58mmx1.1mm. b) Amplifier block diagram.

impedance is 50Ω. However, we removed this line transformer in the array version since the antenna impedance is already very low, and it was easier to match to 25Ω instead of 50Ω. This improves the BW and decreases the matching loss.

5.6.2 Amplifier Measurement Results

The preliminary measurement is done by Teledyne. Teledyne used 140-220GHz frequency extension modules. The measured and simulated s-parameters are shown in Fig. 5.11a. S-parameters simulations are done with the recommended base inductance value (1.5pH for 6μm emitter length transistor). There is a very good agreement between the measured and simulated s-parameters. The amplifier has a peak measured linear

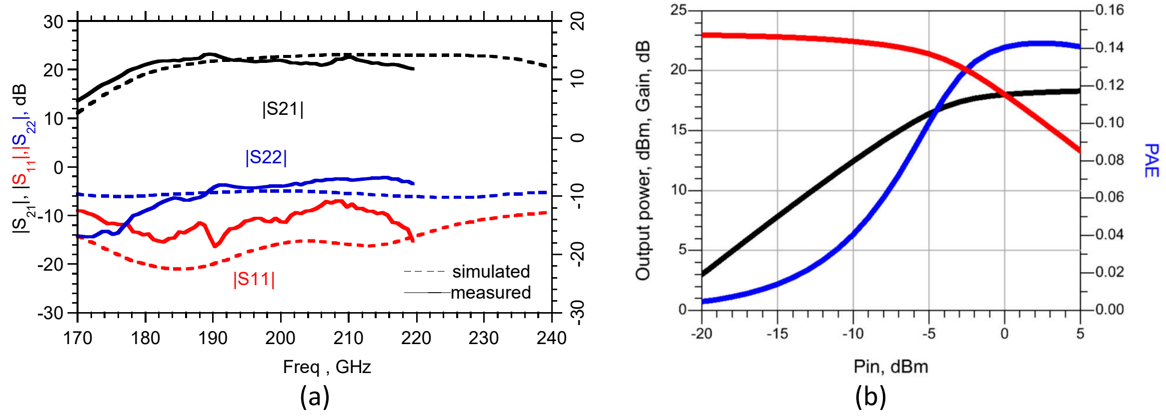

Figure 5.11: a) Measured (solid) and simulated (dashed) S-parameters at different bias conditions. b) Simulated large-signal characteristics at 210GHz.

gain ($|S_{21}|$) of 23dB with more than 41GHz BW. The power measurement has not been performed yet. Fig. 5.11b shows the simulated large-signal power measurement. The amplifier has a simulated peak output power of 18dBm with 13% PAE.

5.6.3 Quartz Antenna Design

Packaging using Quartz is one of the well known packaging techniques [57], [58], [59], [60], [61], [61], [62], and [63]. In this 2x2 array, we are using antennas on superstrate designed by Zhe at UCSD. The patch antenna is designed on a thin layer of Quartz (100μm), and it would be glued on the top of the chip. Using superstrate material such as Quartz simplifies the antenna design compared to on-chip antenna design since it offers lower dielectric constant and significantly larger thickness. The simplified wiring stack is given in Fig. 5.12a. The Quartz layer with the antenna is directly glued on the chip. The air gap is an assembly limitation and degrades the performance of the antenna.

The antenna is fed by coupling the signal from a microstrip line in the chip to the Quartz antenna. The dimensions of the TL coupler and antenna must be designed

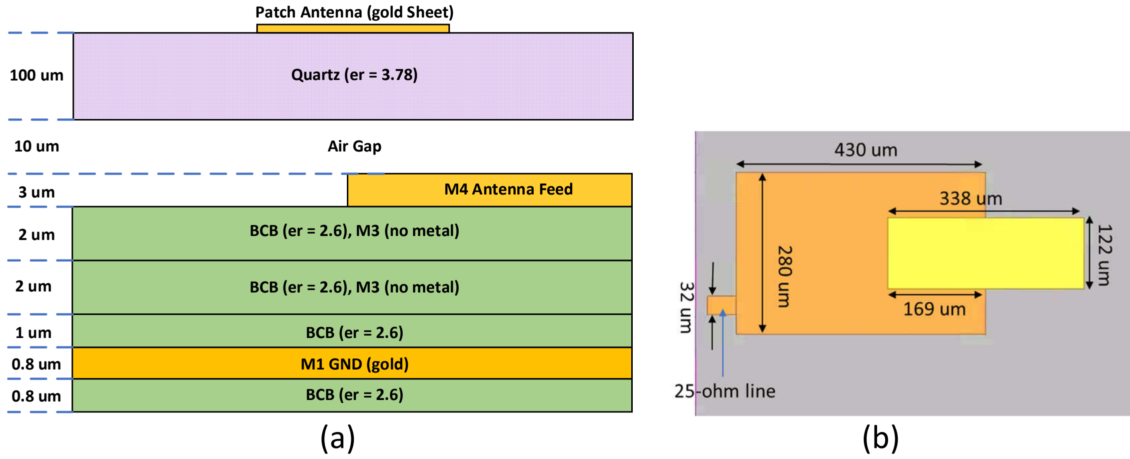

Figure 5.12: Quartz Design: a) EM simulation stack, b) Patch and coupler dimensions (Courtesy of Zhe).

properly to achieve high gain and efficiency. The dimensions of the antenna and coupler are given in Fig.5.12b. Quartz antennas usually have low input impedance. That is why we removed the 25Ω to 50Ω line transformer. There is no need to add intermediate 50Ω matching since it will add more loss and limit the BW. Alternatively, the two-cell amplifier with a 25Ω interface is directly matched to the antenna input.

5.6.4 2x2 Array Design

Fig. 5.13 shows the 2x2 transmitter array. Each element consists of a transmitter connected to a coupler that feeds the antenna. There are lots of bypass capacitors to increase the isolation between channels. The array requires a substantial amount of IO. It will be difficult to measure the array using on-wafer probes, and we are planning to wirebond the array for the measurement purpose. The expected EIRP from the array is 31.9dBm.

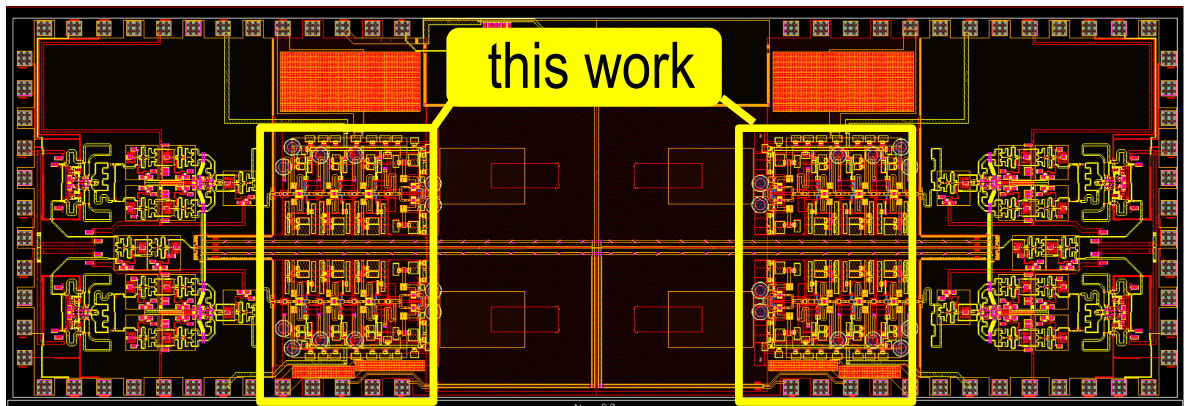

Figure 5.13: 2x2 Transmitter array with Quartz antenna. The thesis work is highlighted by yellow boxes. Other blocks are designed by Munkyo and antenna is designed by Zhe.

Chapter 6

Massive MIMO Demonstration and Millimeter-Wave packaging

6.1 Introduction

Our ultimate goal is to pave the road for the next generation communication system. There is an increasing demand for high-capacity mobile communications [1]. We need high efficient imaging such as [64] and as shown in Fig. 6.1b. We also want to provide a high data rate link between base stations (Fig. 6.2) and serve many users as in (Fig. 6.3). Considering millimeter frequencies for the next communication generation provides larger BW and the shorter wavelengths support massive spatial multiplexing. There are a lot of research interest in building packaged mm-wave modules [65], [66], [67], [68], [69], [70], [71], [72], and [73]. Building a real communications system demands tremendous collaboration between different groups. I was involved in ComSenter https://comsenter.engr.ucsb.edu. where we had regular meetings between system level, signal processing, communications, and hardware groups. System-level and communications groups set the requirements for the hardware groups. For example, they analyze

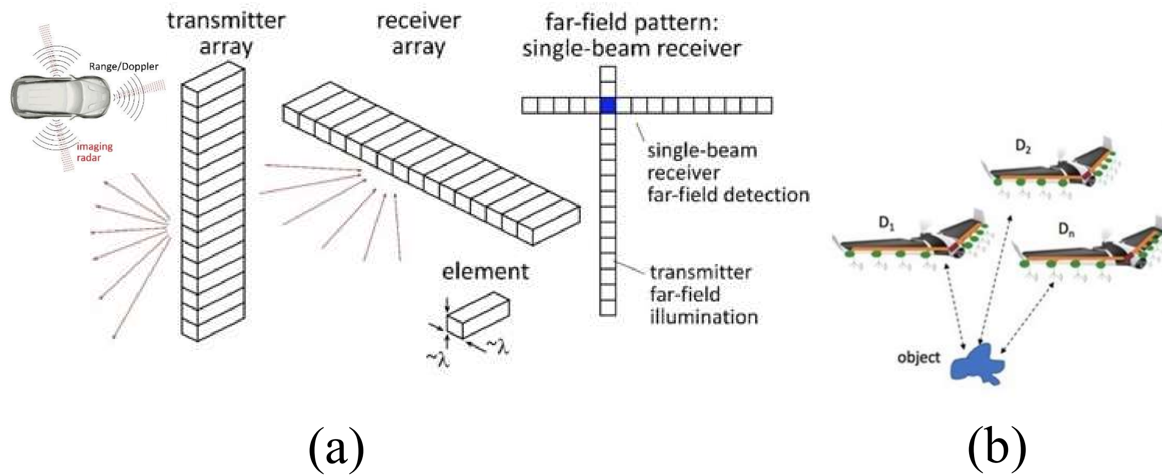

Figure 6.1: a) Hardware-efficient imaging. b) Cooperative/sparse imaging (Courtesy of Mark Rodwell).

the impact of linearity, phase noise... etc [74], [75], and [76]. Then they propose the optimum system to the hardware folks. The hardware group (including myself) takes those requirements and build the physical system.

In this chapter, we will present the design details for a massive MIMO hub at 140GHz. We are building massive MIMO arrays in a modular fashion. The MIMO array (Fig. 6.3a) consists of many elements. Each element carries transmitters or receivers integrated with an antenna array. We are using the 140GHz CMOS transmitters and receivers designed by our group [77]. We are also building a high output power module using heterogeneous integration between CMOS and InP. We are using the InP power amplifier that we presented in [28]. This increases the output power significantly and the corresponding communication range.

We will start with the link budget to determine the system-level requirements for our hardware. Then, we will give an overview of the module design and challenges in a modular approach. Millimeter-wave packaging is the core of this design. We will present

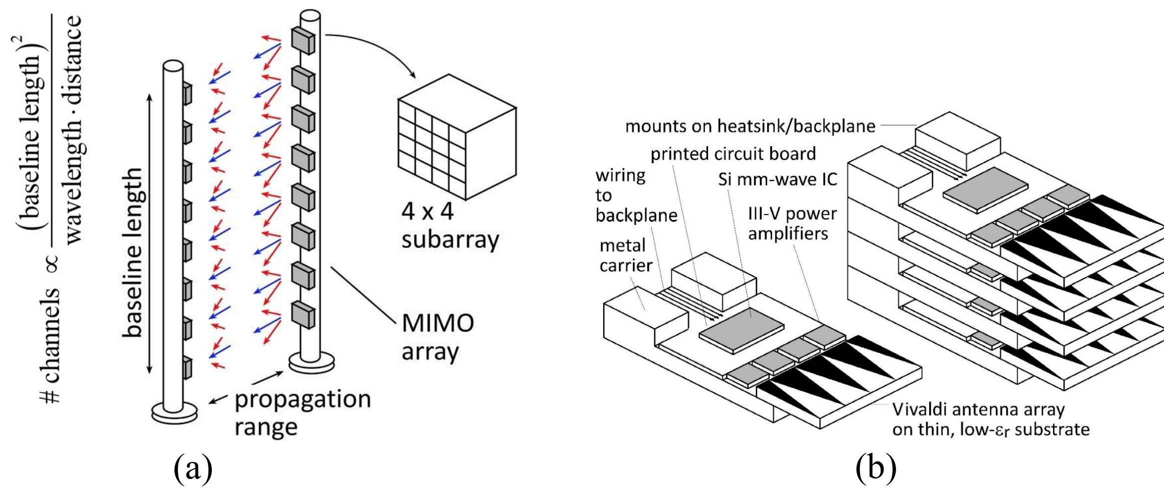

Figure 6.2: a) Point to point MIMO array. b) Cartoon drawing for single tile (Courtesy of Mark Rodwell).

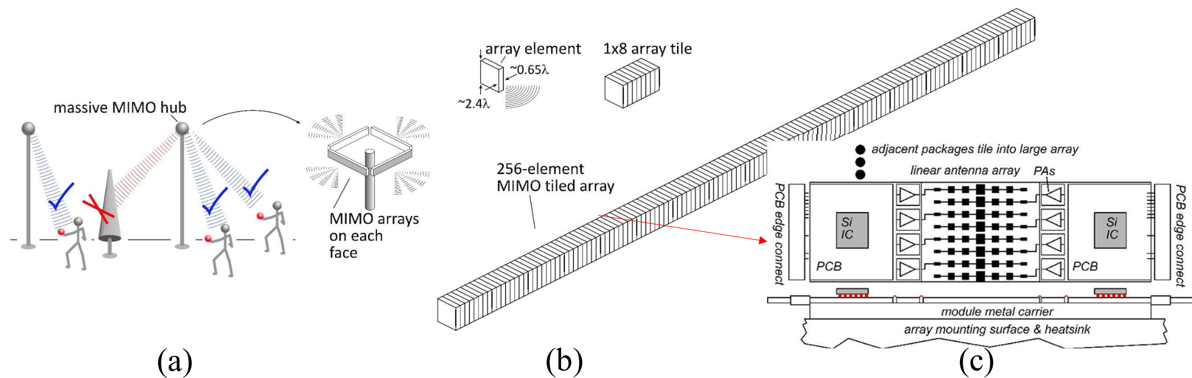

Figure 6.3: a) Massive MIMO hub. b) Cartoon drawing for MIMO array. c) Single tile (Courtesy of Mark Rodwell).

the design options and design details for our packaging. We will move step by step until we reach our ultimate goal. We will start with a single CMOS chip design, then we will present a single channel CMOS transmitter and receiver (CMOS chips integrated with an eight-element series fed patch antenna). Moving to the design of a complete transmitter and receiver tile which carries eight-element transmitters or receivers. Finally, we will repeat the same steps for the heterogeneous solution (CMOS transmitter with InP PA). We will show the design challenges in integrating the InP power amplifier pertaining to the

chip transition option which is wirebond in our case and thermal design considerations.

6.2 System Level Requirement: Link Budget

Given the assumptions in [1], to serve 128 users at 100m range and 10Gb/s/user using a 256-element MIMO array at 140GHz, the required operating output power per element is 16.5dBm. Given the large array, efficient power amplifiers are critical, generating less heat and simplifying the package design.

6.3 Tile Design Overview

We have different variants of the tile. We have a CMOS transmitter tile with a low output power, high-power tile where we integrated the InP power amplifier to the CMOS transmitter, and CMOS receiver tiles. My colleague "Ali Farid" designed the CMOS chips (transmitter and receiver) [[77] using GlobalFoundries technology (22FDX). The chips have the most advanced copper pillars. The InP power amplifiers, designed by me, are bare dies and we are using wirebonds for the transition. The transmitter or receiver tile carries 8 CMOS chips, with or without the InP PAs integrated with a series fed patch antenna.

We considered two approaches in the tile design. The first approach is to mount the chips on high-performance interposer material. For this application, we used Kyocera ceramic interposer. Then we used a low-cost PCB to hold the DC and RF connectors. The cross-section and top views for the interposer approaches are shown in Fig. 6.4a and Fig. 6.4b respectively. In this approach, we have a metal carrier to hold the PCB and the interposer. Additionally, it is serving as a heat sink. The CMOS chips are flipped on

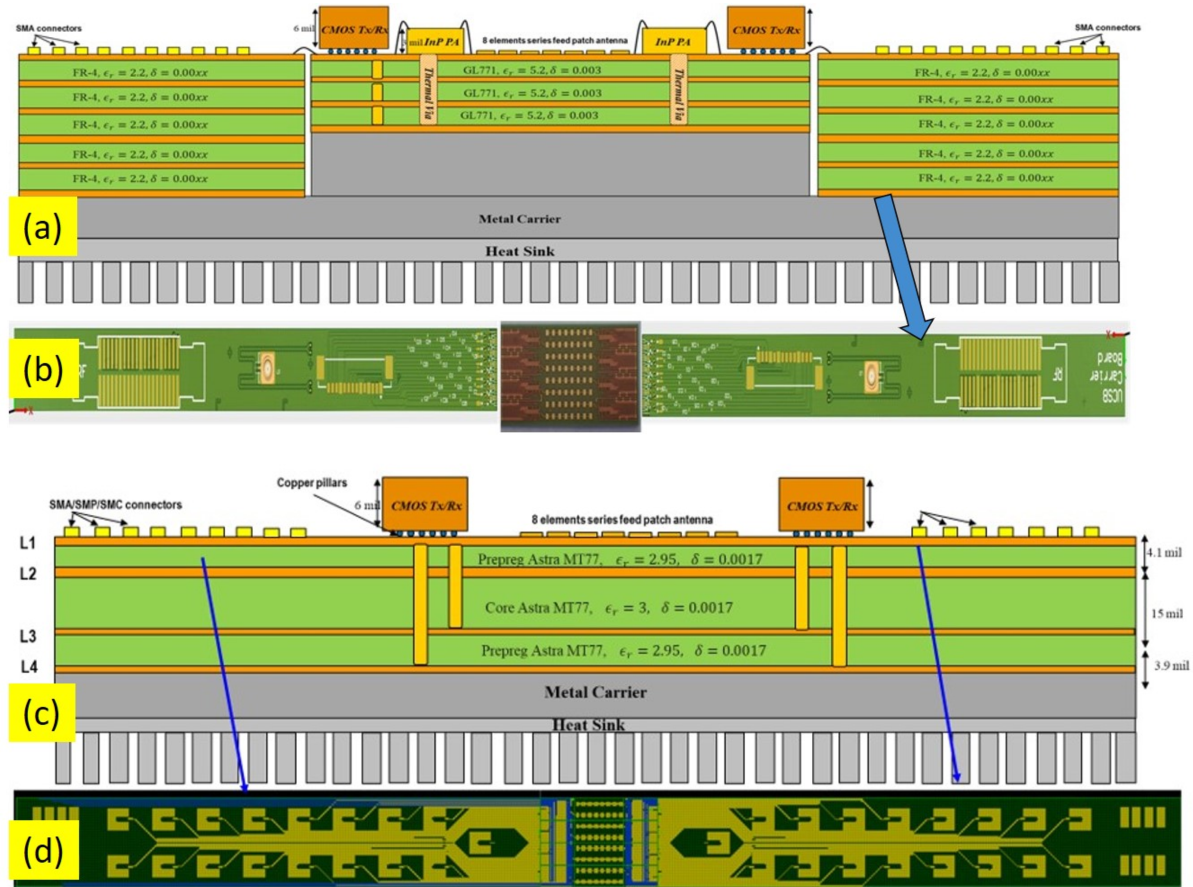

Figure 6.4: a) Cross section of the LTCC approach **(this work)** showing the interposer, chips, PCB carrier board with the DC and RF connectors. b) Top view of the LTCC approach. c) Cross section of the low-cost PCB approach (Courtesy of Ali Farid). d) Top view of the low-cost PCB approach.

the interposer and the InP chips are wirebonded to the interposer. We used wirebond connections between the interposer and the PCB.

The second approach is a low-cost PCB. Fig. 6.4c shows the cross section view for the PCB approach (top view in Fig. 6.4d). In this approach, all the chips are mounted on a low-cost PCB. The pros and cons will be discussed in Section 6.6

6.3.1 Challenges in tileable approach

Given that we are building a modular approach, we have a limitation on the module width to keep a constant antenna pitch. This means that we have to fit the chips routing, DC, and RF connectors in the tile width. This is a huge constraint at mm-wave frequencies. The free wavelength at 140GHz is ∼2.1mm. Our module width is ∼1cm, and it carries 8 transmitter or receiver elements. We have done an interleaved antenna feeding structure, so half of the chips are feeding the antenna array from one side, and the other half is feeding the antenna from the other side. This doubles the available area for the chip footprint. Working with small features adds lots of complications since we are using tiny capacitors and connectors, which complicate the assembly procedures.

6.4 Millimeter-Wave packaging

Millimeter packaging is one of the most challenging parts in building the module. We presented mm-wave record-efficiency amplifiers in Chapter 4. Our group also demonstrated a 140GHz transceiver in CMOS [77]. The major bottleneck is how to package our circuits using commercial facilities. There are multiple ways to build the chip to package transitions. Some of them requires advanced techniques and technologies [78], [79], [80], [81], and [82]. We will focus on the main approaches in the next sections. Some considerations determine the right approach.

1. **Transition to what?**: The first question is what are we interfacing to? The application determines the required interface. For wireless communications, we usually interface to antennas. There are many types of antennas such as patch, Vivaldi [83], horn ... etc. [84]. Based on the system requirements, we can determine the proper antenna. 3-D antennas such as horn require much more expensive

machining, which increases the cost and decreases the product volume. Given that we are targeting communication systems, we prefer planar structures such as patch, Vivaldi, dipole... etc. Planar structures are much easier to fabricate with low costs and high volumes. Each antenna has different properties in terms of gain, efficiency, and BW.

On-chip antenna versus antenna on substrate: We can design on-chip antenna [45], [85], [86], [87], and [88]. This approach does not require any complicated assembly procedures since everything is already integrated on the same design framework which makes the fabrication time very quick. However, modern IC technologies are optimized for circuit performance and not an antenna design. The metal separations are relatively small and the dielectric constant is relatively high. This reduces the radiation efficiency. The antenna dimensions are relatively large and consume huge die areas increasing the cost. The latter drawback is relaxed at mm-wave frequency since the wavelength is getting smaller.

The other approach is to build the antenna on a different substrate [89]. In this approach, we introduce more degrees of freedom. We can select the proper thickness that achieves the required efficiency, gain, and BW. We can use the proper material with the required dielectric constant. In antenna design, lower dielectric constants are usually preferred and give higher efficiency. We also can easily build the array to get higher gain since the substrate area could be significantly larger than the die area. On the other hand, there are many challenges in this approach; We need sorts of interface between the chip and the antenna such as wirebonds or C4. This significantly increases the level of assembly complexity. It is getting worse at mm-wave frequency since the manufacturer's tolerance can have a huge impact on the

performance. The lead time is much larger.

2. **EM performance**: Given that we have different options for the transitions, we must run EM simulation for the transition under consideration. Most of the chip interface, though not mandatory, is 50Ω matched. The antenna does not have to be 50Ω. For example, patch antennas have large input impedances. The purpose of this simulation is to evaluate how hard is it to match between the chip and the antenna given this transition option. If the required matching is minimum, this indicates that we can get broader BW and lower loss. Large impedance transformation is usually a narrow band and most of the time is more sensitive to assembly tolerance.

3. **Assembly challenge**: This is the most critical criterion. It is possible to get great performance for a transition design, but we should consider the practical implementation. Who is going to do the assembly? What are the cost and required volume to do the assembly? Some assembly companies stipulate working for mass production level only. What are the tolerance and yield? It is important to work within the limit of the assembly house's tolerance. There are more challenges that we will discuss as we proceed in the chapter.

6.5 Chip to Package Transition

6.5.1 Wirebond

Wirebond is a very old and well-known technique to build the transition [90], and [91]. It is simply a thin gold or Aluminum wire going from the chip pad to an external PCB. At lower frequencies, the wirebond could be modeled as an inductance. The wirebond works well at lower frequencies where its inductance is negligible. As we increase the frequency,

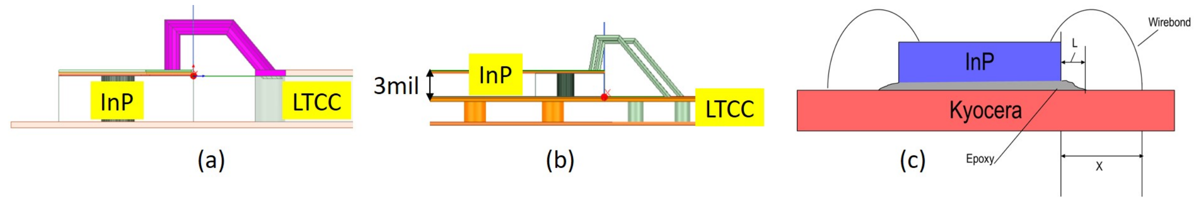

Figure 6.5: a) Cavity approach to reduce the wirebond length. b) Chip mounted on the surface of the LTCC. c) Epoxy leaking problem.

the wirebond impedance becomes much harder to match but there are reasonable results ∼100GHz [92]. We considered some tricks to reduce the wirebond length and therefore simplify the required matching. Fig. 6.5a shows the chip buried in a cavity so the chip pad is getting closer to the interposer's pad which reduces the wirebond length. The wirebond length is determined by the precision of the chip placement and cavity tolerance. Our assembly facility did not have good control for the cavity tolerance, this results in a huge impact on the performance. The other approach is to mount the chip on the surface of the interposer (Fig. 6.5b) since the chip thickness is only 3mils. Though this seems to have a shorter wirebond, we realized that the soldering material, Epoxy, may leak beneath the chip (Fig. 6.5c) and cause short. This sets a minimum wirebond based on assembly tolerance.

We also should check the surface finish of our chip and check the compatibility with the wirebond. This is determined by the assembly manufacturer. There is also a minimum pad size on the chip side. For each wirebond diameter thickness, the assembly house specifies the minimum pad size. In the InP chip, we had an additional problem pertaining to the metal adhesion. The metal in the InP chip does not stick well compared to silicon-based ICs. This requires more attention from the assembly house.

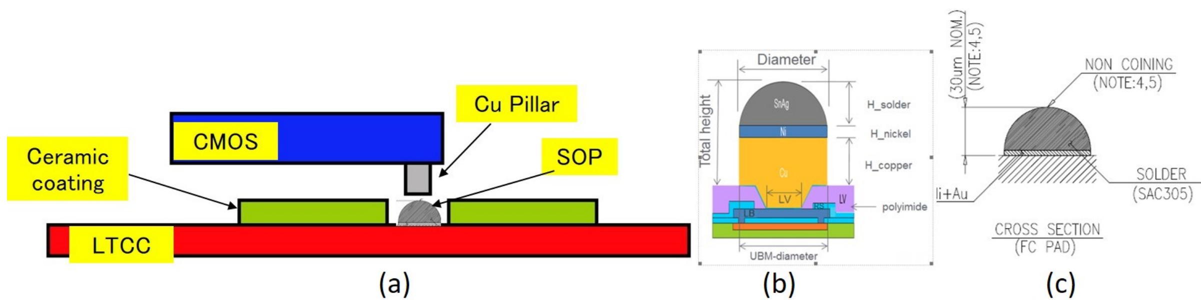

Figure 6.6: a) Sketch for the CMOS chip filpped on the interposer. b) Drawing for the copper pillar. c) Drawing for the SOP.

6.5.2 C4 Flip Chip

Flip-chip techniques are an advanced technique working at higher frequencies. In this approach, the chip has solder bumps to connect the signal [93]. The main advantage is that the dimensions of those balls are smaller than the wirebond. This means C4 transition requires less matching efforts compared to the wirebond. The C4 tolerance is also better so we do not have wide variations in the wirebond technique. The flip-chip technique is more complicated than the typical wirebond which increases the cost.

6.5.3 Copper Pillars

We had access to the copper pillars option from GlobalFoundries which is the most advanced option at that time. The pillar (Fig. 6.6b) consists of a small amount of copper covered by a soldering material. The main advantage of the copper pillar over the typical C4 is that we can get fine pitches and smaller pillar diameter. The main challenge is that the amount of the solder on the pillar is tiny. So, if we attached the chip directly, the solder may wick away causing open connections. There are some solutions for that; one assembly house suggested adding some paste on the interposer before mounting the chip. This should increase the soldering material. However, controlling the paste in this fine pitch was extremely challenging and did not succeed.

The other solution recommended by Kyocera is to add solder on a pad (SOP) (Fig. 6.6a,c). This process is very complicated and expensive. Adding SOP increases the amount of the soldering material which simplifies the attaching material. The other recommendation is to have a ceramic opening (solder mask opening) close to the pillar dimensions. This secures the location of the copper pillars. We can also see that using SOP is mandatory in this case since the height of the pillar is small and the ceramic coating (solder mask) has a certain height. We must make sure that the pillar does not dangle around and have good contact with the board.

6.5.4 Microstrip to Antenna Coupling

This is a sort of contactless approach. The signal is coupled between the microstrip on the chip side to the antenna directly without wirebond or pillars. This technique is similar to what we described in Chapter 5. The advantage of this approach is that we do not have to deal with the wirebond tolerance or access to an expensive special copper pillar. However, it still requires assembly efforts since we want to make sure that we have a precise placement for the antenna on the top of the chip. We want to minimize the gap between the antenna and the chip. Otherwise, we will have poor efficiency. The other drawback is that building the transition on the chip consumes a lot of die area.

6.6 LTCC vs PCB Approaches

There are mainly two approaches to mount the chips on the carrier. The first approach (Fig. 6.4a, b) is using a high-performance interposer. In this case, the chips are first mounted on a high-resolution board called an interposer. We were using Kyocera ceramic interposer with a fine resolution (minimum trace width and spacing is 40μm). The surface finish of the interposer must be compatible with the copper pillar. Usually, the interposer

area is small, and there is not enough space to place the DC and RF connectors. That is why we have to interface this interposer to another carrier board (PCB). This is a low-cost board with coarse resolution. This PCB carrier board carries all the DC and RF connectors. In this approach, the interface between the interposer and the PCB carrier board is challenging. We are using a dense wirebond interface to connect the DC and IF signals. This adds more complications to the assembly. We are also using a metal carrier to hold both the interposer and PCB carrier boards.

The other technique (Fig. 6.4c, d) is to build everything on a low-cost PCB. This is a single board that carries the chips, DC, and RF connectors. It is much cheaper and the turnaround time is much faster. However, this requires a board house with fine resolution and we had lots of problems in this approach and did not proceed.

6.7 Interposer Design

We are using a ceramic interposer from Kyocera. We have three dielectric layers (Fig. 6.7) each is 3mil with $\sim \epsilon_r$=5.2. We are using a relatively thin interposer since the power amplifiers are mounted on the surface of the interposer. Thin interposers have better heat dissipation. Also, we are using thermal vias provided by Kyocera. Those vias also help in dissipating the heat as we will show in the InP tile design. The dielectric constant is relatively high and not preferred in the antenna design, but this is the lowest that we can get.

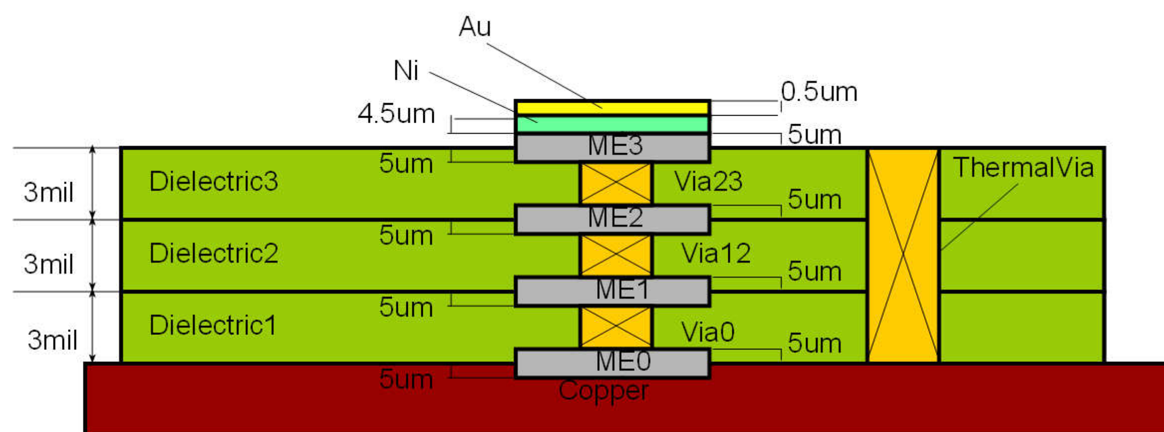

Figure 6.7: Wiring stack for the ceramic interposer.

6.8 Carrier Board Design

We are using 6-layers PCB (Fig. 6.8a) for the carrier board. The PCB has a poor lithographic resolution compared to the interposer. Therefore, we are using a multilayer board to have an enough space to route all the IO connections from the interposer. Note that the width of the PCB equals approximately the width of the interposer to maintain the hierarchy structure. Grounded CPW structures (Fig. 6.8b) are used for the IQ signals to have better shielding (Fig. 6.8b). All the DC, RF connectors and capacitors are surface mounted to simplify the assembly process.

6.9 135GHz CMOS Transmitter Tile

In this section, we will present the design details for a CMOS transmitter tile. We will start with the transition design and copper pillar matching. We will present the results for a single packaged transmitter chip. Then we will design an eight-element series fed patch antenna and integrate it with the transmitter chip. Also, we will provide the measurement results for the integrated chip with the antenna. Finally, we will present

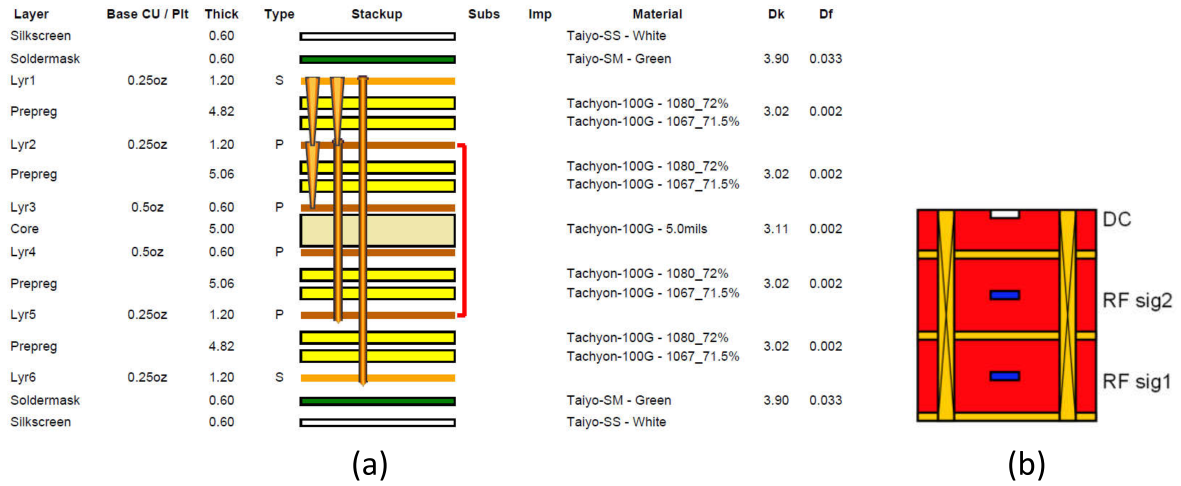

Figure 6.8: a) Wiring stack of the PCB. b) Cross section in the wiring stack showing the RF and DC routing techniques

the design of a tile including 8 CMOS transmitter channels.

One CMOS transmitter tile (Fig. 6.9a) consists of interposer, PCB carrier and metal carrier. The interposer (Fig. 6.9c) carries 8 CMOS chips on the ceramic interposer. Fig. 6.9b shows a cartoon drawing for the CMOS transition. Starting from the CMOS chip, we have a small microstrip line going to the pad. Then a microstrip to CPW transition through the copper pillars. Then another CPW line on the interposer. Finally, we have another CPW to microstrip transition going to the antenna. We considered all those transitions in our matching circuits.

We are using a series fed patch antenna. To get a wide scanning angle without grating lopes, we chose the antenna pitch to be $\sim 0.6\lambda$. It is challenging to fit the transmitter routing in this tiny pitch, so we used an interleaved antenna structure. Half of the antennas are fed from the left and the other half are fed from the right. For proper operation, we should consider adding 180° phase shift to equalize this feeding mechanism.

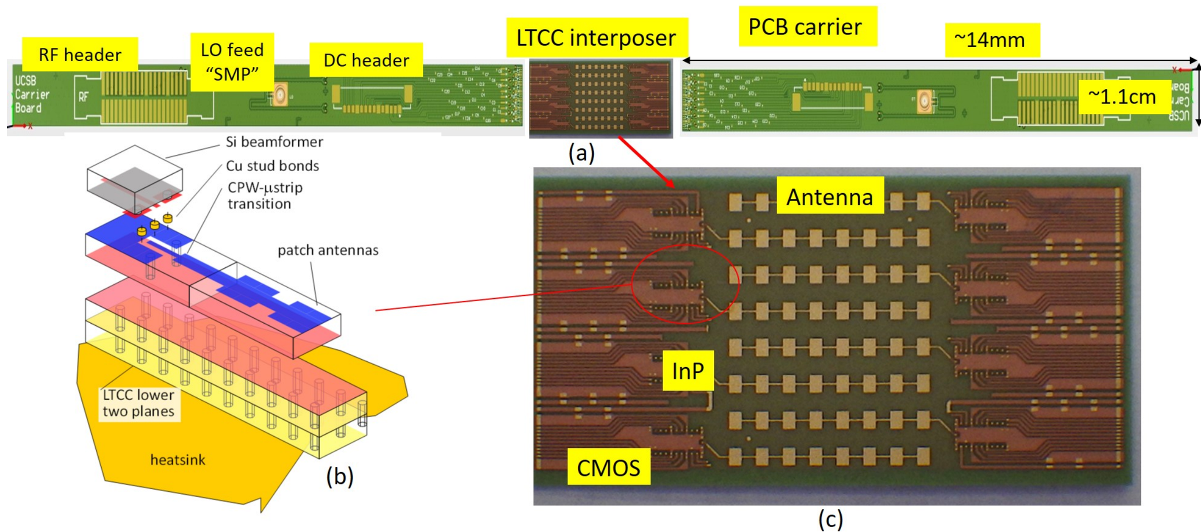

Figure 6.9: a) Photos for the transmitter module showing the LTCC ceramic interposer and PCB carrier board. b) Cartoon drawing for the CMOS transmitter chip to the interposer showing the different type of transitions. c) Close look on the LTCC ceramic interposer showing the antenna arrays and chip footprints.

6.9.1 Copper Pillar Matching

Fig. 6.10 a, b shows the copper pillar modeling using HFSS. We did a simplified cylindrical model for the pillar with the information given by the foundry. This is a 2-port simulation. The first port goes into the CMOS side before the pad using a short TL section. The second port is placed on the Kyocera interposer side. Fig. 6.10c, d shows the unmatched pillar performance. We can see that the pillar impedance is already close to the center of the smith chart which means that it is easier to match with a reasonable BW.

6.9.2 Packaging Results for a Single CMOS Chip

To verify the performance of the copper pillar, we have a test structure holding the chip (Fig. 6.11a) with a tiny CPW structure to land the probes. Fig. 6.11c shows the results of the CMOS transmitter after the copper pillar transition. In this test, the LO

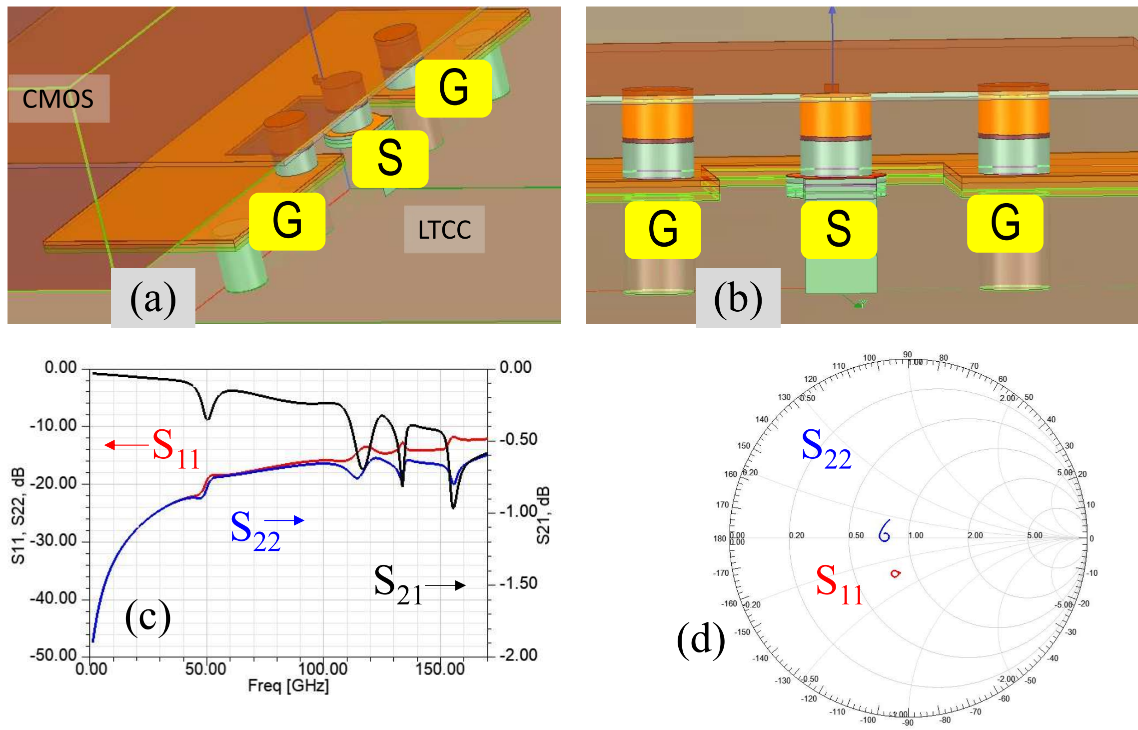

Figure 6.10: a) HFSS model for copper pillar. b) Different views for the transition. c) S-parameters simulations. d) S-parameters simulations on smith chart.

signal is fixed at 135GHz while the transmitter RF Input signal is fixed at 100MHz. The input RF power (RFPin) is swept from -29dBm to 6dBm and the LO signal power is 2dBm. The transmitter including the copper pillar losses and PCB routing has P_{sat} of ~2.1dBm compared to 2.9dBm for on-wafer probing. This means that the copper pillar loss with the PCB tiny trance has less than 1dB of loss. Fig. 6.11b shows the conversion gain. In this test, the LO signal is fixed at 135GHz while the transmitter input signal is swept from 100MHz to 15GHz. The LO signal power is 2dBm, while the input RF signal (RFin) is -16dBm. The 135GHz transmitter without antenna has a 3-dB modulation bandwidth of 12GHz (from 128GHz to 140GHz).

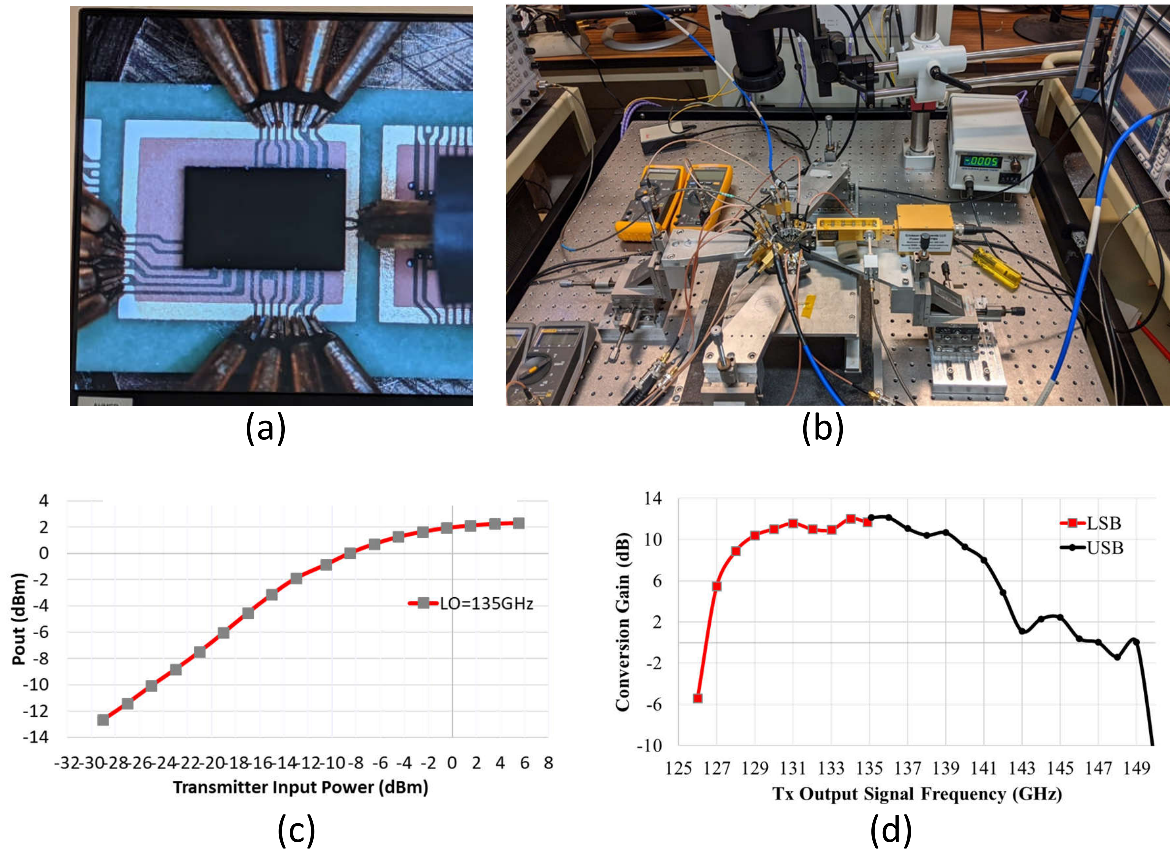

Figure 6.11: Packaging results for 135GHz transmitter with copper pillar transition: a) CMOS transmitter chip mounted on LTCC interposer. b) Measurement setup. c) Measured transmitter's output power versus the input power including the copper pillar transition loss d) Transmitter conversion gain versus the output frequency

6.9.3 Antenna Design

In this module, we are using a series fed patch antenna. Patch antennas are easy to design with a reasonable gain. However, it has a narrow BW. The antenna is designed according to the design procedures in [84]. First, we start designing a modular element (Fig. 6.12a). The frequency of operation defines the patch length according to [84] and the width determines the input impedance for the antenna and the radiation efficiency. Once we define the parameters for the modular element, we can repeat it in series to get more gain (Fig. 6.12b).

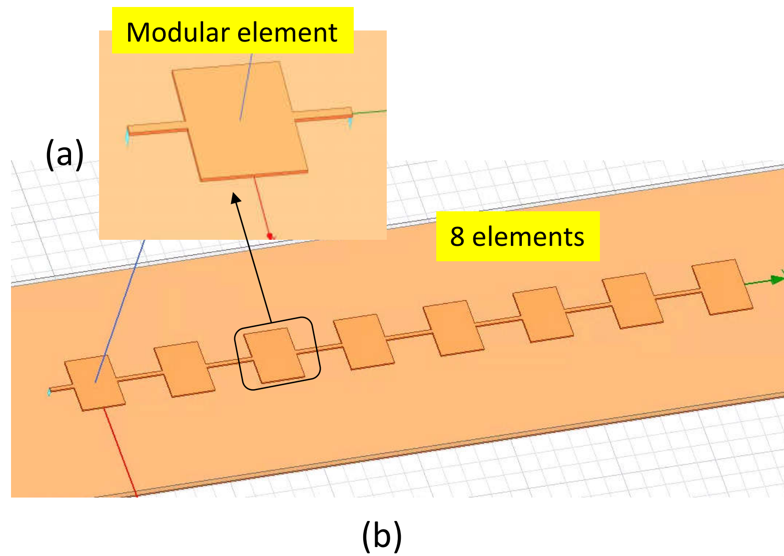

Figure 6.12: Antenna Design: a) Modular element. b) Eight series fed patch antenna.

The patches are connected and matched by a microstrip line. We picked the minimum width for this TL (40μm) to minimize the non-useful radiations from this TL. The length of the TL should be $\sim \lambda$ to have constructive addition between the patches at the broadside. Otherwise, the beam could be squinted. It is better that we do impedance matching between the elements. For infinite series fed patches, each element has the same load impedance which is the input impedance for the following element. However, for a limited number of elements, the last one does not have the same load impedance. We can design a load termination by adding a dummy element after selecting the width and length to give the required termination. Yet I did not see a huge impact, so I did not include it.

6.9.4 CMOS to Antenna Transition

The copper pillar is matched to the antenna input impedance using a transmission line transformer. The width and length are optimized to have good S_{11}. Fig. 6.13a shows a photo of the antenna with the matching circuit to the CMOS. We performed a 1-port S-parameter measurement using 110-170GHz VDI extenders. There is a good agreement (Fig. 6.13c) for the input reflection coefficient which indicates the precision of the modeling and design. However, for the antenna design, S_{11} is not sufficient to verify the functionality and we must measure the radiation pattern. The antenna setup is shown in Fig. 6.14. The antenna is glued by a tape on the wafer chunk and we used a 110-170GHz VDI frequency extender as an input source. We used a D-band standard gain horn antenna with ∼24dB of gain in the receiver. The horn antenna is connected to a D-band harmonic mixer going to a spectrum analyzer. All the component losses are measured and calibrated to get the actual antenna gain. Fig. 6.13b shows the radiation pattern versus the steering angle. The measured antenna peak gain is ∼11dB at 135GHz with 15 degrees 3dB beamwidth. Fig. 6.13c shows the measured and simulated antenna gain versus the frequency. The antenna measured 3-dB bandwidth is 6GHz and has a peak gain of 10.8∼11dB. The measured gain is a little lower than the simulation. It is possible that the losses are underestimated or there are measurement errors.

6.9.5 Single Transmitter Element: Measurement Results

The next progression is building a single channel transmitter. The single CMOS transmitter feeds an 8 element series fed patch antenna. This is an example of a real packaging implementation. The DC and IQ input signals are fed to the CMOS chips by probes (could be easily replaced by DC and SMAs connectors). Then, the output is a ∼

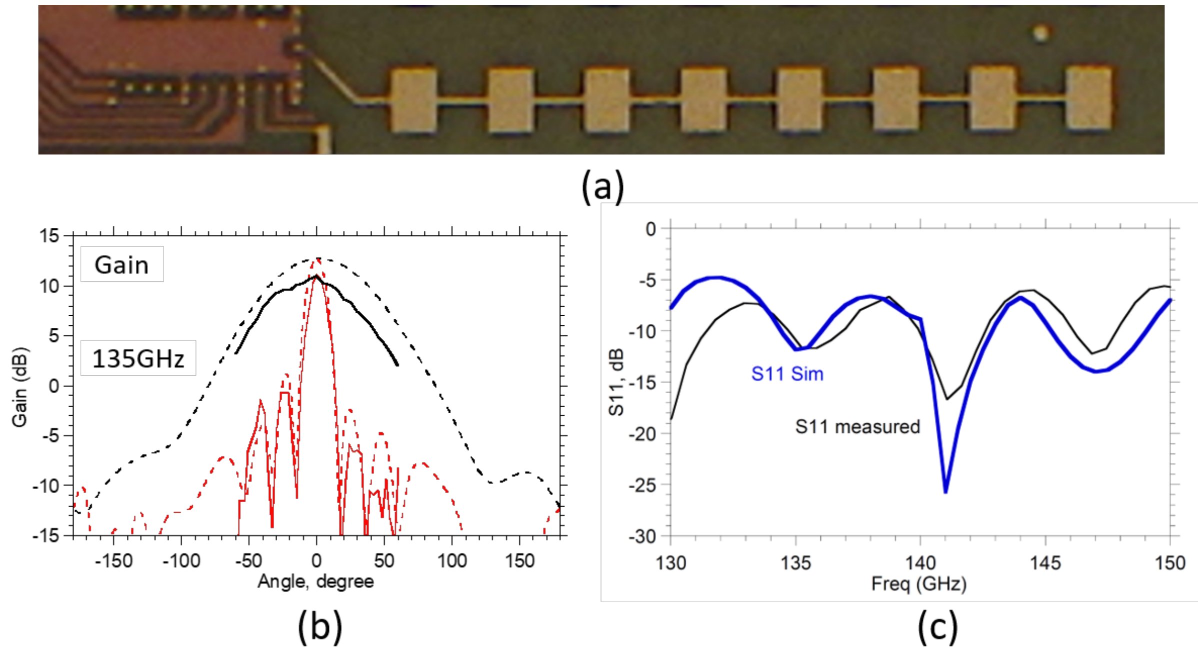

Figure 6.13: a) Photo for the eight-element series fed patch antenna and the chip footprint. b) Measured and simulated radiation patterns at the azimuth and elevation. at 135GHz. c) Measured and simulated input reflection coefficient and gain

135GHz signal transmitted by the antenna. This breakout verifies the transition design between the CMOS chip and the antenna. We demonstrated that we can achieve real mm-wave communication. Fig. 6.15a shows a photo for the chip mounted on the LTCC driving eight series fed patch antenna array.

Fig. 6.15b shows the transmitter EIRP at Elevation and Azimuth directions. The LO is fixed at 135GHz and RFin is 100MHz with RFpin=0dBm (Antenna is rotated from -60 to 60deg) in both the elevation and Azimuth directions. The EIRP at P_{sat} is 13dBm where the Antenna 3-dB Beam width=15degree. The Sidelobes to main Lobe ratio is 13dB (Close to theoretical). Fig. 6.15c shows the conversion gain versus the output frequency. In this test, the LO signal is fixed at 135GHz, while the transmitter input signal is swept from 100Mhz to 15GHz. The LO signal power is 2dBm, while RFin is -26dBm. The

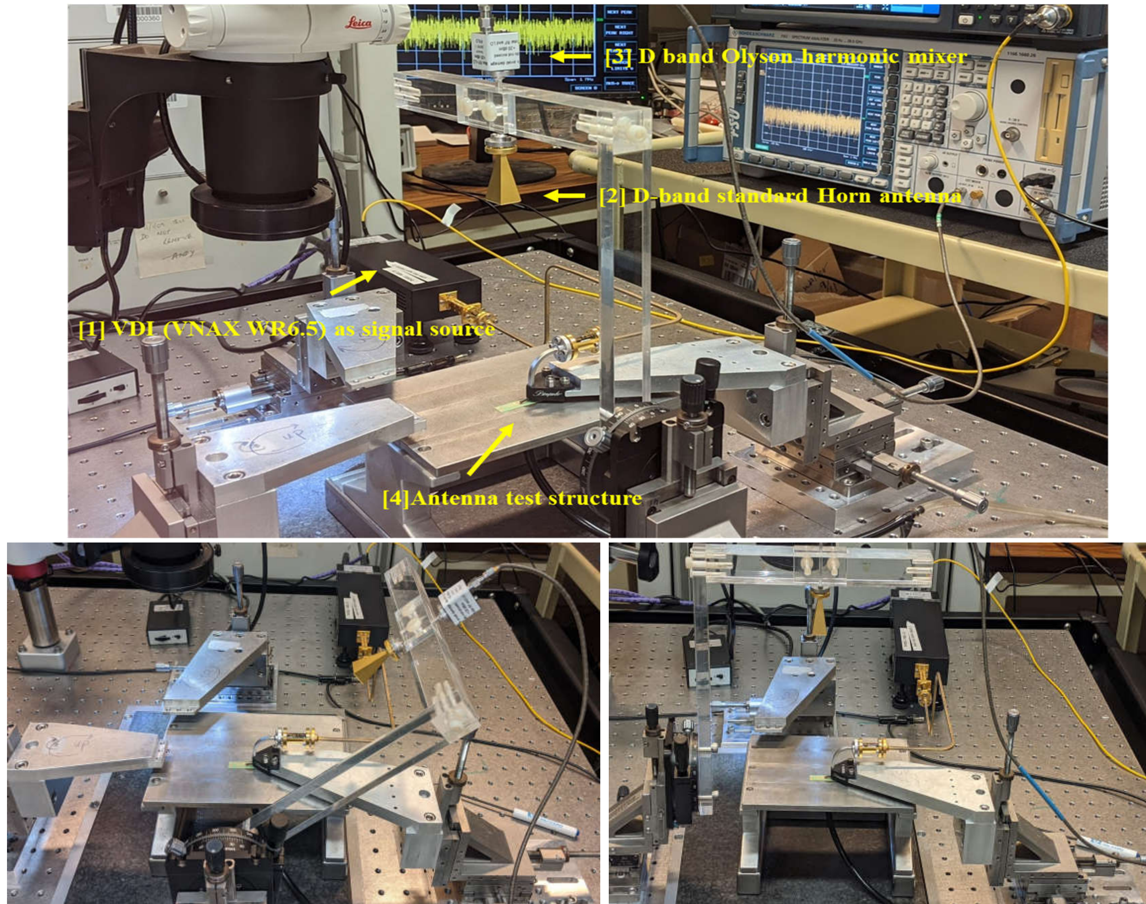

Figure 6.14: Antenna radiation pattern Setup from different angles (Courtesy of Ali Farid).

135GHz transmitter with antenna has a 3-dB modulation bandwidth of ∼5GHz (from 132GHz to 137GHz). The 3-dB Modulation Bandwidth is limited by the antenna BW. Fig. 6.15d shows the 1dB compression Point (RFLO=135GHz, RFin=100MHz, RFPin=-28dBm to 6dBm). The EIRP at P_{sat}=13dBm (at broadside direction) and the OP_{1dB} (EIRP)=8.5dBm (at 4.5 dB back off from P_{sat})

Fig. 6.16a shows the OIIP3 under this condition: RFLO=135GHz, RFin1=100MHz, RFin2=99MHz RFPin=-28dBm to 6dBm. The OIIP3 is 18dBm while the OP_{1dB} (EIRP) is 8dBm (at 4 dB back off from P_{sat}). Fig. 6.16b shows the transmitters LO Tuning

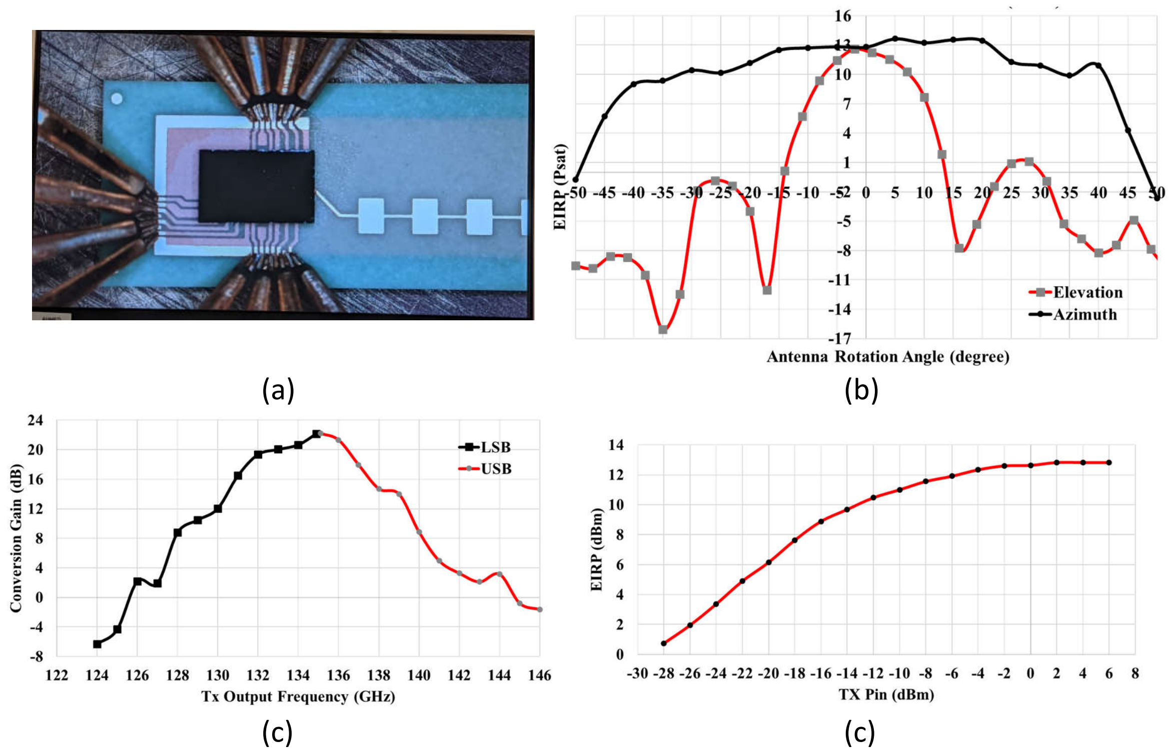

Figure 6.15: Single CMOS transmitter channel with eight series fed patch antenna array) a) photo. b) EIRP at elevation and azimuth. c) conversion gain versus the output frequency. d) EIRP at broadside direction at 135GHz versus the input power (Courtesy of Ali Farid).

Range. The RFLO is swept from 124GHz to 144GHz, Rfin=1GHz, RFPin=-0dBm (to saturate PA). The transmitter LO 3-dB tuning Range is from 133GHz to 137GHz

6.10 135GHz CMOS Receiver Tile

The receiver design is pretty much similar to the transmitter. The only difference is that the receiver pitch is 125um compared to 175um in the transmitter. This added more assembly efforts, but it has a negligible impact on the RF performance. We used the same antenna design. Fig. 6.17 shows the performance of the CMOS receiver with the copper pillar transition. Fig. 6.17a shows the receiver conversion gain. In this test the LO and RF input signals are swept to keep the baseband signal at 1GHz, RF

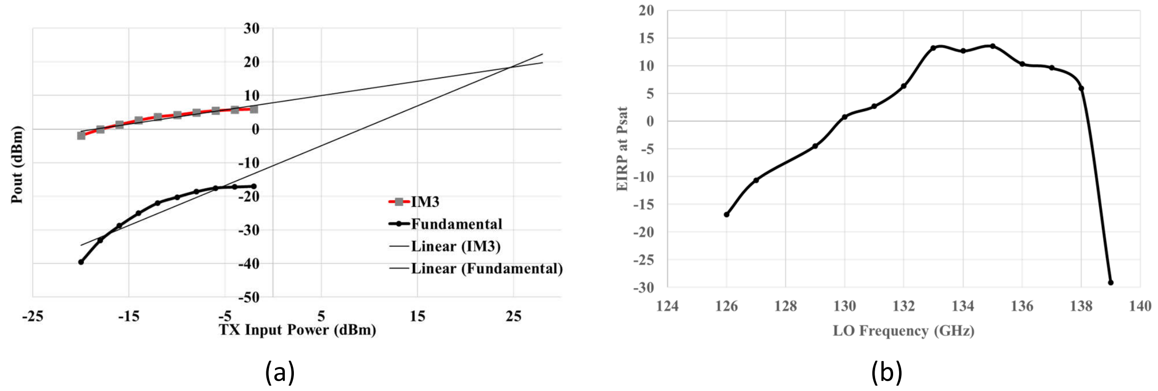

Figure 6.16: Single CMOS transmitter channel with eight series fed patch antenna array a) Output power versus the input power at 135GHz at fundamental and IM3 b) LO tuning range versus the LO frequency (Courtesy of Ali Farid).

input power =-30dBm, LO Tuning range∼=5GHz. The conversion Gain is 26∼27dB (close to the conversion gain of the 1st design without packaging). Fig. 6.17b shows the receiver's output power versus the input power. The LO is fixed at 135GHz and RF fixed at 136GHz, and the BB signal at 1GHz. The RF input power is swept from -42dBm to -4dBm P_{1dB} ∼=-27dBm (Slightly better compared to previous tapeout without packaging).

6.11 135GHz CMOS transmitter with InP PA Transmitter Tile

CMOS transmitters have a limited output power. We already demonstrated a high efficiency with high output power InP power amplifier in [28]. In this section, we will consider the heterogeneous integration between CMOS transmitters to InP power amplifiers. The CMOS chip is working as a driving stage for the InP amplifier (Fig. 6.19). The CMOS chip is similar to the one discussed in [77]. The InP power amplifier is a bare die without any pillars on it. We used the wirebond for the InP power amplifier

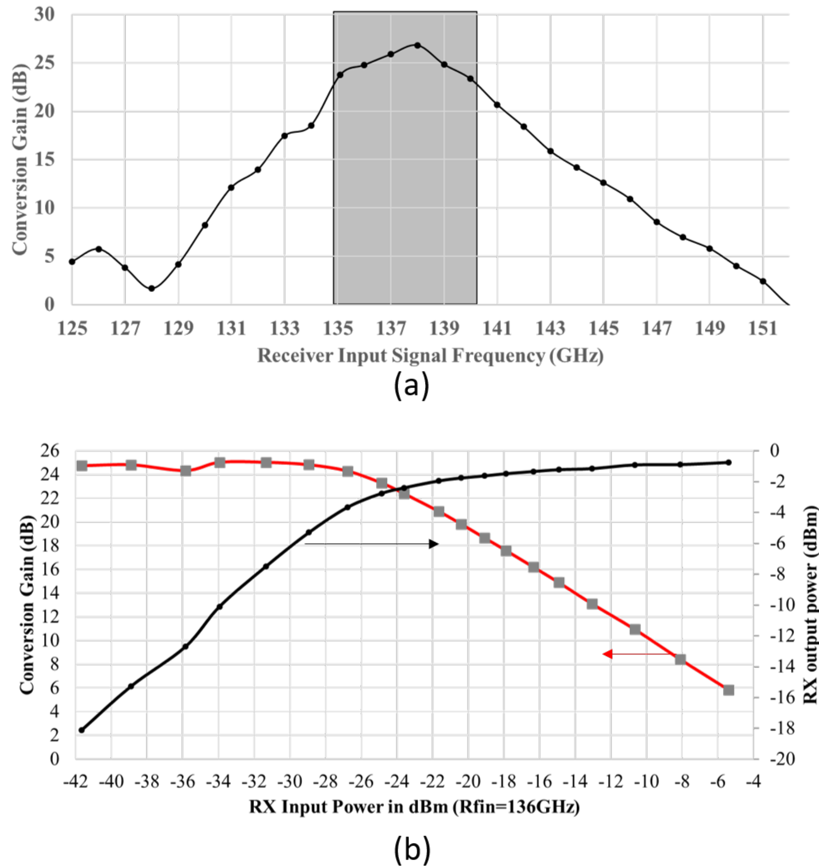

Figure 6.17: Packaging results for 135GHz receiver with copper pillar transition: a) Receiver conversion gain versus the output frequency. b) Measured receiver's output power versus the input power, including the copper pillar transition loss.

transition since this was the available approach. The wirebond challenges were discussed in Section 6.5.1.

6.11.1 Wirebond transition

Fig. 6.20a shows the HFSS model for the wirebond transition. There is a minimum wirebond pad area to bond the wirebond defined by the assembly house. This prevents us from getting good impedance. The S-parameters simulations are shown in Fig. 6.20b. The impedance is close to the edge of the smith chart which means that it is hard to

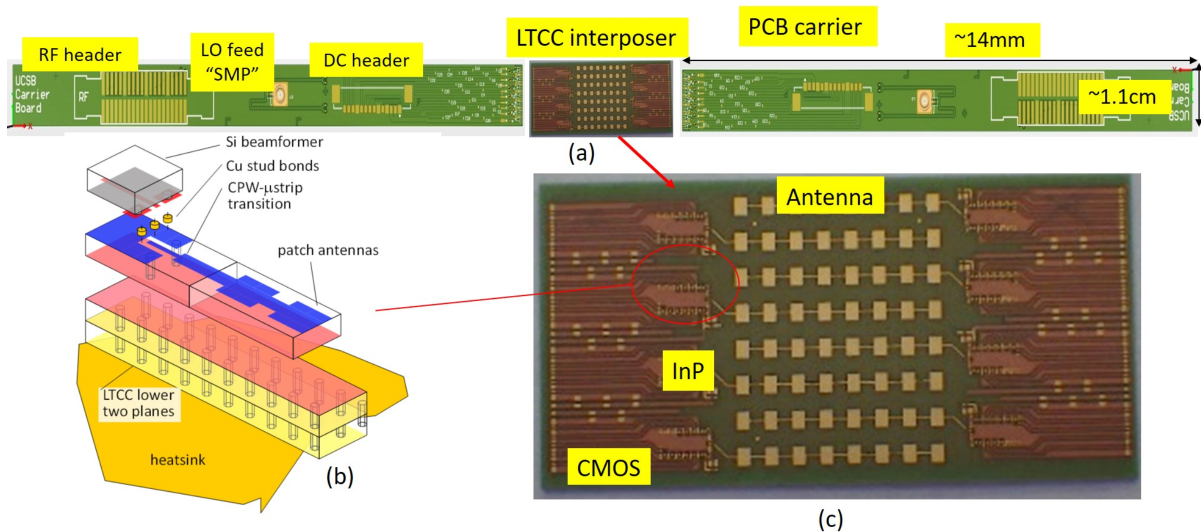

Figure 6.18: a) Photos for the receiver module showing the LTCC ceramic interposer and PCB carrier board. b) Cartoon drawing for the CMOS receiver chip to the interposer showing the different type of transitions. c) Close look on the LTCC ceramic interposer showing the antenna arrays and chip footprints.

match and sensitive. Yet this was the available option at that time.

6.11.2 Thermal Consideration

Power amplifiers dissipate a lot of heat (∼1W). The best approach is to directly mount the power amplifier on a piece of copper (Fig. 6.21a). However, this requires creating a cavity in the LTCC dielectric (Fig. 6.5a). The assembly company could not precisely control the cavity tolerance, so we could not use this approach. The other approach that we have done is to mount the chip on the top of the interposer (Fig. 6.5b and Fig. 6.19b). Mounting the chip on a ceramic does not act as a good heatsink since ceramic has poor thermal conductivity. Our solution is to use thermal vias (Fig. 6.21b) provided by Kyocera. Fig. 6.21 shows a simplified thermal model in ADS. We compared dissipating 1W in the best case (copper) (Fig. 6.21a) versus mounting the chip on a ceramic layer without thermal vias Fig. 6.21b and finally mounting the amplifier on

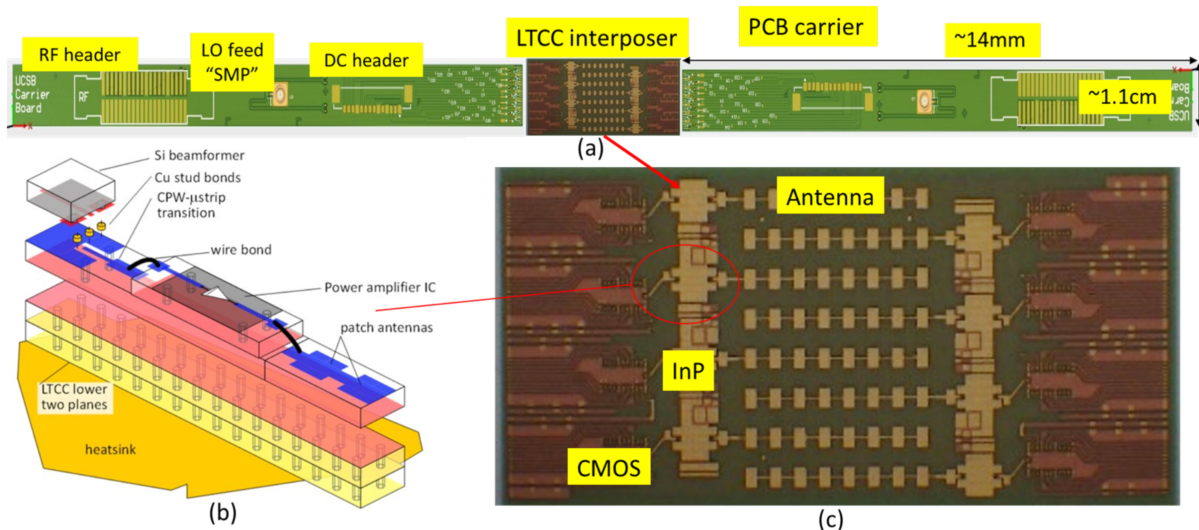

Figure 6.19: a) Photos for the high-power transmitter module (CMOS with InP PAs) showing the LTCC ceramic interposer and PCB carrier board. b) Cartoon drawing for the CMOS transmitter and InP chips to the interposer showing the different type of transitions. c) Close look on the LTCC ceramic interposer showing the antenna arrays and InP and CMOS chips footprints.

ceramic with thermal vias (Fig. 6.21c). We can see that the thermal vias succeeded to reduce the temperature which improves thermal dissipation.

6.11.3 InP PA to Antenna and CMOS Transition

Fig.6.22a shows a photo for the CMOS and InP chip footprint with the antenna array. We used cascaded sections of transmission lines with different widths for the matching purpose. Fig. 6.22b shows the S-parameters for the InP to CMOS chips. The loss is ~2.6dB at 135GHz. Fig. 6.22c shows the antenna gain and S_{11} versus frequency. The antenna has a simulated 12.2dBi of gain. The assembly is still in progress for this module.

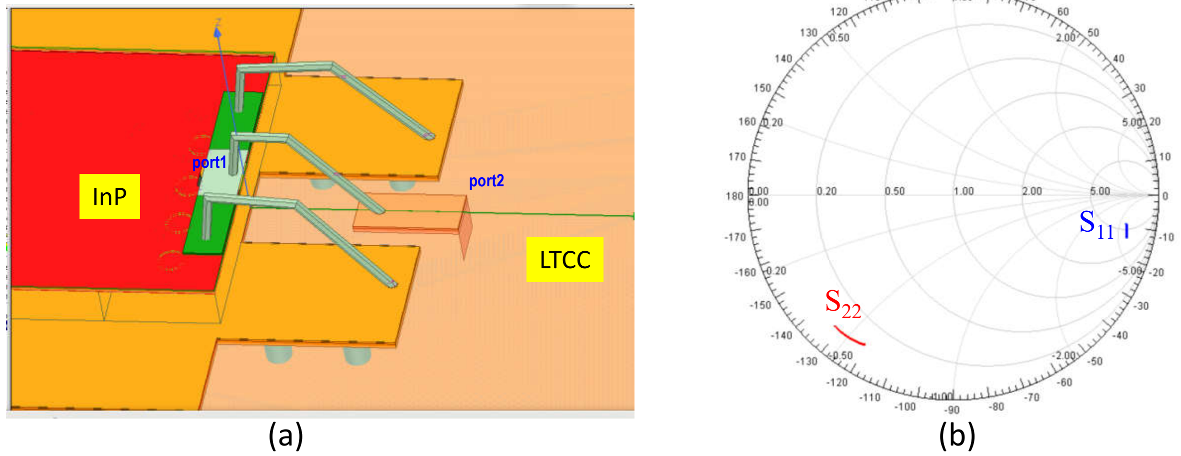

Figure 6.20: a) HFSS model for the wirebond transition. b) Simulated S-parameters.

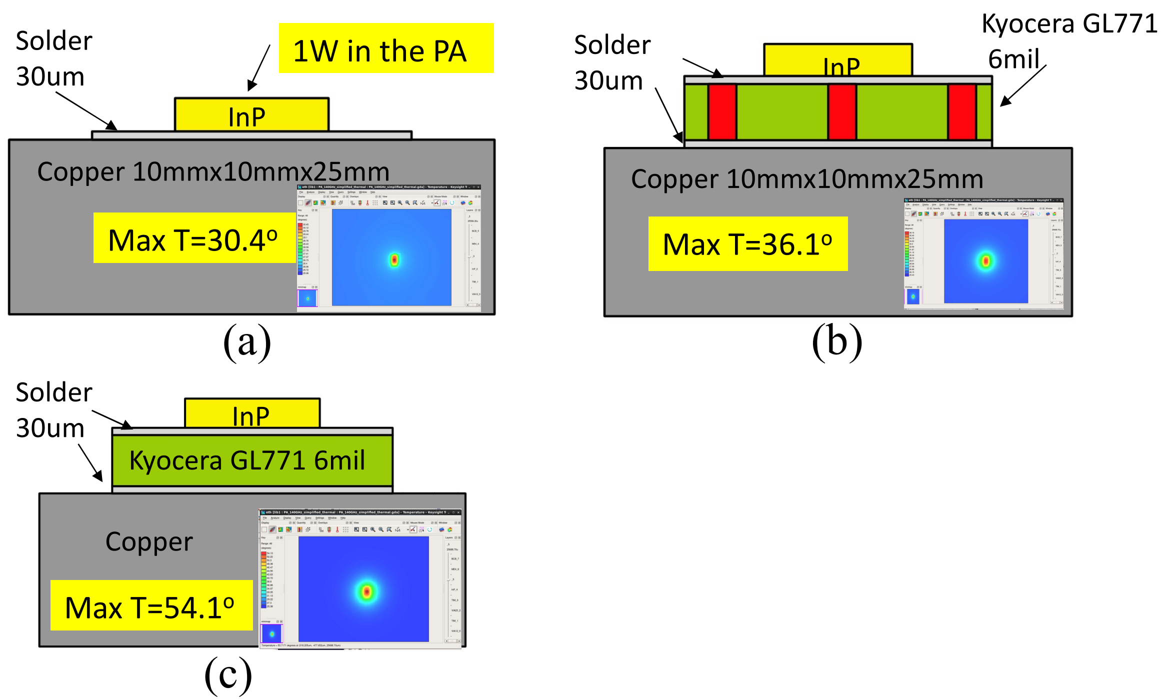

Figure 6.21: Thermal simulation: a) Amplifier is mounted directly on a copper block. b) Amplifier is mounted on ceramic layer with thermal vias. c) Amplifier is mounted on ceramic piece without thermal vias.

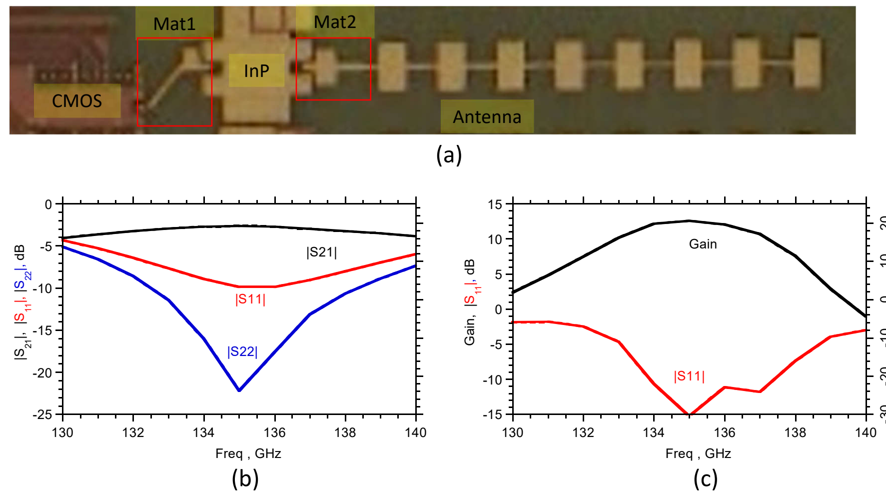

Figure 6.22: a) CMOS integrated to an InP chip and an eight-element series-fed patch antenna. b) Simulated S-parameters for the transition between InP and CMOS chips. c) Simulated antenna gain and the input reflection coefficient.

Chapter 7

Conclusions and Future Work

This thesis presented the key components of building a mm-wave communication system. Millimeter-wave power amplifiers are the key components in any transmitter. We covered the design fundamentals then we proposed a network theory for the design. The proposed network theory introduces an amplifier design framework using two-port network techniques. The proposed theory involves different degrees of freedom such as stacking concept and area progression techniques. We represented the design procedures by equations and graphical representations which give lots of design intuition and great depth for the design tradeoffs.

We presented lots of fabricated amplifiers with record results at 140GHz, 210GHz, and ∼300GHz. This shows that it is feasible to get moderate power with reasonable efficiency at these high frequencies which is necessary for long-range communication. We covered the design key features to achieve those results. We discussed the design degrees of freedom and selection criteria. The selection of the power, driver, and combiner cells have been shown in great depth.

We also moved from the chip level to the packaging level. Millimeter-wave packag-

ing is one of the main challenges to demonstrate a real communication system. We demonstrated a 140GHz packaged solution where we integrated CMOS chips to a patch array. There is still ongoing assembly work to build the tile with eight transmitters or receivers. Once we have the tile, the communication teams can use it for more advanced measurements, and algorithms and real deployment.

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