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Regrown Extrinsic Base InP HBT with Sub-100nm Emitter Contact

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by

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Abstract

Regrown Extrinsic Base InP HBT

with Sub-100nm Emitter Contact

by

Yihao Fang

This work presents the efforts pursued to optimize InP HBTs for power amplifiers above 100 GHz. Emitter width W_e reduction to sub-100nm dimension is achieved using a novel cosputtered $Ti_{4wt\%}W$ emitter metal, and high power ICP dry etching. The cosputtering process enables fine-tuning of TiW alloy composition for vertical dry etch profile along sidewalls of the 600nm tall emitter metal, retaining sub-100nm emitter width from top to bottom. Base contacts are formed by low-temperature MOCVD regrowth (490 °C) of thick p-GaAs ($> 4 \times 20\, cm^{-3}$) extrinsic base on the intrinsic p-InGaAs or p-GaAsSb base layer, and subsequent UV i-line lift-off of e-beam deposited Pt/Ti/Pd/Au metal stack. Low overall base contact resistivity $\rho_{b,c}$ is extracted by TLM on scaled sub-100nm W_e DC "large area" devices to be $0.98 \pm 0.4\Omega$-um^2, which meets the requirement for >2THz f_{max} scaling. The larger bandgap of p-GaAs allows direct abutment of the regrown extrinsic base against sides of the n-InP emitter semiconductor, while blocking undesired electron injection into the extrinsic base. The extended regrown extrinsic base, thus, lowers R_{gap} by a factor of >2 between the base contact metal and emitter semiconductor, a significant contributor to R_{bb} in deep submicron HBTs, thanks to the much lower sheet resistance of the extrinsic base ($\rho_{s,ex} < 300\Omega/\square$). Hydrogen passivation of carbon dopants in the p-InGaAs intrinsic base layer is found, and partially reversed with an in-situ N_2 anneal in MOCVD before temperature ramp down. Lateral hydrogen out-diffusion is believed to limit carbon dopant reactivation as the smallest W_e devices showed the lowest apparent intrinsic base sheet resistance ($\rho_{s,in} = 1900\Omega/\square$) after the

N_2 anneal. While the added base spreading resistance R_{spread} underneath emitter semiconductor is manageable in sub-100nm W_e devices, DC devices with a GaAsSb intrinsic base are studied as a passivation-proof alternative to InGaAs for maximum R_{bb} scaling. Collector-base capacitance C_{cb} scaling is intentionally excluded in this work, so is vertical epitaxial scaling for higher f_T, as both face challenges in terms of lithographic and semiconductor doping limits. RF device integration faced tremendous logistic difficulties due to the pandemic lockdown. Nevertheless, working RF devices with f_{max} in excess of 300GHz are demonstrated. In addition, a detailed review of conventional InP HBT scaling roadmap shows drawbacks of continued C_{cb}, and f_T scaling in sub-100nm W_e process (e.g., high R_{gap}, and stagnating C_{cb}) previously overlooked due to simplified assumptions. It can be shown that conventional beyond-130-nm technology nodes offer comparable or worse device performance, a trend that can be reversed by the insertion of the regrown extrinsic base process module already a reality in SiGe HBT.

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Chapter 1

Introduction

This chapter reviews current transistor technologies in both Si and III-V material systems, and state-of-the-art RF amplifier circuits at 28-39 GHz and > 100 GHz. Despite progress in device current gain cut-off frequency f_T and maximum power gain cut-off frequency f_{max}, circuit-level performance gains, in terms of saturated output power P_{sat} and power-added efficiency PAE, have so far eluded requirements for widespread commercialization – e.g. $P_{sat} > 30$ dBm, and $PAE_{6dB-backoff} > 30\,\%$ for power-constrained user equipment. An analysis of f_T, f_{max}, and Johnson's figure of merit $JFOM$ reveals their limited suitability at guiding device scaling for RF applications. A new pair of parameters $f_{50\Omega}$ and $P_{sat-50\Omega}$ are proposed to better assess a technology's RF potential within a given frequency band, and help guide further device optimization.

1.1 Transistor Technologies for RF Power Amplifiers

Indium phosphide heterojunction bipolar transistors achieve higher f_T/f_{max} than other transistor technologies at a given lithographic feature size. Current state-of-the-art 130 nm InP HBT exhibits f_T/f_{max} in excess of 0.52/1.1 THz [1]. Current record high PAE

and P_{sat} RF power amplifiers above 100 GHz are all demonstrated in a 250 nm InP process [2, 3, 4]. Yet, InP HBT has seen little widespread commercialization apart from niche applications in defense and test instrumentation [5, 6], and certainly not in commercial RF communication. The lack of commercial InP processes might be attributed to the higher cost compared to their GaAs counterparts [7]. From a performance perspective, however, for sub-10 GHz RF PA, the mature 250 nm 350/700 GHz f_T/f_{max} InP HBT provides a similar maximum stable gain $MSG \sim 30$ dB and a less than half normalized saturated power density $\frac{P_{sat}}{L_E} \sim 1.5$ mW/μm compared to a 50/175 GHz f_T/f_{max} GaAs HBT from the 1980s [2, 8]. While f_T/f_{max} do provide the upper limit at which power amplification is possible, f_T/f_{max} *alone* are inadequate in predicting RF power amplifier performance *in a given technology*.

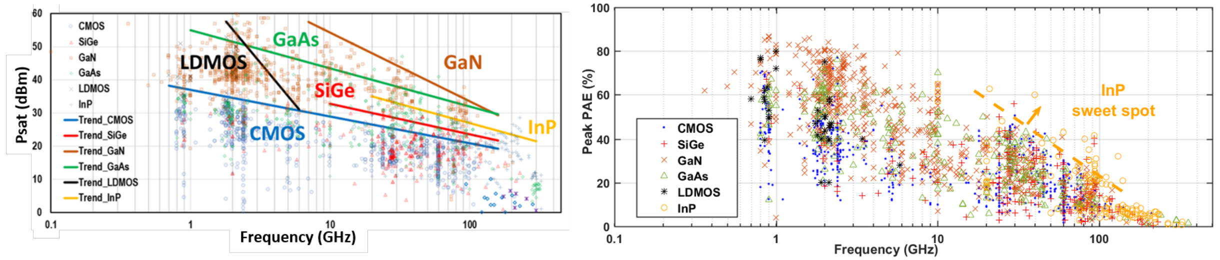


Figure 1.1: RF PA P_{sat} (left), and peak PAE (right) vs. frequency in various processes [9]

Si CMOS, Si LDMOS, SiGe HBT, GaAs HBT, GaAs HEMT, and more recently GaN HEMT with lower f_T/f_{max} have dominated the commercial sub-10 GHz RF PA arena both in terms of P_{sat} and peak PAE (Fig. 1.1) [9]. A widely accepted parameter that evaluates the promise of a transistor technology for RF power amplification – Johnson's figure of merit $JFOM$ – is the product of the charge carrier saturation velocity v_{sat} in a semiconductor and the dielectric strength $E_{breakdown}$ under same applied bias [10]. Equivalently, $JFOM$ is $f_T \times BV$, where BV is the breakdown voltage of the transistor. Fig. 1.2 (left) shows BV vs. f_T for the aforementioned transistors [12]. Despite a high

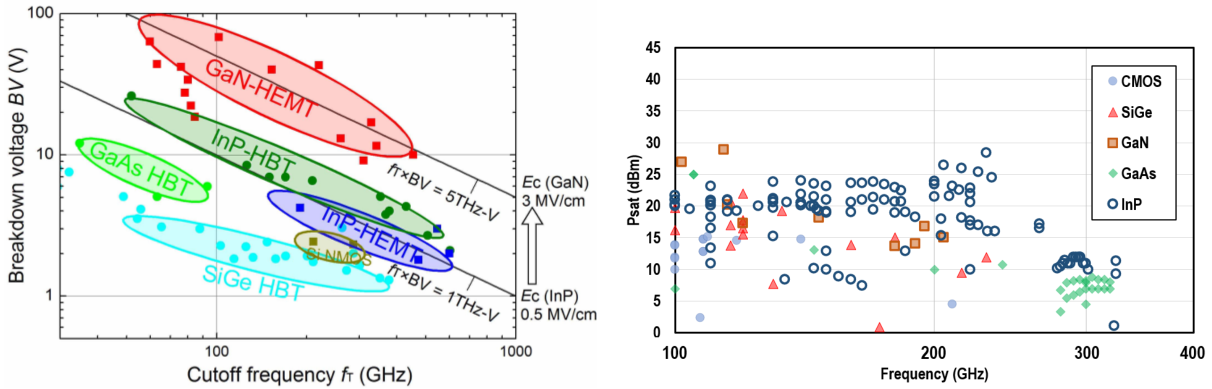


Figure 1.2: BV vs. f_T with $JFOM$ asymptotes (left) [11]; P_{sat} vs. frequency > 100 GHz (right) [9]

$JFOM$ and sufficient f_T/f_{max}, GaN HEMT does not currently offer superior saturated output power P_{sat} or power added efficiency PAE between 100 - 300 GHz (Fig. 1.1 & 1.2). Other factors such as electromagnetic limits on realizable cell sizes, optimal power matching impedance Z_{OPT}, maximum power gain impedance Z_{conj}, and availability of efficient power combining should be considered for RF power amplifier applications where P_{sat} and PAE are of chief concern.

1.2 f_T & f_{max} Scaling, $JFOM$, and $P_{sat-50\Omega}$

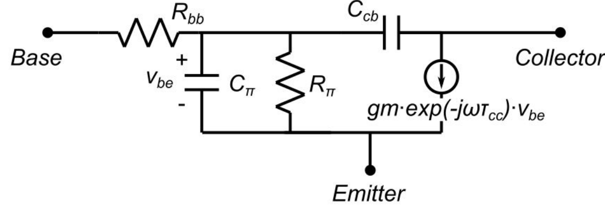


Figure 1.3: Basic hybrid-π small-signal model of an HBT

A bipolar junction transistor[i] represented by the hybrid-π model in Fig. 1.3 has a high frequency short-circuit current gain h_{21} as followed, assuming $R_\pi \gg \frac{1}{j\omega C_\pi}$

$$h_{21} = \frac{i_{out}}{i_{in}} \approx \frac{g_m - j\omega C_{cb}}{j\omega(C_\pi + C_{cb})} \tag{1.1}$$

Current gain cut-off frequency f_T is defined as the frequency at which $|h_{21}| = 1$. Thus, when $\omega \gg g_m/C_{cb}$, we have

$$f_T = \frac{g_m}{2\pi(C_\pi + C_{cb})} \tag{1.2}$$

Using $g_m = \beta/R_\pi$ where β is the DC current, and because g_m is proportional to the slope of the exponential emitter-base I-V characteristics, we have

$$\frac{1}{2\pi f_T} = \frac{1}{g_m}(C_{je} + C_{cb} + C_{b,t} + C_{b,\Delta Q_c}) = \frac{1}{g_m}(C_{je} + C_{cb}) + \frac{1}{g_m}(C_{b,t} + C_{b,\Delta Q_c}) \tag{1.3}$$

$$= \underbrace{\frac{1}{g_m}(C_{je} + C_{cb})}_{\propto \text{junction areas}} + \underbrace{\frac{1}{\beta}(\tau_b + \tau_C)}_{\propto \text{electron transit times}} \tag{1.4}$$

where C_{je} and C_{cb} are the junction capacitances of the emitter-base and base-collector junctions. $C_{b,t}$ and $C_{b,\Delta Q_c}$ are differential capacitances due to charging of electrons in the base (charge control) terminal. τ_b and τ_c are the base and collector electron transit

[i] or a MOSFET, or any charge control transistor device

times. f_T scales with smaller junction areas and thinner device structure for faster electron transit times. In an HBT, these correspond to lateral lithographic scaling, and vertical epi scaling as detailed in [13].

Therefore, a 2:1 increase in f_T leads to a constant maximum current per emitter length I_{max} (mA/μm), and a 1:2 scaling in maximum voltage V_{max} (V) due to a 1:2 scaling in the collector thickness.[ii] On a per emitter length basis, this corresponds to a 1:2 scaling in loadline impedance, and a 1:2 scaling in output power. To maintain a constant optimal power matching Z_{OPT} for a PA power cell, the emitter finger length must be scaled by 1:2, for a 1:4 scaling in P_{sat}.

Corollary 1: Higher f_T leads to *smaller* PA cell sizing for a given Z_{OPT}

The power gain cut-off frequency f_{max} is defined as the frequency at which the transistor has unity power gain. A transistor modeled by a single-pole system shows a -6 dB/octave roll-off in its Mason's unilateral power gain up to f_{max} [16]. In reality, transistors are not single-pole systems and have "non-dominant" poles and often zeros at high frequencies [17, 18]. Consider again the single-pole transistor model in Fig. 1.3 represented by its Z-parameters

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = Z_S + Z_A \tag{1.5}$$

where Z_{21} may or may not be equal to Z_{12}. The matrix can be separated into a symmetric part Z_S where $Z_{S,ij} = Z_{S,ji}$ for $i \neq j$, and an associated antisymmetric part where Z_A where $Z_{A,ij} \neq Z_{A,ji}$ for $i \neq j$. It can be shown that any lossless passive (reciprocal) embedding N around Z can only perform one or a combination of the following elemental

[ii]This is a pessimistic position because it ignores velocity overshoot effects in highly scaled devices. Measured V_{max} in modern bipolar and FET devices scales sublinearly with regard to f_T [13, 14, 15].

operations

$$\text{Real transformation: } Z' = n\,Z\,n^T \tag{1.6a}$$

$$\text{Reactive padding: } Z' = Z + j\chi \tag{1.6b}$$

$$\text{Inversion: } Z' = Z^{-1} \tag{1.6c}$$

where n in Eq. 1.6a is the real transformation matrix. n can be, for instance, constructed with quarter-wavelength transmission lines for impedance transformation. One important n is the permutation matrix n_{perm}

$$n_{perm} = \begin{bmatrix} 1 & -1 \\ 0 & -1 \end{bmatrix} \tag{1.7}$$

which rotates the original Z matrix to obtain Z' (Fig. 1.4). From a circuit perspective, n_{perm} links the common-emitter, common-base, and common-collector configurations.

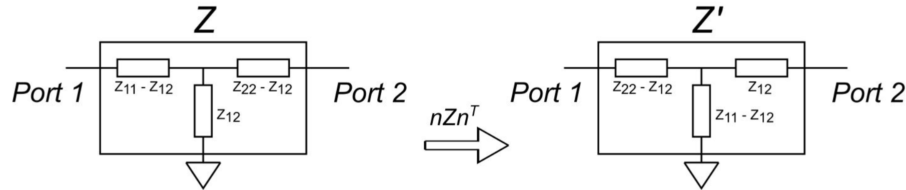


Figure 1.4: $Z' = n_{perm}\,Z\,n_{perm}^T$ rotates the three terminals counter-clockwise

χ in Eq. 1.6b is the *passive* reactance padding matrix with $\chi_{ij} = \chi_{ji}$. Therefore, for any Z, one has

$$(Z + j\chi) + \overline{(Z + j\chi)} = Z + \overline{Z} = \text{invariant w.r.t. Eq. 1.6b} \tag{1.8}$$

$$(Z + j\chi) - (Z + j\chi)^T = Z - Z^T = \text{invariant w.r.t. Eq. 1.6b} \tag{1.9}$$

Equivalently, padding a transistor with ideal lossless reactive embedding will not change its $Z+\overline{Z}$ or $Z-Z^T$. Note, however, that $Z+\overline{Z}$, and $Z-Z^T$ are not the original Z, and, thus, do *not* represent the original device as included reactances of the original device cannot be inferred from either expression. Any expression also stays invariant with regard to Eq. 1.6a must be of the form $f[(Z+\overline{Z}),(Z-Z^T)]$. One such matrix found by Mason was $\Delta[Z-Z^T]/\Delta[Z+\overline{Z}]$ because

$$\Delta[(n(Z-Z^T)n^T)(n(Z+\overline{Z})n^T)^{-1}] = \Delta[n]\cdot\Delta[Z-Z^T]\cdot\Delta[(Z+\overline{Z})^{-1}]\cdot\Delta[n^{-1}] = \Delta[Z-Z^T]\cdot\Delta[Z+\overline{Z}]^{-1} = \text{invariant w.r.t. Eq. 1.6a, 1.6b} \quad (1.10)$$

Finally, because $\{\Delta[Z-Z^T]/\Delta[Z+\overline{Z}]\}^{-1} = -\Delta[Z-Z^T]/\Delta[Z+\overline{Z}]$, we arrive at the Mason's unilateral gain U

$$U = \frac{\left|\Delta(Z-Z^T)\right|}{\Delta(Z+\overline{Z})} = \text{invariant w.r.t. Eq. 1.6a, 1.6b, 1.6c} \quad (1.11)$$

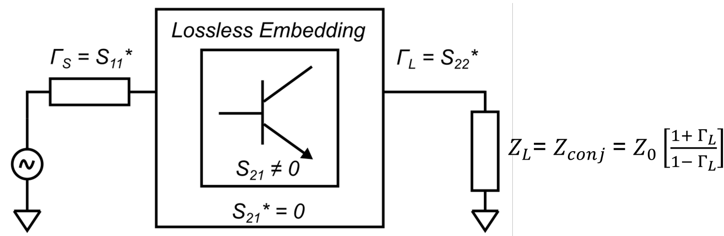


Figure 1.5: Maximum power gain matching for U that requires Z_{conj} load matching

Physically, U can be achieved by methodically embeddding a transistor in one configuration (CE for example) with lossless matching networks, rotating it to other configurations and matching again to get an overall real $Z_{overall}$ before transforming it to the 50 Ω environment with quarter-wave transformers. f_{max} is derived at the frequency where $U=1$. Therefore, a high f_{max} does not guarantee a high power gain as the required

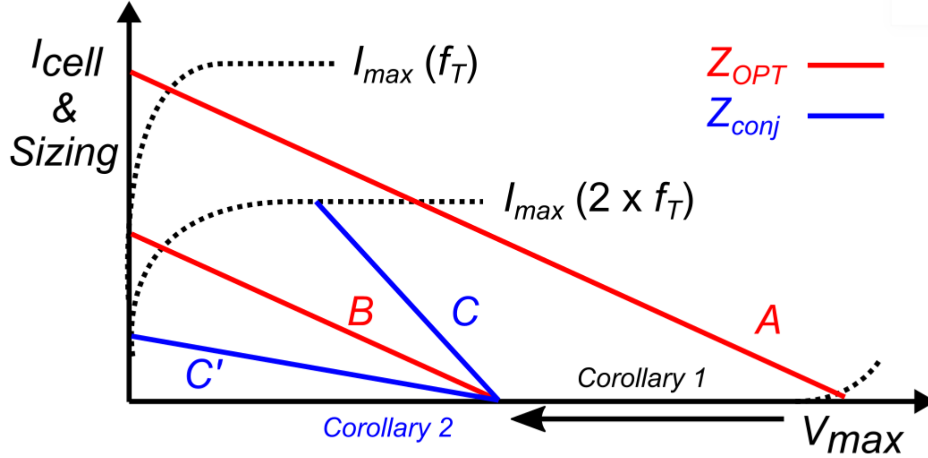


Figure 1.6: A $2 \times f_T$ shifts loadline A to B for a 1:4 P_{sat} (Corollary 1), and the mismatch between loadlines B and C & C' due to mismatch between Z_{conj} and Z_{OPT} (Corollary 2)

Z_{conj} could be rather complex, and may or may not overlap with Z_{OPT} (Fig. 1.5). The power gain under optimal load matching Z_{OPT} is the operating gain G_P and is usually less than or equal to U extrapolated from f_{max}.[iii] Therefore, we have

Corollary 2: Gain extrapolated from f_{max} corresponds to Z_{conj}, not necessarily Z_{OPT}

When G_P is less than U due to the mismatch between Z_{conj} and Z_{OPT}, $PAE \propto \frac{1}{1-G_P}$ is less than that suggested by U extrapolated from f_{max}. Loadline C in Fig. 1.6 corresponds to $Z_{conj} < Z_{OPT}$, where the transistor is *current-limited*. A current-limited transistor would benefit from an increase in I_{max} if V_{max} can be kept constant. On the other hand, loadline C' corresponds to $Z_{conj} > Z_{OPT}$, where the transistor is *voltage-limited*. A voltage-limited transistor would benefit from an increase in V_{max} if I_{max} can be kept constant. In Section 1.5, it will be shown that whether a transistor is current- or voltage-limited is independent of its finger-length and Z_{OPT}.

Because the feasible load impedance realizable on wafe is constrained, loadlines A & B in Fig. 1.6 cannot be of arbitrary impedance. Calculated characteristic impedance Z_0

[iii] In general, $G_P \le G_{max} = (2U-1) + 2\sqrt{\frac{U}{U-1}} \approx 4U$ at a frequency well below f_{max} [19]. But G_{max} approaches unity at f_{max} as well.

of a microstrip transmission line embedded in various materials and of common aspect ratios is tabulated in Table 1.1 [20]. For ILDs on the order of a few μm, reasonable Z_0 is between 20 Ω and 150 Ω, with a geometric mean very close to the 50 Ω standard impedance.

		Aspect ratio (w/h)					
		0.1	1	2	3	5	10
ε_r	2.2 (PTFE)	204	95	66	51	36	20
	2.6 (BCB)	192	89	61	48	33	19
	4 (SiO)	162	74	51	39	27	15
	8.9 (GaN)	114	51	35	27	18	10
	11.7 (Si)	101	45	31	24	16	9
	12.5 (InP)	98	44	30	23	16	9
	12.9 (GaAs)	96	43	30	23	16	9
							Z_0 (Ω)

Table 1.1: Calculated Z_0 of microstrip transmission lines in common materials with reasonable aspect ratios

Loadline impedances of power cells in RF PAs operating close to or above 100 GHz in different transistor technologies are within the 20-150 Ω range readily realizable on wafer, with III-V & nitride FETs closer to the high end, while HBTs and CMOS closer to 50 Ω [2, 3, 4, 21, 22, 23, 24]. With a typical 50 μm substrate and a low g_m forbidding the use of ILDs, III-V & nitride FETs' closer to 100 Ω loadline impedance matches the calculated values in Table 1.1.

The combined effect of Collorary 1 & Collorary 2 and realizable $Z_0 \approx 50$ Ω, therefore, determines cell sizing in an RF PA. Cell sizing is *not* a free variable in RF PA design. In an RF PA, a 2:1 scaling in f_T implies a 1:2 scaling in PA cell size, reducing P_{sat} of the power cell. Here $P_{sat-50\Omega}$ is defined as the saturated output power of a PA cell with a sizing that matches 50Ω. $P_{sat-50\Omega}$ of 3 generations of InP HBT [1, 13, 25], record GaN HEMT [26], Globalfoundries 45RFSOI [27], and IBM 90nm SiGe HBT [28] are given in Table 1.2. Although a large V_{max} leads to higher $P_{sat-50\Omega}$ in a 50 Ω PA cell as suggested

Technology	250 nm InP HBT	130 nm InP HBT	60 nm* InP HBT	75 nm GaN HEMT	45RFSOI CMOS	90nm SiGe HBT
I_{max} (mA/μm)	3	3	3	1.6	0.65	3
V_{max} (V)	4.2	3.5	2.5	40	2.4	1.8
V_{knee} (V)	0.6	0.6	0.5	1	0.3	0.2
$P_{sat-1\mu m}$ (mW)	1.4	1.1	0.8	7.8	0.17	0.6
$Z_{L-1\mu m}$ (Ω)	1200	970	700	24300	3200	550
50 Ω cell size (n×L-μm)	4×6	4×5	4×3.5	13×37.5	64×1	11×1
$P_{sat-50\Omega}$ (dBm)	15.1	13.4	10.2	35.8	10.4	8.2

*: Extrapolated

Table 1.2: $P_{sat-50\Omega}$ of 3 generations of InP HBT vs. competing RF technologies

by $JFOM$, the transistor size required in such PA cell could be a concern due to its ratio to the electrical length the associated RC delay [29].

In section 1.3, a second parameter, $f_{50\Omega}$, related to $P_{sat-50\Omega}$ is introduced in an attempt to explain the observed dominance of PA in InP HBT at > 100 GHz.

1.3 $f_{50\Omega}$ – Lumped or Distributed Element?

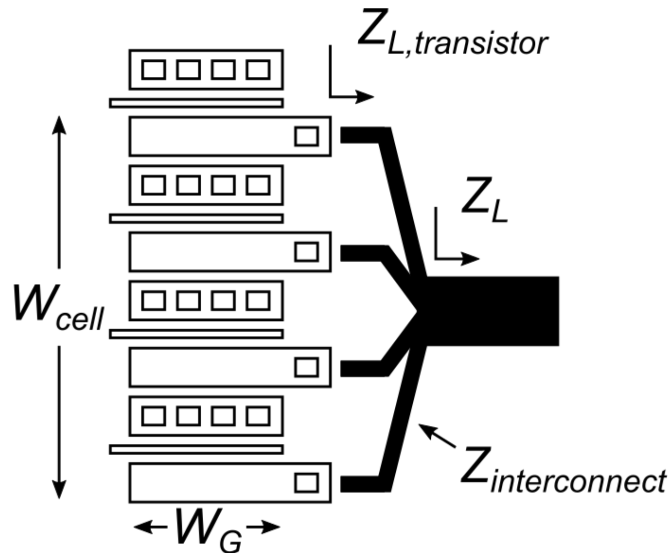


Figure 1.7: Schematic of a CMOS PA cell with only output wiring shown for clarity

A power cell in an RF PA is treated as a lumped element in elementary analysis. Because interconnect wiring between parallel devices is of variable length, the impedance presented to each transistor finger $Z_{L,transistor}$ is not identical. To maintain a consistent overall Z_L and $Z_{L,transistor}$ the interconnect needs to be much shorter than a wavelength [30]. Therefore, maximum cell width is limited by the phase and impedance differences between the outer and inner transistors in 1.7. For efficient power delivery $> 90\%$, amplitude sum of the outer and inner transistors $exp(-j\frac{\phi_{mismatch}}{2})+exp(j\frac{\phi_{mismatch}}{2})$ should be $> 95\%$, leading to a maximum electrical length of $1/10\,\lambda$ for $\frac{1}{2}W_{cell}$. Depending on design tradeoffs, W_{cell} can be adjusted for a higher P_{sat} at the expense of a lower PAE. Fig. 1.8 shows the drop in power delivery efficiency of a 4-transistor cell shown in the previous schematic as a function of W_{cell} due to phase mismatch. For the purpose of guiding device optimization, P_{sat} vs. PAE tradeoff is not considered, and a fixed $W_{cell} = 1/5\lambda$ is used for analysis. Therefore, $W_{cell} \propto 1/f$.

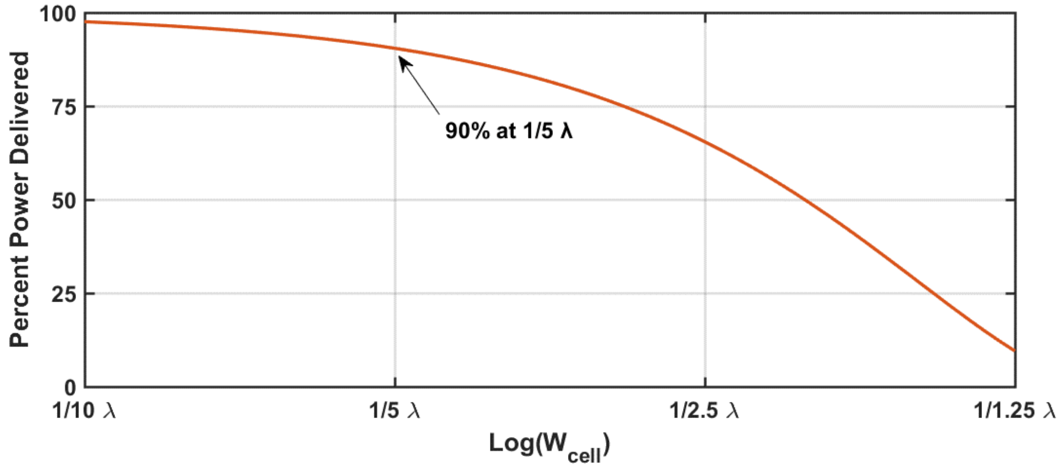


Figure 1.8: Tradeoff between power delivery efficiency vs. power cell width W_{cell} due to phase mismatch

Similarly, transistor finger length W_G is ultimately limited by the electrical length of electromagnetic waves in materials. Therefore, $W_G \propto 1/f$, and is limited to $1/10\lambda$ for the

analysis. One subtlety exists for transistors with high feed resistance – e.g. poly-gated Si CMOS with gate sheet resistance on the order of 10 $\Omega/_\square$ [31]– where distributed RC delay along the finger length dominates. Because $R \propto W_G$ and $C \propto W_G$, $W_G \propto 1/\sqrt{f}$ in transistors with a high feed resistance. Given that

$$I_{cell,max} \propto W_G \times W_{cell} \tag{1.12}$$

$$P_{sat} = \frac{1}{8} I_{cell,max}^2 Z_{OPT} \tag{1.13}$$

$$Z_{OPT} = 50\,\Omega \tag{1.14}$$

we have $P_{sat-50\Omega}(f) \propto 1/f^4$ in general, and $P_{sat-50\Omega}(f) \propto 1/f^3$ for high feed resistance transistors as shown in Fig. 1.9.

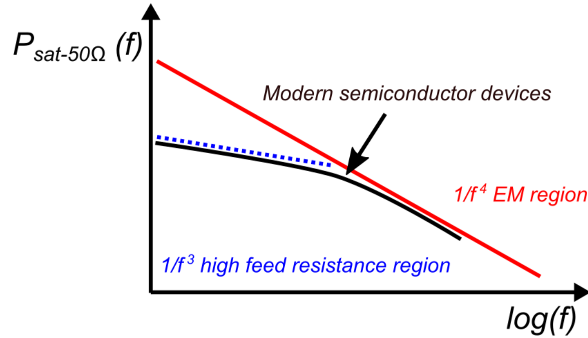


Figure 1.9: $P_{sat-50\Omega}$ as a function of frequency for high feed resistance transistors (Si CMOS), and low feed resistance transistors (III-Vs)

Since $P_{sat-50\Omega}(f)$ is a function of the PA operating frequency, maximum $P_{sat-50\Omega}$ defined in previous section corresponds to a characteristic frequency, $f_{50\Omega}$, defined as the frequency at which full voltage swing of the transistor is utilized. At frequency greater than $f_{50\Omega}$, the PA power cell is current-limited, and cannot access its full voltage supporting capability as shown in Fig. 1.10.

$f_{50\Omega}$ of transistors found in Table 1.2 are calculated by first finding the minimum spacing between transistor fingers due to thermal and resistive effects [32, 33, 34], and

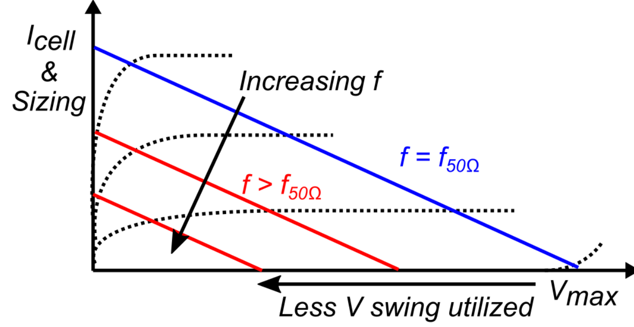


Figure 1.10: I_{cell} decreases in proportion to cell sizing with constant I_{max} at frequency above $f_{50\Omega}$, whereas V_{cell} becomes less than transistor V_{max}

then balancing W_G and W_{cell} to fit into a $1/10\lambda \times 1/5\lambda$ area. Finally, $f_{50\Omega} = \frac{c_0}{\lambda\sqrt{\varepsilon_r}}$. Effective dielectric constant for microstrip transmission line on GaN is assumed to be 6.0, 2.6 for transmission line in BCB on InP [20], and 3.8 for transmission line in SiO_x on Si. The results are given in Table 1.3.

With the exception of GaN HEMT, all other transistor technologies have $f_{50\Omega}$ in excess of their f_T/f_{max}. In other words, InP HBT, 45RFSOI, and SiGe HBT are voltage-limited and would benefit from a higher breakdown voltage if possible. GaN HEMT, on the other hand, is current-limited even for the record 75 nm devices above 75 GHz. To operate above 100 GHz, mature and larger node GaN HEMT processes must give up their higher breakdown voltage for a realizable loadline matching. The lack of high P_{sat} GaN HEMT PA above 100 GHz compared to InP HBT PA seen in Fig. 1.2 is, thus, explained.

In this section, it has been shown that by taking into account electromagnetic phenomena, GaN HEMT's higher $JFOM$ and breakdown voltage are not fully exploitable at > 100 GHz because of its low $f_{50\Omega}$ for realizable loadline matching. Compared to 45RFSOI, 90 nm SiGe HBT, and its smaller node counterparts, 250 nm InP HBT is less voltage-limited, and is more suitable for > 100 GHz PA applications. The first utility of $f_{50\Omega}$ is that it provides a quantitative measure for guiding both technology selection for

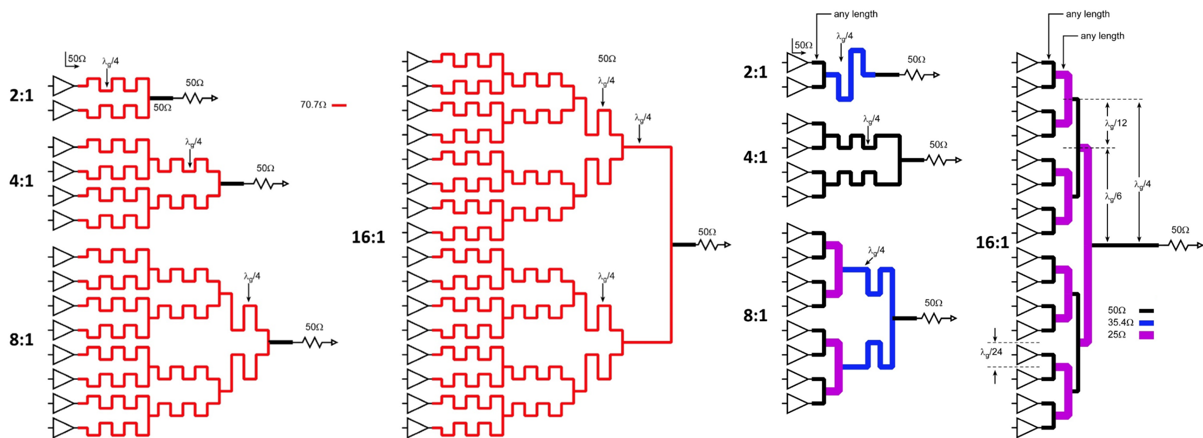
Technology	250 nm InP HBT	130 nm InP HBT	60 nm* InP HBT	75 nm GaN HEMT	45RFSOI CMOS	90nm SiGe HBT
$P_{sat-50\Omega}$ (dBm)	16.5	14	12	36	12	9.2
Finger pitch (μm)	6	5	4.5	25	0.5	1
$f_{50\Omega}$ (GHz)	1500	1800	2100	75	850	2400
Frequency Dependence	$1/f^{4\sim3}$	$1/f^{4\sim3}$	$1/f^{4\sim3}$	$1/f^{4\sim3}$	$1/f^{3}$	$1/f^{3}$

*: Extrapolated

Table 1.3: $f_{50\Omega}$ of 3 generations of InP HBT vs. competing RF technologies

PA design at a given frequency, and a direction device scaling should take to optimize for PA applications. In section 1.4, relation between $f_{50\Omega}$ and limit of efficient power combining using corporate power combiners are discussed.

1.4 Relation between Power Combining and $f_{50\Omega}$



*: Resistors omitted for Wilkinson combiners for clarity

Figure 1.11: Conventional Wilkinson N-way power combiners using $log_2(N)$ sections of $\lambda/4$ transmission line (left) vs. single-section $\lambda/4$ transmission line N-way corporate power combiners (right)

Efficient power combining of parallel power cells using single-section $\lambda/4$ transmission line N-way corporate power combiners are shown in Fig. 1.11. The advantage of

single-section $\lambda/4$ transmission line N-way corporate power combiners over conventional Wilkinson combiners is their lower loss shown in Fig. 1.12 [3, 4, 30]. The disadvantages are their limitations on port isolation, and power cell width W_{cell}. In the 16-way combined output network in Fig 1.11, W_{cell} must be less than $\lambda/24$ to fit within the layout.

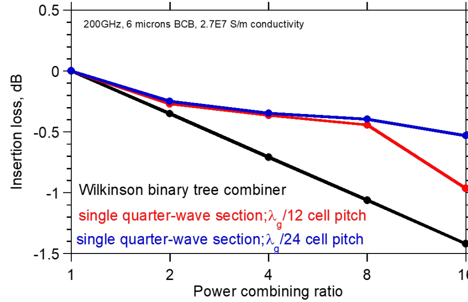


Figure 1.12: Loss of single-section $\lambda/4$ transmission line N-way corporate power combiners in typical BCB wiring environment in InP HBT

As discussed in section 1.3, a 50 Ω-matched PA cell in 250 nm InP HBT would be $\lambda/5$ wide at 1500 GHz, or its $f_{50\Omega}$. Therefore, at 140 GHz, the same cell would have an electrical width of $\frac{\lambda}{5} \times \frac{140\,\text{GHz}}{1500\,\text{GHz}} = \frac{\lambda}{50} \ll \frac{\lambda}{24}$ required for 16-way combining (Fig. 1.11), bringing P_{sat} of a 16-way combined PA in 250 nm InP HBT to potentially 28 dBm without increasing finger length. This is in good agreement with published 8-way combined 23 dBm results in 250 nm InP HBT [3].

For a PA operating at f_0, efficient N-way power combining is, thus, possible for $N \approx \frac{2\times f_{50\Omega}}{f_0}$ without incurring much of a power-combining penalty. Finally, Fig. 1.13 shows the theoretical P_{sat} of a PA in transistor technologies discussed above, including effects of electrical length and efficient single-section $\lambda/4$ transmission line power combining. Despite its low $f_{50\Omega}$ that excludes the use of power combining, GaN HEMT can provide more saturated output power than other technologies in realizable PA layout at 140 GHz and below. Though published PAs in InP HBT above 100 GHz have exhibited impressive

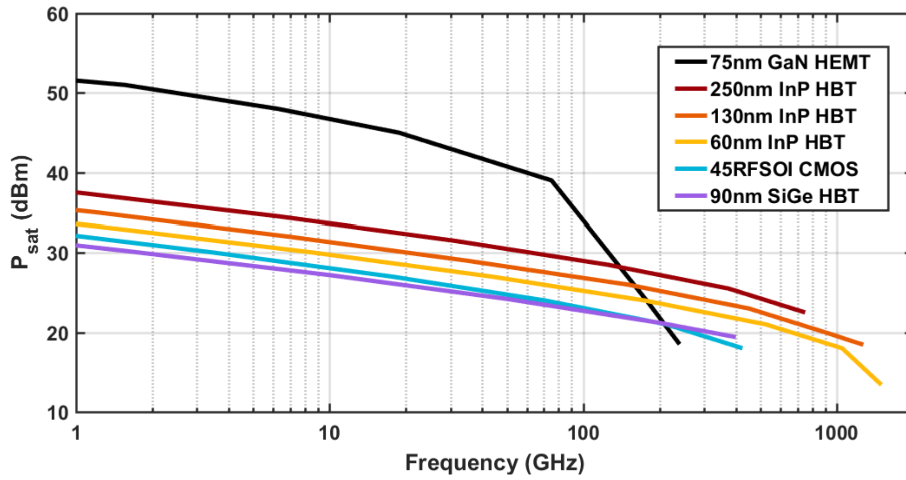


Figure 1.13: Theoretical P_{sat} of power-combined PA in various technologies up to corresponding f_{max}, including effects of $f_{50\Omega}$ and power combining (finger length is kept constant for low RC delay)

performance, it is at above ∼140 GHz InP HBT is more favored theoretically. It should be noted that both $P_{sat-50\Omega}$ and $f_{50\Omega}$ defined hitherto with the $\lambda/5$ cell size and RC delay limit are not hard limits on PA P_{sat}, but presents a benchmark for technology comparison.

1.5 Z_{conj} and Z_{OPT} Mismatch and PAE Limit

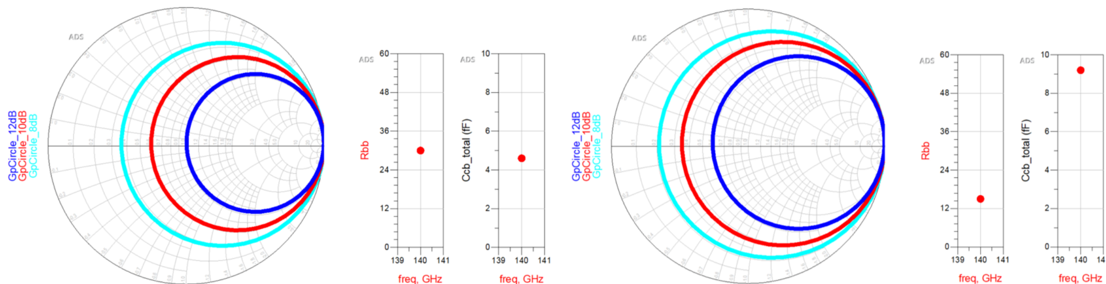


Figure 1.14: Common-emitter G_p circles of a 3 μm-long 250 nm InP HBT (left) vs. those of a modified HBT with half the R_{bb} and twice the C_{cb} (right)

A close overlap between the optimal power matching impedance Z_{OPT} and maximum

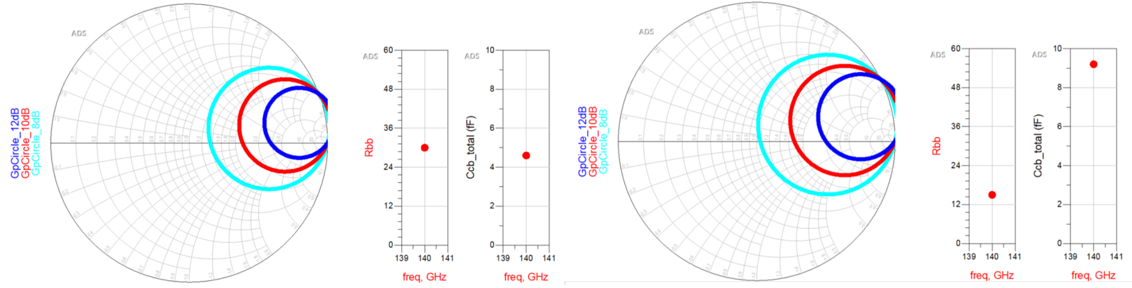


Figure 1.15: Common-base G_p circles of a $3\,\mu$m-long 250 nm InP HBT (left) vs. those of a modified HBT with half the R_{bb} and twice the C_{cb} (right)

power gain impedance Z_{conj} ensures G_P at an impedance $Z_{OPT} \neq Z_{conj}$ approaches the power gain limit set by f_{max} for large-signal operation of an RF PA.

Mathematically, it can be shown that for the common-emitter stage, maximum gain matching occurs when both the input and output are conjugately matched, and thus

$$Z_{conj} \approx \frac{1 + j\omega(C'_{be} + C_{cb})Z'_{01}}{j\omega C_{cb}[1 + g'_m Z'_{01}] - \omega^2 C'_{be} C_{cb} Z'_{01}} \tag{1.15}$$

where $C'_{be} = C_{be}/(1 + g_m R_{ex})$, $g'_m = g_m/(1 + g_m R_{ex})$, and $Z'_{01} = (Z_0 + R_{bb})||R_\pi \approx R_\pi$ [35, 36]. Z_{out} is, therefore, influenced by C_{be} and C_{cb}, but not R_{bb}. When R_{bb} decreases, the locus of the G_p circuits stays constant, while the radii expand.

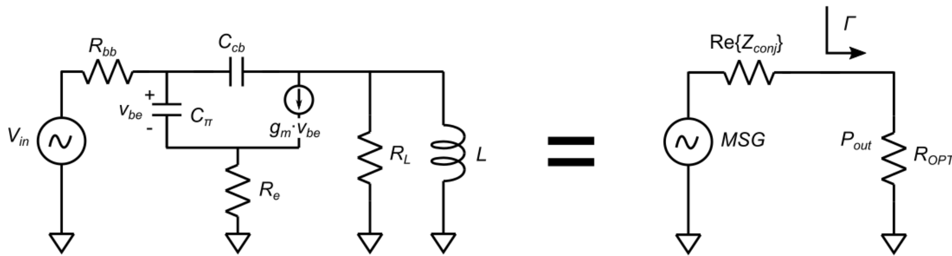


Figure 1.16: P_{out} modeled as a fraction of MSG due to the mismatch between Z_{OPT} and Re$\{Z_{conj}\}$

Interestingly, the degree of overlap/mismatch between Z_{OPT} and Z_{conj} is independent of power cell finger length when layout losses are ignored, and only first-order frequency-

dependent terms are discussed. Because $\mathrm{Re}\{Z_{conj}\}$ in the above equations are proportional to $1/L_e$, and $Z_{OPT} \approx V_{max}/I_{max} \propto 1/L_e$ as well. The mismatch between Z_{OPT} and Z_{conj} is determined by the transistor technology used. Thus, when the output of a power cell is modeled as a power source with a source impedance of $\mathrm{Re}\{Z_{conj}\}$ connected to a load impedance Z_{OPT} (Fig. 1.16), P_{out} is given by

$$P_{out} = MSG \cdot (1 - \Gamma^2) \text{ without unilateralization} \tag{1.16}$$

where MSG is the maximum stable gain, and Γ is the reflection coefficient between Z_{OPT} and $\mathrm{Re}\{Z_{conj}\}$. The two expressions are given by

$$MSG = \frac{|S_{21}|}{|S_{12}|} = \frac{|-2\,Z_0\,\frac{1}{j\omega C'_{be}}\,(g'_m\,\frac{1}{j\omega C_{cb}} - 1)|}{|2\,Z_0\,\frac{1}{j\omega C'_{be}}|} = \frac{g'_m}{\omega C_{cb}} - 1 \quad (K < 1) \tag{1.17}$$

$$\Gamma = \frac{Z_{OPT} - \mathrm{Re}\{Z_{conj}\}}{Z_{OPT} + \mathrm{Re}\{Z_{conj}\}} = L_e\text{-}independent \tag{1.18}$$

given that the numerator and denominator are both proportional to $1/L_e$. The degree of overlap between $\mathrm{Re}\{Z_{conj}\}$ and Z_{OPT} is, again, a technology-dependent parameter, *not* a circuit-level design variable at low frequency. Common Z_{OPT} between 12.5 - 100 Ω, Γ for various technologies and its mismatch with respect to $\mathrm{Re}\{Z_{conj}\}$ is virtually constant between DC - 100 GHz and calculated in Table 1.4.

	$\lvert\Gamma\rvert$ w.r.t. Z_{OPT} (DC - 100 GHz)			
	12.5 Ω	25 Ω	50 Ω	100 Ω
130 nm InP HBT	1.86e-4 - 1.92e-2	1.86e-4 - 1.92e-2	1.86e-4 - 1.92e-2	1.86e-4 - 1.92e-2
250 nm InP HBT	0.146 - 0.189	0.146 - 0.189	0.146 - 0.189	0.146 - 0.189
90 nm SiGe HBT	0.451 - 0.472	0.451 - 0.472	0.451 - 0.472	0.451 - 0.472
75nm GaN HEMT	0.509 - 0.591	0.509 - 0.591	0.509 - 0.591	0.509 - 0.591

Table 1.4: Mismatch between optimal power matching Z_{OPT} and maximum power gain Z_{conj} calculated for various technologies

To illustrate the applicability of Eq. 1.15 and the output-equivalent power source

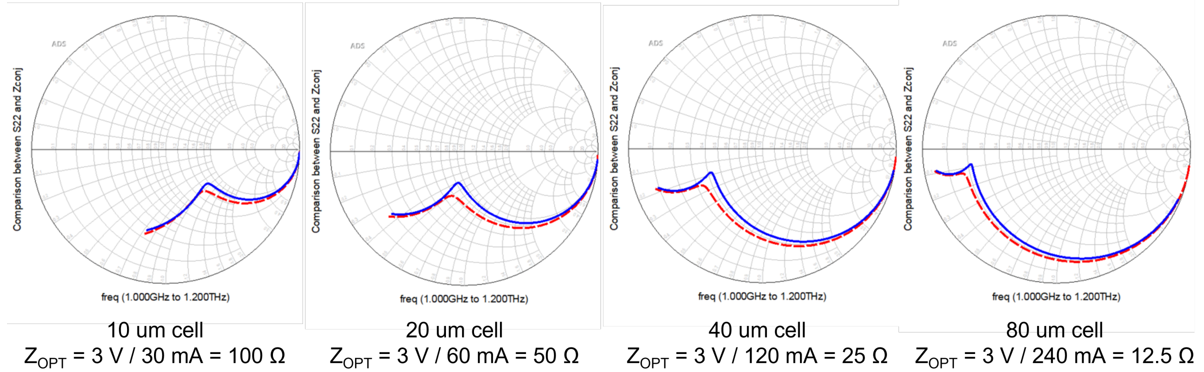


Figure 1.17: A comparison between power cell Z_{out} and Z_{conj} at different transistor sizings in 130 nm InP HBT where the blue curves are exact S_{22} of the hyrid-π model, and red dashed lines approximations per Eq. 1.15

formulism in Fig. 1.16, a comparison between Z_{out} and Z_{conj} is plotted in Fig. 1.17 for the 1 THz f_{max} 130 nm InP HBT at different finger lengths modeled with a hybrid-π model in the common-emitter configuration. A good agreement between the approximations following Eq. 1.15 and the exact S_{22} of the hybrid-π model is observed. Since Γ for the 1 THz f_{max} 130 nm InP HBT is approximately zero in Table 1.4, and MSG is 22 dB (Eq. 1.17) at 100 GHz, G_P at 4 different Z_{OPT} (12.5/25/50/100 Ω) for 4 transistor sizings should be $\sim$ 22 dB, which is the case shown in Fig. 1.18.

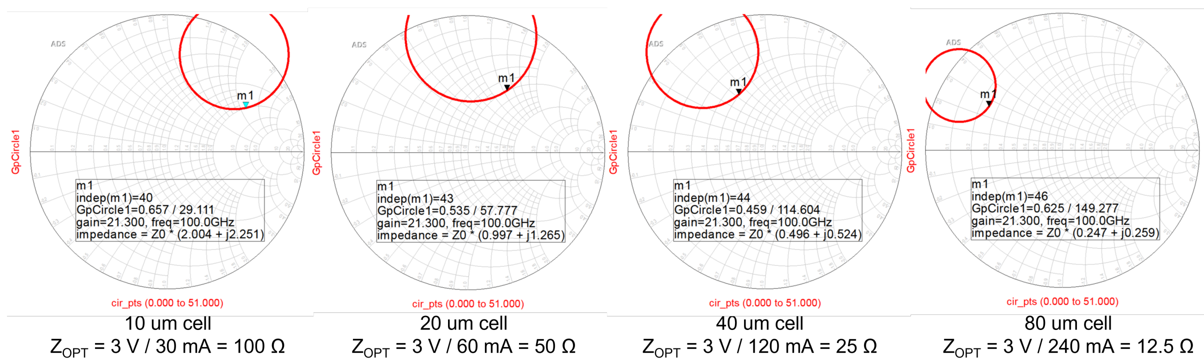


Figure 1.18: 21.3 dB operating gain G_P at 100 GHz with various transistor sizings and associated Z_{OPT} in 130 nm InP HBT

For technologies with $\Gamma \sim 0.5$, G_p under the optimal power matching condition

sees a -1.2 dB drop in power gain before all else losses are accounted for, which negates the gain capability suggested by f_{max} of these devices in RF PA. For the 240 GHz f_{max} 75 nm GaN HEMT, $MSG = 11.7$ dB matched to Z_{conj} is calculated, while a 10.5 dB large-signal gain matched to Z_{OPT} is expected, which is again the case in Fig. 1.19.

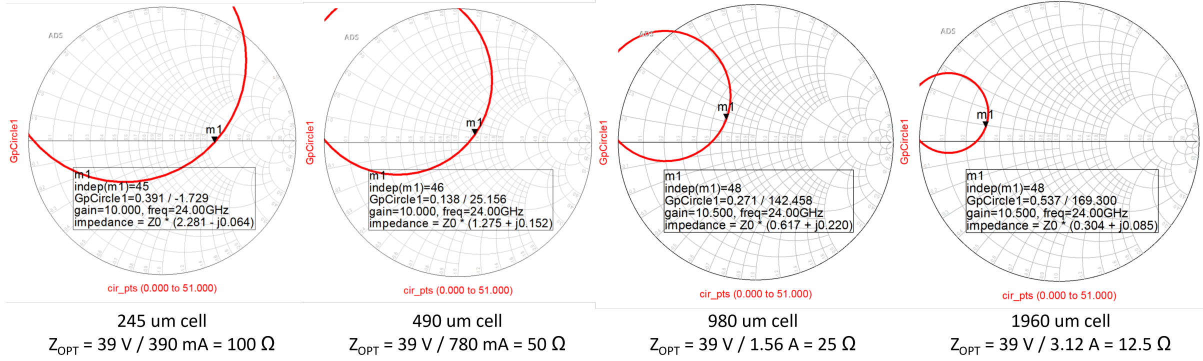


Figure 1.19: 10.5 dB operating gain G_P at 24 GHz with various transistor sizings and associated Z_{OPT} in 75 nm GaN HEMT

Here $f_{power,1}$ is defined as the frequency at which the operating gain G_P of a transistor is unity under the optimal power matching Z_{OPT}, or $P_{out}/P_{in} = MSG{\cdot}(1{-}\Gamma(f_{power,1})^2) = 1$. Because $MSG = MAG$ at frequencies close to f_{max} when $K > 1$, and Eq. 1.17 is modified by a pre-factor $(K - \sqrt{K^2 - 1})$, MSG is assumed to be approximately equal to U for simplicity. Therefore, we have

$$U \cdot [1 - \Gamma(f_{power,1})^2] \approx 1 \tag{1.19}$$

The calculated $f_{power,1}$ are listed in Table 1.5 for the 130 nm InP HBT, 250 nm InP HBT, 90 nm SiGe HBT, and 75 nm GaN HEMT.

	f_{max} (GHz)	$f_{power,1}$ (GHz) & Fraction of f_{max}	$f_{power,2}$ (GHz) & Fraction of f_{max}
130 nm InP HBT	1100	847 (77%)	930 (85%)
250 nm InP HBT	760	600 (79%)	655 (86%)
90 nm SiGe HBT	340	275 (81%)	277 (81%)
75nm GaN HEMT	240	156 (65%)	194 (81%)

Table 1.5: f_{max} of small-signal operation vs. $f_{power,1}$ and $f_{power,2}$ calculated for Z_{OPT} matching condition for various technologies

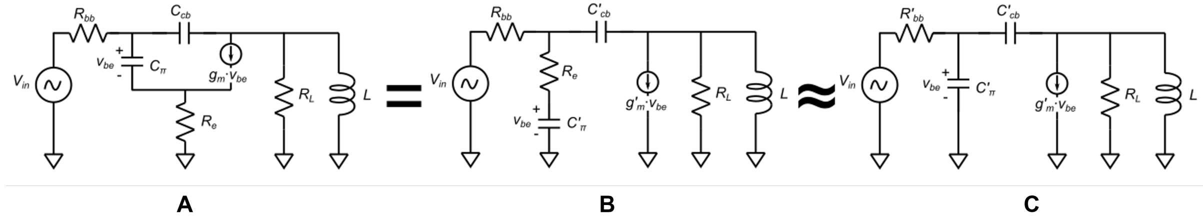


Figure 1.20: Hyprid-π models for alternative large-signal gain analysis

In addition to the output-focused formulism presented above, an alternative input-focused formulism[iv] that reconciles the small-signal gain matched to Z_{conj} and large-signal gain matched to Z_{OPT} is shown in Fig. 1.20, where C'_{cb}, C'_{π}, and g'_m are the same as above. In addition, $R'_{bb} \approx R_{bb} + R_e$. In Fig. 1.20, model A and B are identical. When $R_e = 0$, $g_m \cdot V_{be}$ is in phase with V_{be}, whereas the current through C_{cb} is $\pi/2$ out of phase. To ensure V_{out} is in phase with $g_m \cdot V_{be}$ (for a linear loadline), the current through C_{cb} must be equal to the current through L. When $R_e \neq 0$, the current through C_{cb} and L are not equal due to a phase shift in V_{be} introduced by R_e seen in Model B. However, R_e in Model B can be pulled out of the branch, and assigned to R'_{bb} as seen in Model C. Differences between the two devices (Model B & C) are negligible as shown in Fig. 1.21. Therefore, the input and power powers of a Model C device is given by

$$P_{in} = \omega^2 \, |V_{be}|^2 \, R'_{bb} \, [C'_{\pi} + C'_{cb}(1 + g'_m R_L)]^2 \tag{1.20}$$

$$P_{out} = |V_{be}|^2 \, {g'_m}^2 \, R_L \tag{1.21}$$

[iv] Courtesy of Professor Mark Rodwell

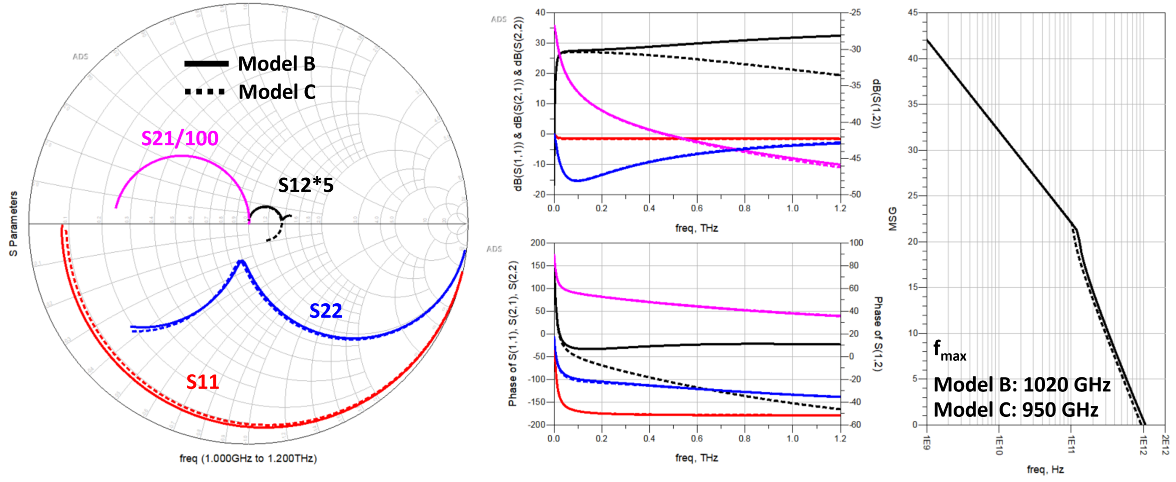


Figure 1.21: Comparison between a $0.13 \times 20\ \mu\text{m}^2$ 50 Ω InP HBT modeled by Model B & C in terms of S parameters in the Smith chart (left), dB and phase of S parameters (center), and transistor MSG (right)

For the optimal power matching Z_{OPT} loadline, $R_L = \frac{V_{max}-V_{min}}{I_{max}}$, and $P_{DC} = \frac{1}{4}(V_{max} + V_{min})\, I_{max}$, and thus PAE as a function of frequency is given by

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{1}{2}(\frac{V_{max} - V_{min}}{V_{max} - V_{min}})[1 - (\frac{f}{f_{power,2}})^2] \tag{1.22}$$

where $f_{power,2}$ is defined here as the frequency at which PAE is zero, and $G_P = \frac{P_{out}}{P_{in}} = 1$, or

$$f_{power,2} = \frac{1}{2\pi}\frac{g_m'}{C_\pi' + C_{cb}(1 + g_m' R_L)}\sqrt{\frac{R_L}{R_{bb}'}} \tag{1.23}$$

The calculated $f_{power,2}$ are listed in Table 1.5 for the 130 nm InP HBT, 250 nm InP HBT, 90 nm SiGe HBT, and 75 nm GaN HEMT.

Both $f_{power,1}$ and $f_{power,2}$ suggest RF PA is feasible up to ∼80% of f_{max} in various modern transistor technologies <u>*without the use of circuit-level neutralization techniques*</u>. A power gain higher than the transistor MSG is certainly realizable on a circuit level with

neutralization techniques. But in terms of device engineering, it is desirable to establish figures-of-merits such as $f_{power,1}$ and $f_{power,2}$ to better guide future device scaling for RF power amplifier applications. For example, one way to increase GaN HEMT's $f_{power,1}$ is to increase its current density to move its Z_{OPT} closer to Z_{conj}. This can be potentially achieved by incorporating high thermal conductivity cladding materials in the device structure [37, 38]. For InP HBT whose present proximity between Z_{OPT} and Z_{conj} is preserved following the conventional InP HBT scaling roadmap, non-idealities in process technologies and material limits obstruct such scaling beyond the 130 nm technology node (see Chapter 3).

1.6 Approaches to Off-Roadmap InP HBT Scaling

For millimeter-wave PA up to 300 GHz, Fig. 1.13 suggests further scaling of InP HBT leads to similar or lower P_{sat} and negligible improvement in power gain. Published PA results in 250 and 130 nm InP HBT processes within similar frequency bands confirm such observations [39, 40, 41, 42, 43]. Therefore, lithographic scaling of InP HBT to 60 nm technology node demands additional scrutiny. Two off-roadmap scaling alternatives are discussed in the following sections to boost InP HBT performance. They are the transferred-substrate InP HBT with low thermal conductivity substrate materials, and the regrown extrinsic base InP HBT.

1.7 Transferred-substrate Low Thermal Conductivity InP HBT

Power density of InP HBT is limited by heat dissipation like in other transistor technologies. Like other technologies, the inclusion of a high thermal conductivity heatsink

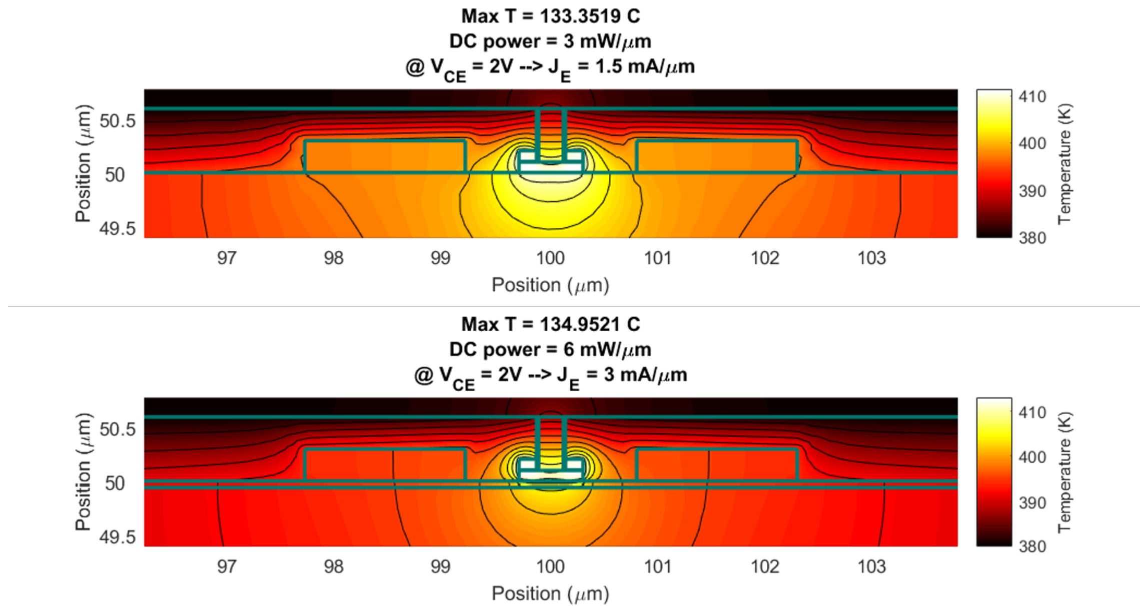


Figure 1.22: Temperature profile of conventional 250 nm InP HBT under typical bias conditions (top) vs. transferred-substrate InP HBT with Au subcollector 50 nm below device drift collector (bottom)

near the device active region could improve device performance [32, 34, 44, 45, 46, 47]. At a junction temperature of 150-200°C, InP HBT undergoes catastrophic destruction [48]. Therefore, at each scaling generation, maximum current density per emitter finger length is kept constant at 3 mA/μm. Fig. 1.22 (top) shows temperature profile of a 250 nm InP HBT biased at $\frac{1}{2}I_{max}$, and $\frac{1}{2}V_{max}$ for class-A operation. The substrate is 50 μm InP with gold back plating. Fig. 1.22 (bottom), on the other hand, shows a transferred-substrate 250 nm InP HBT with a gold subcollector 50 nm below its drift collector. The transferred-substrate HBT is biased at twice the current density for the same maximum junction temperature. In terms of potential PA performance, the twice current density yields a 2× increase in $f_{50\Omega}$, and doubles the device's ability to be power combined, offering roughly 3dB more P_{sat} at a given frequency. At 100 GHz, a PA in a transferred-substrate 250 nm InP HBT should be able to provide 32 dBm or 1.5 W P_{sat}. NTT, Teledyne, and Ferdinand-Braun-Institut are among the teams that work on this

technology [49, 50, 51]. Teledyne's published results demonstrates a multi-finger device that has a 9.4 W/mm power density and a 450 GHz f_{max} shown in Fig. 1.23 [51].

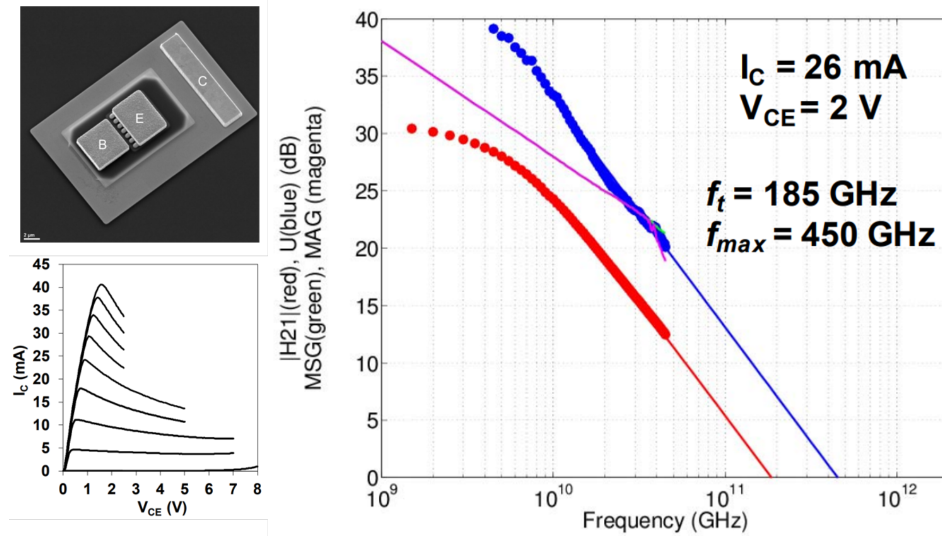


Figure 1.23: An 8-finger $0.25 \times 5\mu m^2$ transferred-substrate InP reported by Teledyne Scientific & Imaging [51]

Issues with the transferred-substrate technology include placement errors on the order of $\sim$1 μm, and scalability.

1.8 Regrown Extrinsic Base InP HBT

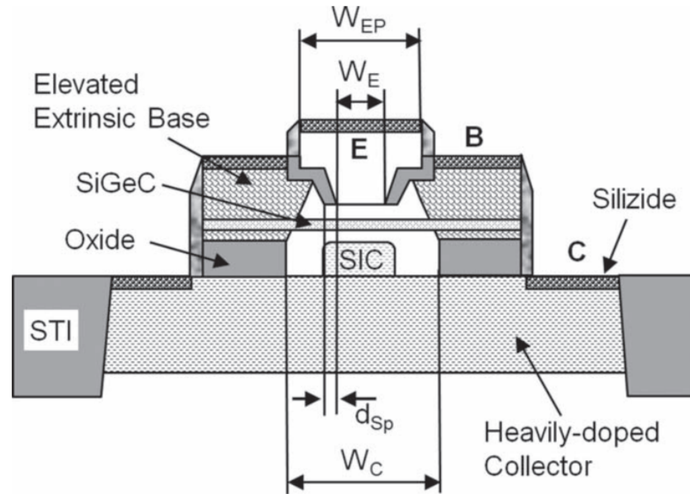


Figure 1.24: Schematic cross-section of a SiGe HBT with the elevated extrinsic base [52]; Reprint under the Creative Commons Attribution 3.0 license

The regrown extrinsic base process module is ubiquitous in modern SiGe HBT as shown in Fig. 1.24 [52]. The process module enables the use of a low sheet resistance ρ_s extrinsic semiconductor region, usually in heavily-doped poly-Si, as well as a deep metal silicide low contact resistivity ρ_c base contact for low base access resistance. Given the extrinsic base is deposited on top of a local oxide (LOCO) that minimizes capacitive coupling between the base and collector terminals, width of the extrinsic base region can be made $\gg 3 \times L_T$, where the transfer length is $L_T = \sqrt{\frac{\rho_c}{\rho_s}}$, for low base contact resistance $R_{b,cont} = \frac{\sqrt{\rho_c \rho_s}}{2L_e}$. Intuitively, f_{max} scales as $R_{bb}{}^{-0.5}$. So for a base contact resistance limited HBT, scaling R_{bb} leads to higher power gain at a given frequency *without* sacrificing maximum voltage or current swing.

Early attempts found in the literature at incorporating a regrown extrinsic base module in the InP HBT process flow were demonstrated at the 1.6 μm emitter width technology node shown in Fig. 1.25 [53]. The process required a SiN_x dummy emitter for the definition of the extrinsic base regrowth window, and subsequent realignment/deposition

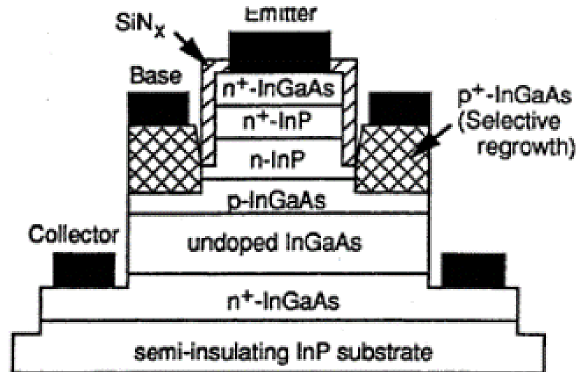


Figure 1.25: Regrown extrinsic base InP HBT with a realigned emitter contact reported in 1996 [53]

of the emitter metal contact. Compared to the baseline device, a 1.8× reduction in R_{bb} was reported. However, several issues were recognized, including difficulties of scaling due to realignment of the emitter contact, and redistribution of the p-type Zn dopants after regrowth. Thus, future regrown extrinsic base InP HBT should employ a self-aligned emitter metal contact, and a less diffusive p-type dopant (e.g. carbon) for both smaller lateral feature sizes and thinner intrinsic epitaxial structures.

1.9 Conclusions

This chapter details the current technology landscape of radio-frequency power amplifiers at millimeter-wave frequencies (30 - 300 GHz) in competing technologies. The limited applicability of f_T/f_{max}, and $JFOM$ at predicting reasonable PA performance is explained. A new pair of variables, $P_{sat-50\Omega}$ and $f_{50\Omega}$, are introduced to address the issue. P_{sat} of theoretically realizable PA in the various transistor technologies as a function of frequency is derived. 250 nm InP HBT is shown to be an adequate technology for PA at above 100 GHz, with 75 nm GaN HEMT a close second. With future scaling, GaN HEMT is expected to offer more power at above 100 GHz when more current per μm

is available to overcome its current $1/f^4$ electromagnetic limit. Finally, further scaling of InP HBT proves to be problematic as the 250 nm technology node is already beyond its electromagnetic limitations, and both P_{sat} and power gain are now hindered by loadline matching. Two off-roadmap scaling alternatives are discussed: transferred substrate InP HBT, and regrown extrinsic base InP HBT. Both offer slight improvement in device f_{max}, but more importantly aim to tackle the loadline problem without sacrificing power density.

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Chapter 2

Design of Intrinsic InP HBT

This chapter reviews the operating principles of conventional InP mesa HBTs, derivation and conventional scaling law of important device parameters, and current technological challenges that serve as the basis for regrown extrinsic base InP HBT detailed in chapter 3.

2.1 Principle of Operation

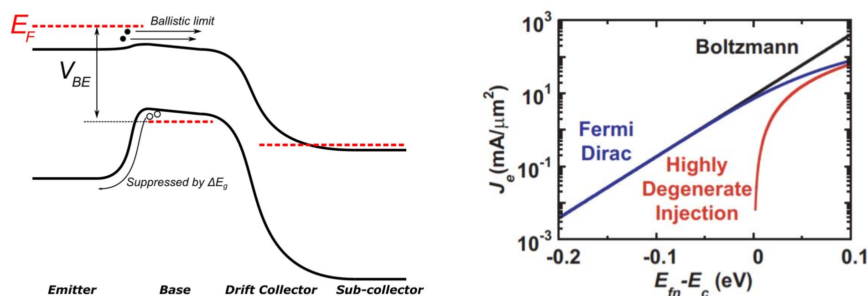

Figure 2.1: Band alignment of a graded heterojunction InP HBT with doping-graded base (left); Early onset of γ degradation in an *abrupt* InP/InGaAs emitter-base junction (right) [1]

InP HBT, like its mature GaAs counterpart pioneered by Kromer and Woodall [2, 3]

in the 1970s, owns its high-frequency performance to first the use of a wide-gap InP emitter [4], which blocks hole diffusion current across the emitter-base junction (Fig. 2.1). Base semiconductor InGaAs, therefore, can be made thin, and doped much higher than the emitter semiconductor, while maintaining a high emitter injection efficiency γ. Base current is dominated by Auger recombination in the base region, rather than the hole diffusion current at the emitter-base junction.

For a low to moderate applied V_{be}, the diffusion current densities are limited by the Boltzmann tail of the Fermi distribution, and thus

$$\frac{J_{n,low\,V_{be}}}{J_{p,low\,V_{be}}} = \frac{N_e}{P_b} \cdot \frac{\upsilon_{n,b}}{\upsilon_{p,e}} \cdot \exp(\Delta E_g/k_B T) \tag{2.1}$$

where $\exp(\Delta E_g/k_B T) \cong 1 \times 10^{11}$ for $\Delta E_g = 0.7\text{eV}$ in the case of a graded InGaAs/InP heterojunction. Thus, $\gamma_{low,\,V_{be}} \cong 1$.

Under the high-level injection condition where emitter Fermi level is above $E_{c,b}$, rather than the Fermi distribution, electron injection is limited by the diminishing density of states in the base conduction band. Considering only a single 3D Γ-valley, we have

$$\begin{aligned} J_{n,\,high\,V_{be}} &= \frac{8\sqrt{2}\pi}{h^3} m^{*3/2} \int_{E_{c,b}}^{\infty} \frac{g_i}{\exp((E-E_{F,e})/k_B T)-1} \cdot (E-E_{c,b})\,\mathrm{d}E \\ &= C_0 \int_{E_{c,b}}^{\infty} \frac{1}{\exp[(E-E_{c,b}-(qV_{be}-E_{g,b}))/k_B T]-1} \cdot (E-E_{c,b})\,\mathrm{d}E \end{aligned}$$

where $(qV_{be} - E_{g,b})$ in modern HBT is in excess of 0.3eV, and thus the Fermi function could be approximated by a unit step-function with a discontinuity at the quasi-Fermi level

$$J_{n,\,high\,V_{be}} \cong C_0 \int_{E_{c,b}}^{E_{F,e}} (E-E_{c,b})\,\mathrm{d}E \cong {C_0}^{*} \cdot V_{be}^2 \tag{2.2}$$

J_n approaches the Landauer ballistic limit under strong forward bias, and deviates from

exponential behavior as shown in Fig. 2.1 (right) [5]. Yet, despite J_n degradation under high V_{be}, γ in InP HBT remains close to unity with the help of the bandgap difference between InP and InGaAs according to Eq. 2.1.

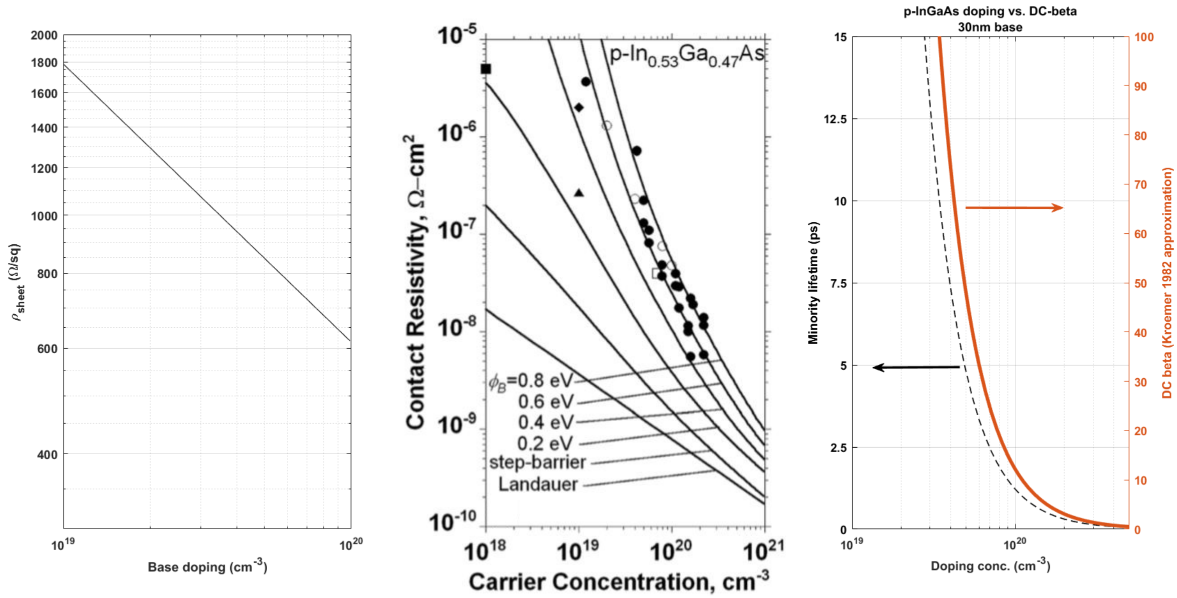

Figure 2.2: $\rho_{c,b}$ to base (left), ρ_{sh} of 30nm thick p-InGaAs (center) [6], and β_F vs. doping conc. (right); Reprint with Permission © AIP 2013[i]

The base region can, therefore, be doped much higher than the emitter region for a low base sheet resistance $\rho_{sh,b}$ and low contact resistivity $\rho_{c,b}$, and much thinner for low base transit time τ_b. Figure 2.2 (left & center) shows experimental and fitted $\rho_{sh,b}$, and $\rho_{c,b}$ of a 30nm thick p-InGaAs:C layer [6, 7]. In a 250 nm technology node InP HBT, the average dopant concentration in the base is 7e19 cm^{-3} for an Auger-limited minority carrier life-time τ_{Auger} of 2.5 ps [8, 9]. Given base current density J_b in an InP HBT is dominated by Auger recombination, device DC current gain can be approximated by the

[i]Reproduced from "A. Baraskar, A. Gossard, and M. J. Rodwell, *Lower limits to metal-semiconductor contact resistance: Theoretical models and experimental data*, Journal of Applied Physics, vol. 114, no. 15, p. 154516, 2013.", with the permission of AIP Publishing.

ratio between τ_{Auger} and τ_b [2]

$$J_b = J_{p,r} = N_e T_b / \tau_{Auger}$$
$$\beta = J_c / J_b \cong \frac{v_{n,b}\,\tau_{Auger}}{T_b} = \frac{\tau_{Auger}}{\tau_b} \quad (2.3)$$

Assuming an electron injection velocity $v_{n,b} = \sqrt{\frac{2\Delta E_c}{m^*}}$ from the abrupt emitter-base junction, a calculated $\beta = 25$ is in good agreement with experimental results [10].

Doping gradient is introduced to produce a quasi-electric field to further accelerate electrons across the base region [11, 12, 13]. A $9 - 5 \times 10^{19} cm^{-3}$ doping grade in the InGaAs base produces an appreciable quasi-electric field ΔE_c of $\sim$ 60meV (Figure 2.1) using the Joyce-Dixon approximation given by [14]

$$\Delta E_c / k_B T \cong \ln \frac{p_{b,e}}{p_{b,c}} + \frac{1}{\sqrt{8}} \frac{p_{b,e} - p_{b,c}}{N_v} + \left(\frac{\sqrt{3}}{9} - \frac{3}{16}\right) \frac{{p_{b,e}}^2 - {p_{b,c}}^2}{{N_v}^2} \quad (2.4)$$

In more mature technologies (e.g. GaAs, SiGe HBTs), compositional grading is preferred over doping grading for achieving a better defined quasi-field in the base [15, 16, 17]. τ_b in the presence of ΔE_c is given as a slight modification to the classic Moll-Ross relation [18]

$$\tau_b = \frac{{T_b}^2}{D_{n,b}} \frac{k_B T}{\Delta E_c} \left[1 - \frac{k_B T}{\Delta E_c}\left(1 - e^{-\Delta E_c / k_B T}\right)\right] + \frac{T_b}{v_{exit}} \frac{k_B T}{\Delta E_c}\left(1 - e^{-\Delta E_c / k_B T}\right) \quad (2.5)$$

where the finite v_{exit} for electrons entering the drift collector relates to the Kirk effect discussed below.

The lightly doped n-type InP drift collector is able to handle large voltage swings similar to the PIN diode. A good rule of thumb to avoid avalanche breakdown in the base-collector junction is 35V/um-InP-drift-collector [20, 21]. Doping in the drift collector is determined by the Kirk current density J_{Kirk}, at which the point charge density of electrons injected from the base exceeds the concentration of the fixed ionized acceptors

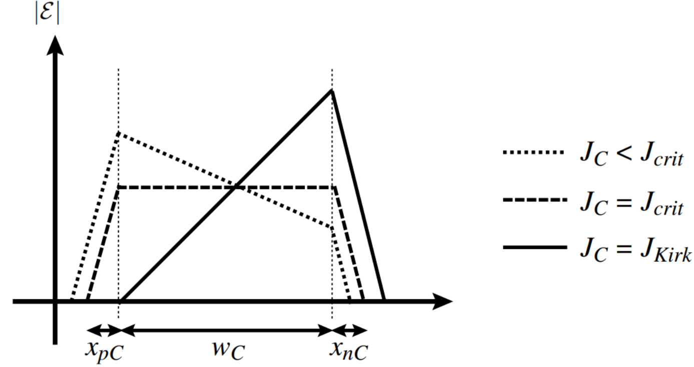

Figure 2.3: Electric field profils in the collector when $J_c < J_{crit}$, $J_c = J_{crit}$, and $J_c < J_{Kirk}$ [19]; Reprinted with permission © Springer 2008

in the drift collector. As a result, the conduction band profile becomes flat at the base side of the drift collector, giving the effect its alternative name *base pushout.* τ_b increases dramatically beyond J_{Kirk} as electric field collapses as seen in Fig. 2.3 [19]. For a given J_{Kirk}, collector doping concentration N_c is given by

$$J_{Kirk} = [\frac{2\epsilon_0\epsilon_r}{T_c^2}(\phi_{bi} + V_{cb}) + qN_c] \cdot v_{eff} \tag{2.6}$$

where v_{eff} is the effective electron velocity across the drift collector due to *velocity overshoot* in InP.

Due to the large ~ 0.6eV Γ-L separation, electrons injected in the InP drift collector can travel in the Γ-valley faster than the drift-diffusion limit before gaining enough energy to scatter into lower velocity L-valleys. Fig. 2.4 shows comparison between results of Monte Carlo simulations (left), and empirical $\frac{1}{2}m^*v^2$ approximations (right) [22, 23]. Both suggest a peak velocity above 1e8 cm/s, and a drift-diffusion velocity of 2e7 cm/s. In earlier literature, the velocity overshoot phenomenon is usually fitted by a step-like 2-section velocity profile as a function of distance x [24]. v_{eff} in Eq. 2.6 is simply the time-weighted average of $v(x)$. The width of the high velocity region is on the

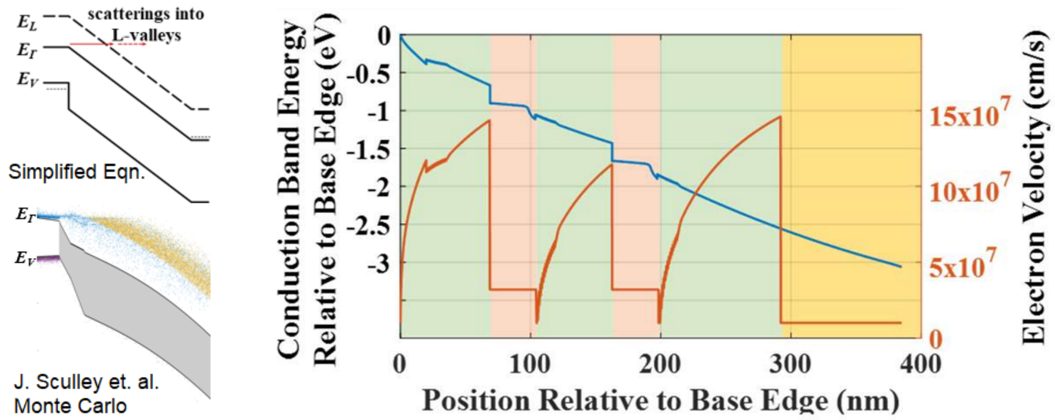

Figure 2.4: Monte Carlo results (left) show comparable extent of velocity overshoot vs. empirical calculations (right) [22]

order of 60-80 nm, followed by a low velocity region that spans the rest of the drift collector. Drift collector dopant concentration N_c is, thus, constant. Recently, it has been confirmed by Monte Carlo simulations that a dopant gradient should be employed instead, as electron slowdown towards the end of the drift collector leads to band flattening, which in turn further slows down electrons in a positive feedback leading to Gunn oscillation and negative output impedance [25]. The current engineering solution to Gunn oscillation and output impedance instability is to simply dope the entire drift collector beyond what the Kirk effect demands. The tradeoff, in this case, is a decrease in transistor breakdown voltages.

In the charge control model, where time constant is defined as the ratio between ΔQ and I, the amount of charge imagined at the base terminal by transient electrons in the drift collector is given by

$$\Delta Q_{b,c} = Q_c(x) \times (1 - \frac{x}{T_c}) \tag{2.7}$$

Thus, collector transit time τ_c is given by

$$\tau_c = \int_0^{T_c} \frac{1}{v(x)} (1 - \frac{x}{T_c}) \, \mathrm{d}x \tag{2.8}$$

Or empirically,

$$\tau_c = \frac{T_c}{2v_{eff}} \tag{2.9}$$

where v_eff is the effective average electron velocity including velocity overshoot and the Kirk effect discussed above. Such definition of τ_c is a source of perpetual confusion, and is often instead referred to as the *collector signal delay time* to emphasize its relation to an input RF signal instead of the amount of time an electron takes to traverse the drift collector [26].

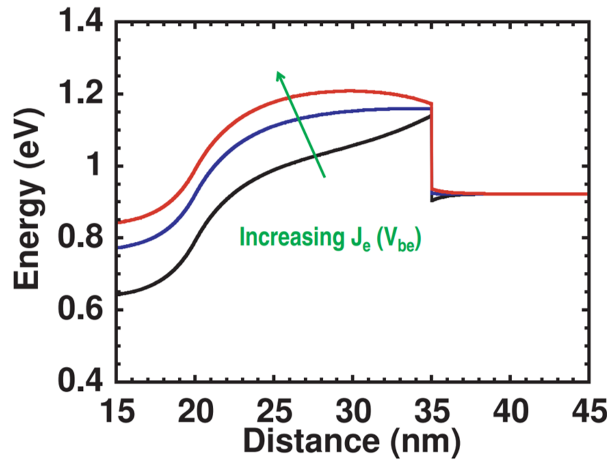

Figure 2.5: Emitter starvation under high current injection [1]

In an effect similar to the Kirk effect in the drift collector, the emitter-base junction can experience a charge accumulation effect that degrades g_m rapidly, termed *emitter starvation* (Fig. 2.5) [1]. Therefore, emitter is heavily doped as well in modern InP HBT [27, 28].

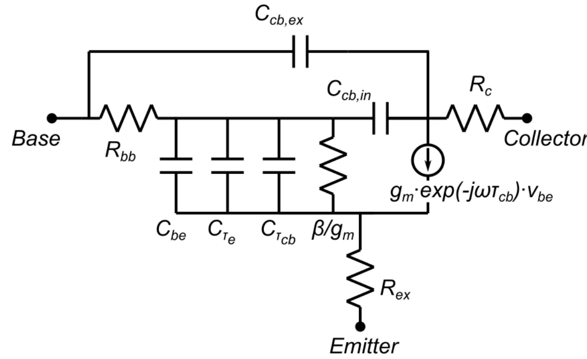

Figure 2.6: correspondence between physical elements and small signal model circuit components

Finally, junction capacitances and sheet and contact resistances are present throughout an actual device structure. The correspondence between physical elements and small signal model circuit components are shown in Fig. 2.6, where C_{be}, $C_{cb,in}$ and $C_{cb,ex}$ are the junction capacitances, C_{τ_e}, and $C_{\tau_c b}$ are diffusion capacitances due to finite electron velocity, and R_{bb}, R_c, and R_{ex} the various sheet and contact resistances.

2.2 Conventional InP HBT Scaling Roadmap

In this section, mapping between the physical model developed in section 2.1 and actual device layouts is discuss, together with the conventional InP HBT scaling roadmap introduced.

Fig. 2.7 (left) shows the cross-sectional schematic of a conventional InP mesa HBT defined by its emitter contact width W_{ec}, emitter junction width W_e, base-emitter contact gap distance $W_{b,gap}$, single-sided base metal contact width W_{bc}, base-collector mesa width $W_{b,mesa}$, base-collector mesa undercut distancec $W_{b,undercut}$, single-sided base-collector metal gap distance $W_{c,gap}$, and collector metal contact width W_{cc}. Length of emitter strip L_e is seen in Fig. 2.7 (right), with extrinsic features such as base metal post, and collector metal post for wiring purposes. It is worth mentioning area of the base metal

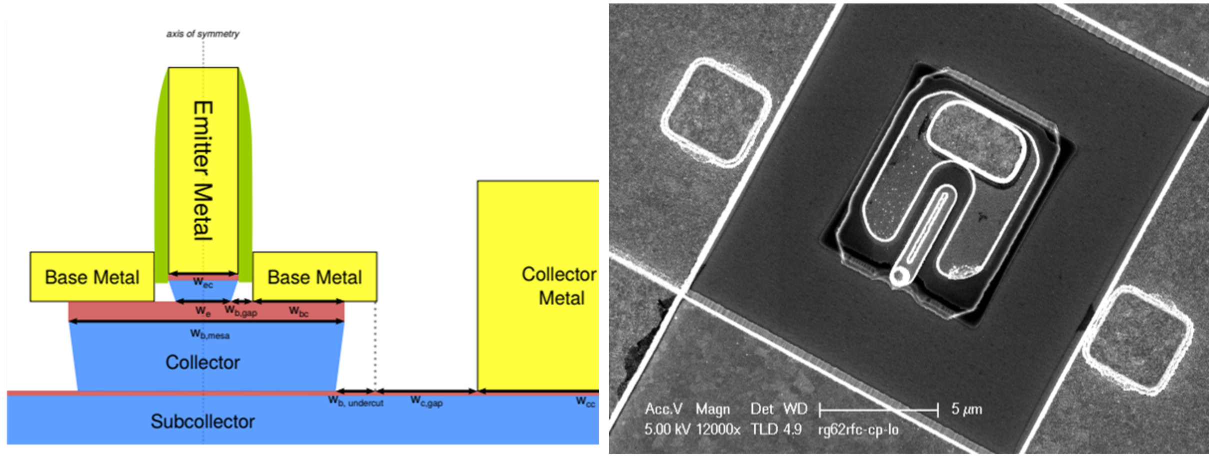

Figure 2.7: Cross-sectional schematic of a conventional InP mesa HBT with critical dimensions indicated (left), and a top-down view of an InP HBT embedded in TRL wiring environment prior to BCB planarization (right)

post $A_{b,post}$ contributes to extrinsic C_{cb}. Together with emitter semiconductor thickness T_e, base semiconductor thickness T_b, and drift collector semiconductor thickness T_c, straightforward correspondence to small-signal equivalent circuit components normalized to per L_e are given as the following[ii]

$$R_{ex} = \underbrace{\frac{\rho_{ec}}{W_{ec}}}_{\text{T.D.}} + \frac{\rho_{e,bulk}}{W_{ec}} \tag{2.10}$$

$$C_{be} = \frac{\varepsilon_{InP} W_e}{T_{j,be}} \tag{2.11}$$

$$C_{\tau_b} = g_m [\underbrace{\frac{T_b}{v_{n,b}}}_{\text{T.D.}} + \frac{{T_b}^2}{2D_{n,b}}] \tag{2.12}$$

$$C_{\tau_{cb}} = g_m \frac{T_c}{2v_{eff}} \tag{2.13}$$

$$C_{diff} = C_{\tau_b} + \underbrace{C_{\tau_{cb}}}_{\text{T.D.}} \tag{2.14}$$

[ii]T.D.: Traditionally dominant

$$C_\pi = \underbrace{C_{be}}_{\text{T.D.}} + C_{diff} \tag{2.15}$$

$$R_\pi = \frac{\beta}{g_m} \tag{2.16}$$

$$R_{bb} = \rho_{bs}\frac{W_e}{12} + \rho_{bs}\frac{W_{b,gap}}{2} + \underbrace{\frac{\sqrt{\rho_{bc}\rho_{bs}}}{2}\coth(\frac{W_{bc}}{L_{T,b}})}_{\text{T.D.} \approx \frac{\rho_{bc}}{2W_{bc}} + \rho_{bs}\frac{W_{bc}}{6}} \tag{2.17}$$

$$g_m = \frac{q\,J_c}{\eta k_B T} \tag{2.18}$$

$$C_{cb,in} = \frac{\varepsilon_{InP} W_{cb,in}}{T_{j,cb}} \approx \frac{2\varepsilon_{InP} W_e}{T_{j,cb}} \tag{2.19}$$

$$C_{cb,ex} = \frac{\varepsilon_{InP} W_{cb,ex}}{T_{j,cb}} \approx \frac{\varepsilon_{InP}[W_{b,mesa} - 2W_e]}{T_{j,cb}} + \frac{\varepsilon_{InP} A_{b,post}}{L_e\,T_{j,cb}} \tag{2.20}$$

$$C_{cb,tot} = C_{cb,in} + \underbrace{C_{cb,ex}}_{\text{T.D.}} \tag{2.21}$$

$$R_c = \rho_{cs}\frac{W_{b,mesa}}{12} + \underbrace{\rho_{bs}\frac{W_{c,gap}}{2}}_{\text{T.D.}} + \frac{\sqrt{\rho_{cc}\rho_{cs}}}{2}\coth(\frac{W_{cc}}{L_{T,c}}) \tag{2.22}$$

$$\begin{aligned}\tau_{ec} &= \tau_{eb} + \tau_b + \tau_{bc} + \tau_c \\ &= \underbrace{\frac{C_{be}}{g_m}}_{\text{T.D.}} + [\frac{T_b}{v_{n,b}} + \frac{{T_b}^2}{2D_{n,b}}] \\ &\qquad + \frac{T_c}{2v_{eff}} + [\frac{1}{g_m} + R_{ex} + R_c]C_{cb,in}\end{aligned} \tag{2.23}$$

Conventional figures of merit f_T/f_{max} derived in section 1.2, thus, need to be slightly modified to take into account the effects of the various RC delay times, and

$$\frac{1}{2\pi f_T} = \tau_{ec} \tag{2.24}$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{cb,in} R_{bb}}} \tag{2.25}$$

Parameter	250 nm node	130 nm node	65 nm node	30 nm node	Scaling
Emitter Width W_e (nm)	250	130	65	30	$1/\gamma^2$
Emitter-base Capacitance C_{be} (fF/μm-L_e)	30	21	15	11	$1/\gamma$
Emitter Contact Resistivity ρ_{ec} (Ω-μm^2)	8	4	2	1	$1/\gamma^2$
Emitter Access Resistance R_{ex} (Ω-μm-L_e)	32				1
Emitter Current Density J_e (mA/μm^2)	9	18	36	72	γ^2
Transconductance g_m (mS/μm-L_e)	100				1
Base Contact Width W_{bc} (nm)	175	120	60	30	$1/\gamma^2$
Base Contact Overlay Accuracy (nm)	30	20	10	5	$1/\gamma^2$
Base Thickness T_b (nm)	250	212	180	150	$1/\gamma^{0.5}$
Base Contact Resistivity ρ_{bc} (Ω-μm^2)	10	5	2	1	$1/\gamma^2$
Base Access Resistance R_{bb} (Ω-μm-L_e)	~ 60				1
Drift Collector Thickness T_c (nm)	100	75	50	40	$1/\gamma$
Open-base Collector-emitter Breakdown Voltage BV_{CEO} (V)	4.9	4.0	3.3	2.8	$1/\gamma^{\sim 0.5}$
Base-collector Capacitance $C_{cb,tot}$ (fF/μm-L_e)	0.65	0.46	0.32	0.23	$1/\gamma$
f_T (GHz)	520	730	1000	1400	γ
f_{max} (GHz)	850	1300	2000	2800	γ

Table 2.1: Conventional InP HBT scaling roadmap with issues discussed in text

As a result, the requirements set forth by the conventional InP HBT scaling roadmap are tabulated in Table 2.1 [29]. Previous technology development has demonstrated both n- and p-type contact resistivities less than 5 Ω-μm^2 for the 130 nm node requirements with MBE in-situ and ex-situ Mo/W refractory contact evaporation [30, 31]. Ruthenium-based dry-etched contact to p-InGaAs has exhibited close to 2 Ω-μm^2 contact resistivity in standalone TLM structures, but shows a 4 Ω-μm^2 contact resistivity in the full HBT process flow [32]. It has been recognized that strong surface pinning leads to depletion

of charge carriers at the surface of the base semiconductor, leading to high contact resistivity. Therefore, $> 1\times10^{20}$ cm^{-3} carbon pulse-doping is utilized to combat such effect [33, 34]. According to theoretical calculations, however, lower than 4 Ω-μm^2 contact resistivities to n- and p-InGaAs are hard to realize, casting doubts on future scaling of InP HBT [35].

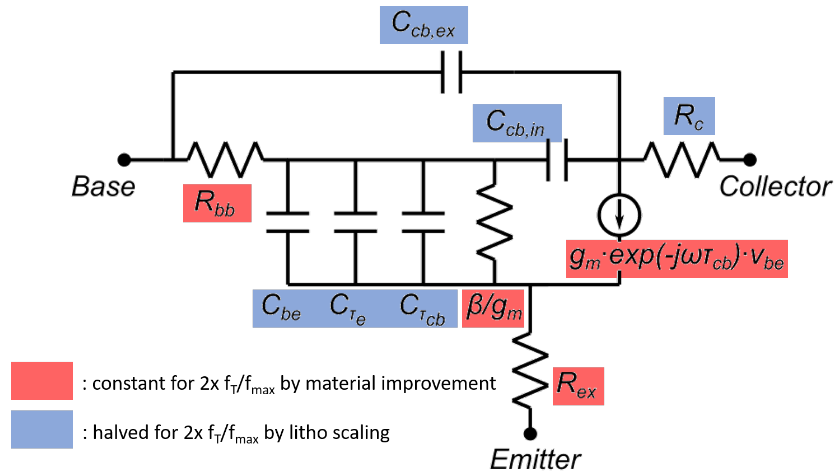

Figure 2.8: Improvement in small-signal parameters categorized into lithographic feature size driven (blue) and materials science driven (red)

The issues with the conventional requirements are obvious, and can be more easily visualized in the small-signal model in Fig. 2.8. Apart from the quadratic increase in overlay accuracy capability that most III-V foundries lack, progress in device f_T/f_{max} is realized by continued progress in materials science in terms of contact resistivities, and realizable doping concentrations. The current $> 1\times10^{20}$ cm^{-3} carbon dopant concentration approaches highest reported p-type dopant concentration in InGaAs [36]. In addition, g_m non-scaling due to the conduction band density of states limit and other quantum effects [37], $> 5\times$ increase in tungsten bulk resistivity at below 100 nm grain size [38], accelerated degradation of device performance under high current densities [39], high emitter-base gap resistance due to a minimum emitter dielectric sidewall thickness

[33], high self-inductance in the shrinking base metal contact [40], higher contribution of extrinsic parasitics (e.g. base post landing area) [41], and mechanical failure of high aspect-ratio emitter metal/semiconductor structures during stress release at the back-end stage all compound the difficulty to beyond the 130 nm scaling. Therefore, an architectural redesign of the conventional InP mesa HBT is needed to extend the technology beyond the 130 nm technology node.

2.3 Intrinsic Epitaxial Design for 130 nm InP HBT

The intrinsic epitaxial device structures used in this work are grown by solid source molecular beam epitaxy on 4" semi-insulating Fe-doped InP substrates by commercial epi vendors IQE and IntelliEpi. Two designs utilizing an InGaAs base, DHBT62, DHBT64 and DHBT67, are ordered from IQE, while a GaAsSb base design is ordered from IntelliEpi. Substrates are from Sumitomo Electric with a slight 0.15° miscut towards [110].

Thickness (nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	8×10^{19} : Si	Emitter Contact Cap
15	InP	5×10^{19} : Si	Emitter
15	InP	5×10^{18} : Si	Emitter
2.5	$In_{\approx 0.5}Ga_{\approx 0.5}As$	11×10^{19} : C	Base Contact
20	$In_{\approx 0.5}Ga_{\approx 0.5}As$	11-7 $\times 10^{19}$: C	Base
13.5	$In_{0.53}Ga_{0.47}As$	5×10^{16} : Si	Setback
16.5	InGaAs/InAlAs	5×10^{16} : Si	Chirped B-C Grade
3	InP	3.6×10^{18} : Si	Pulse Doping
67	InP	5×10^{16} : Si	Drift Collector
7.5	InP	2×10^{19} : Si	Sub-collector
7.5	$In_{0.53}Ga_{0.47}As$	4×10^{19} : Si	Sub-collector
300	InP	1×10^{19} : Si	Sub-collector
3.5	$In_{0.53}Ga_{0.47}As$	UID	Etch Stop
10	InP	UID	Growth Initiation
$\approx$ 630k	SI-InP	Fe	Substrate

Table 2.2: Design of DHBT64 with a base contact layer compared to old HBT64

DHBT64 design is based on the old HBT64 design from previous generation of Rodwell students. It features a thin 15 nm n-InP:Si emitter space charge region doped at 5×10^{18} cm^{-3} to reduce emitter starvation effects. The base region consists of a thin 2.5 nm high doping top contact layer, and a 20 nm thick intrinsic base doping graded from 11×10^{19} cm^{-3} at the emitter side to 7×10^{19} cm^{-3} at the collector side for a 90 meV quasi-electric field in the base conduction band.

Thickness (nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	8×10^{19} : Si	Emitter Contact Cap
15	InP	5×10^{19} : Si	Emitter
15	InP	5×10^{18} : Si	Emitter
30	$In_{\approx 0.5}Ga_{\approx 0.5}As$	9-5 $\times 10^{19}$: C	Base
13.5	$In_{0.53}Ga_{0.47}As$	5×10^{16} : Si	Setback
16.5	InGaAs/InAlAs	5×10^{16} : Si	Chirped B-C Grade
3	InP	3.6×10^{18} : Si	Pulse Doping
67	InP	5×10^{16} : Si	Drift Collector
7.5	InP	2×10^{19} : Si	Sub-collector
7.5	$In_{0.53}Ga_{0.47}As$	4×10^{19} : Si	Sub-collector
300	InP	1×10^{19} : Si	Sub-collector
3.5	$In_{0.53}Ga_{0.47}As$	UID	Etch Stop
10	InP	UID	Growth Initiation
$\approx$ 630k	SI-InP	Fe	Substrate

Table 2.3: Design of DHBT67 with a 30 nm thick p-InGaAs base

DHBT67 design is similar to DHBT64, with the same thin 15 nm n-InP:Si emitter space charge region doped at 5×10^{18} cm^{-3} to reduce emitter starvation effects. However, for the intrinsic base, DHBT67 takes a more conservative approach, and does *not* include a thin 2.5 nm high doping top contact layer. Instead, a 30 nm thick intrinsic base doping graded from 9×10^{19} cm^{-3} at the emitter side to 5×10^{19} cm^{-3} at the collector side for a 60 meV quasi-electric field in the base conduction band. The rest of the epitaxial design is, otherwise, same as DHBT64.

DHBT62 design is outdated, and resembles DHBT64. The two differences are 1). a lower emitter space charge region dopant concentration at 3×10^{19} cm^{-3}, and 2). a thinner 16nm thick doping graded intrinsic base. The lower emitter space charge region dopant concentration leads to stronger emitter starvation, while the thinner base layer provides a higher base sheet resistance. Both features are not conducive to high RF performance.

Thickness (nm)	Material	Doping (cm^{-3})	Description
10	$In_{0.53}Ga_{0.47}As$	8×10^{19} : Si	Emitter Contact Cap
15	InP	5×10^{19} : Si	Emitter
10	InP	5×10^{18} : Si	Emitter
5	$In_{1-0.85}Ga_{0-0.15}P$	5×10^{18} : Si	Emitter
2.5	$GaAs_{0.58}Sb_{0.42}$	15×10^{19} : C	Base Contact
17.5	$GaAs_{0.58-0.45}Sb_{0.42-0.55}$	15-8 $\times 10^{19}$: C	Base
100	InP	7×10^{16} : Si	Drift Collector
7.5	InP	2×10^{19} : Si	Sub-collector
7.5	$In_{0.53}Ga_{0.47}As$	4×10^{19} : Si	Sub-collector
300	InP	1×10^{19} : Si	Sub-collector
3.5	$In_{0.53}Ga_{0.47}As$	UID	Etch Stop
10	InP	UID	Growth Initiation
$\approx$ 630k	SI-InP	Fe	Substrate

Table 2.4: Design of DHBT90-Sb with a 20 nm thick p-GaAsSb base

DHBT90-Sb design is similar to DHBT64, with a thinner 15 nm n-InP:Si emitter space charge region doped at 5×10^{18} cm^{-3} to reduce emitter starvation effects. Slight GaP-alloying in the emitter for the 5 nm close to the base layer is introduced to ensure a type-I band alignment that again minimizes emitter starvation effects. Instead of a p-InGaAs base the group has been using since the first generation of InP HBT research, a p-GaAsSb base is employed for higher realizable p-type carbon dopant concentration. The higher p-type carbon dopant concentration does *not* produce a lower intrinsic base sheet resistance ρ_{bs} as p-GaAsSb has a roughly 2$\times$ bulk resistivity compared to p-InGaAs at a given dopant concentration. Such dopant concentration is needed to maintain a low

sheet resistance $\sim 700\Omega/_\square$. Rather, the lack of indium atoms in the base region is sought after because of the prominent dopant passivation of p-InGaAs due to the strong In-C bonding reported and observed in-house during MOCVD regrowths [42, 43, 44]. p-GaAsSb, as shown later in the work, also provides a lower contact resistivity perhaps due to Sb-containing layers' strong surface pinning close to the valence band edge for both n- and p-doping that reverses the effect of surface charge carrier depletion [45, 46]. A 30% improvement in base access resistance R_{bb} with a p-GaAsSb base over p-InGaAs base has been reported [47]. The top 2.5 nm of base layer is doped at 15×10^{19} cm^{-3}, with the rest 17.5 nm graded from 15×10^{19} cm^{-3} at the emitter side to 8×10^{19} cm^{-3} at the collector side. Composition grading is also included for With no need for a base-collector conduction band grading, 100 nm of InP doped at 7×10^{16} cm^{-3} is immediately below the intrinsic base. The subcollector design is identical to DHBT64.

2.4 TLM Resistance Test Structure

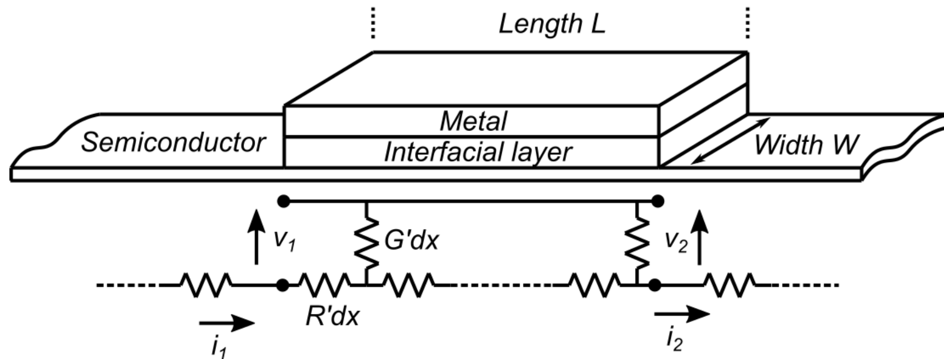

Figure 2.9: TLM modeling for contact resistance

The transmission line method resistance test structure enables the extraction of contact resistivity ρ_c between a metal contact and an underlying semiconductor layer, as well as sheet resistance ρ_s of the semiconductor layer [48]. As its name suggests, the

transmission line method models a metal/semiconductor contact as a section of a transmission line as shown in Fig. 2.9, where the metal sheet resistance is assumed to be negligible. Thus, for the contact region, it is obvious that

$$R' = \frac{\rho_s}{w} \tag{2.26}$$

$$G' = \frac{w}{\rho_c} \tag{2.27}$$

And voltage and current as a function of position along the contact is given by

$$V_1 = V_2 \cosh(\gamma x) + I_2 \, Z \sinh(\gamma x) \tag{2.28}$$

$$I_1 = \frac{V_2}{Z} \sinh(\gamma x) + I_2 \cosh(\gamma x) \tag{2.29}$$

where Z is the characteristic impedance of the transmission line, and γ is the propagation constant. With no reactive components in the specific transmission line model, Z and $1/\gamma$ are more aptly defined as the contact resistance of infinitely long metal contact, and voltage & current transfer length

$$R_{c,L=\infty} = Z = \frac{1}{w}\sqrt{\rho_s \rho_c} \tag{2.30}$$

$$L_T = 1/\gamma = \sqrt{\frac{\rho_c}{\rho_s}} \tag{2.31}$$

In a typical TLM test structure, where a pair of large metal contacts of identical length L are separated by a varying gap distance L_{gap}, the overall resistance measured would be

$$R_{total}\left(L_{gap}\right) = 2R_c + \frac{\rho_s}{W} L_{gap} \tag{2.32}$$

where R_{total} is a linear function of L_{gap}, with a slope of $\frac{\rho_s}{W}$, and a vertical intercept of $2R_c$ (Fig. 2.9).

When the length of the metal contact L is greater than a few L_T, $R_c \approx R_{c,L=\infty} = \frac{1}{w}\sqrt{\rho_s \rho_c}$. Therefore, contact resistance in devices with sufficiently long contact lengths, e.g. source/drain contacts in III-V HEMT, R_c can be thought as independent of contact length L, and is inversely proportional to contact width, or gate length in the case of III-V HEMT. However, when L is on the order of, or less than L_T, R_c must be expressed in this analytical form for further inspection

$$R_c = \frac{\sqrt{\rho_s \rho_c}}{W} \coth(\frac{L}{L_T}) \tag{2.33}$$

$$R_c \approx \frac{\sqrt{\rho_s \rho_c}}{W} \text{ when } L > 3L_T\text{, classic large contact limit} \tag{2.34}$$

$$R_c \approx \frac{\rho_c}{WL} + \frac{\rho_s L}{3W} \text{ when } L < 3L_T\text{, small contact solution} \tag{2.35}$$

The small metal contact solution in Eq. 2.35 is of particular interest in InP HBT because the single-sided base contact width $W_{b,c}$ is on the order of $1 \sim 3L_T$, and is larger than R_c given by the classic large contact limit in Eq. 2.34. Thus, it is of paramount importance to ensure careful extraction of ρ_s and ρ_c from TLM test structures for accurate prediction & fitting of device RF performance with the correct small-signal model.

2.5 RF Device Measurement

Small-signal 2-port S-parameter measurements of RF HBT are performed on a vector network analyzer with the internal bias-tees enabled. Fig. 2.10 shows a fictious VNA with port 1 lacking an internal bias-tee, and port 2 equipped with one [49]. The reason VNA internal bias-tees are preferred over conventional external components for transistor characterization is that the internal ones are placed before the test port receiver couplers

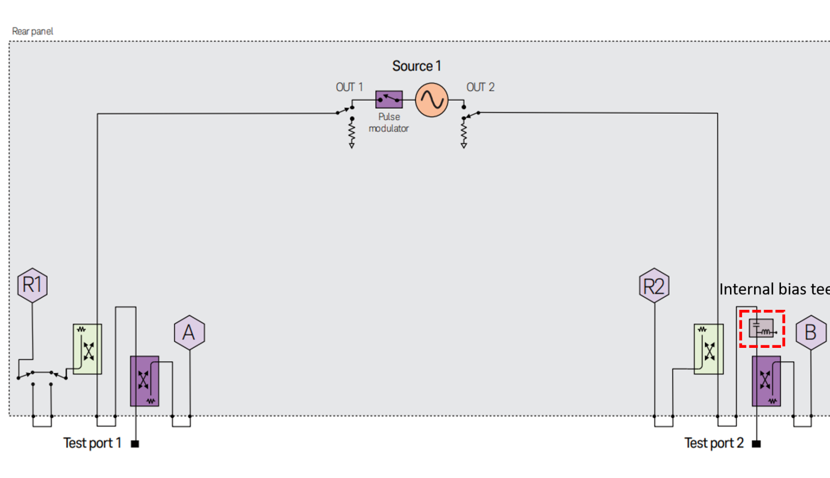

Figure 2.10: Block diagram of a fictious VNA without an internal bias-tee along port 1's signal path, and with an internal bias-tee along port 2's signal path [49]

(purple blocks before the receivers denoted by "A" and "B" in Fig. 2.10) along the signal paths, whereas external bias-tees are placed after the test port receiver couplers. Therefore, source power must undergo attenuation incurred by a pair of external bias-tees once after leaving the test ports and twice before entering the test ports, as opposed to just once in the case of internal bias-tees. The extra attenuation caused by a pair of external bias-tees could lead to a drop up to 10 dB in measured power by receiver A and B [50]. Granted that such attenuation can be theoretically removed by the calibration process. But since the noise floor is fixed, any form of attenuation would lead to degradation in the measured signal-to-noise ratio, and should be, thus, avoided. For single-finger transistors with a gate/emitter length only a few microns long, the small-signal source power is usually in the -25 dBm range. Assuming no signal attenuation within the VNA, and typical values for cable & probe losses, close to -80 dBm measured test port receiver

power is not unheard of for S_{12} measurements

$$\begin{aligned} P_{A,received} &= P_{source} - 2 \times [IL_{bias-tee} + IL_{cable} + IL_{probe}] - S_{12} \\ &= -25 \text{ dBm} - 2 \times [10 \text{ dB} + 0.5 \text{ dB} + 1.5 \text{ dB}] - 30 \text{ dB} \\ &= -79 \text{ dBm} \end{aligned}$$

Spurious S_{12} can be measured if the IF bandwidth of the VNA system is above 1 kHz using the numbers above. In practice, a positive source power slope is applied to combat diminishing SNR at higher frequencies caused by the insertion loss of the components along the signal path.

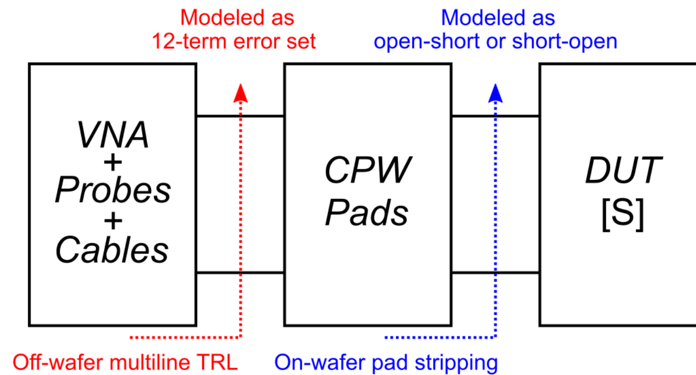

Figure 2.11: Two-tier calibration scheme to move reference plane to transistor

A two-tier calibration scheme is used for device S-parameter measurements (Fig. 2.11). First, an off-wafer calibration moves the reference plane to probe tips using a commercially available impedance standard substrate[iii] placed on the auxiliary RF absorbing ceramic chuck of the probe station[iv] [51, 52, 53]. Multiline thru-reflect-line calibration is performed with a nominal 1 ps thru standard, a synthesized 10-mm-above-chuck mid-air open (reflect) standard, and five lines of nominal 3 ps, 7 ps, 14 ps, 27 ps, and 50 ps de-

[iii]Cascade Microtech 104-783
[iv]MPI TS 150-THZ

lays. A probe tip overtravel between 75 and 125 μm is attained following the alignment marks on the ISS. Distance between the probes is adjusted to 1 μm precision between different lines using the integrated digital micrometers on the micropositioners [53]. A source power of 0 dBm, and an IF BW of 100 Hz are used for the calibration routine. A 12-term error set is inferred from a closed-form 8-term error-box model implemented in WinCal XE 4.5 using the NIST multiline TRL algorithm, and sent to the VNA to complete the calibration [54, 55]. A calibration is deemed valid when all of the five delay lines are measured to have <-50 dB ripple-free return loss vs. frequency, and linear phase vs. frequency relations seen in Fig. 2.12 (left).

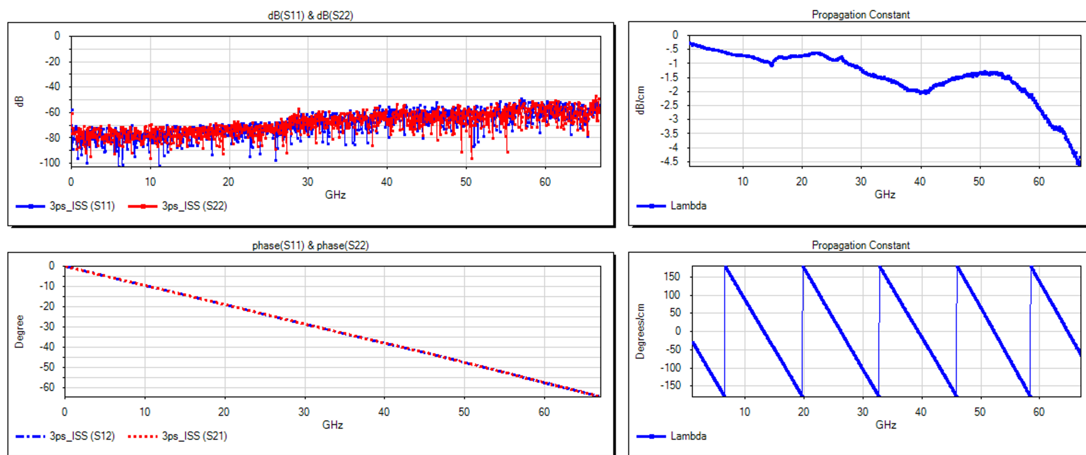

Figure 2.12: Calibration validation on a 3 ps delay line standard for return loss and phase vs. frequency

Note *no* nominal 50 Ω matched load standard is used in the multiline TRL routine. Because the characteristic impedance of a nominal 50 Ω resistor cannot be exactly $50 + j0\ \Omega$ across, or in fact at any point within, the entire DC-67 GHz range due to parasitics and boundary conditions [51]. Therefore, by measuring the *complex* propagation constant as a function of frequency of multiple lines, multiline TRL makes no assumption about the ISS parameters, and is more accurate than other VNA calibration methods that require a matched nominal 50 Ω standard (e.g. SOLT, and LRRM) [56]. Fig. 2.12 (right) shows

the modeled complex propagation constant with non-zero angle with respect to the real axis.

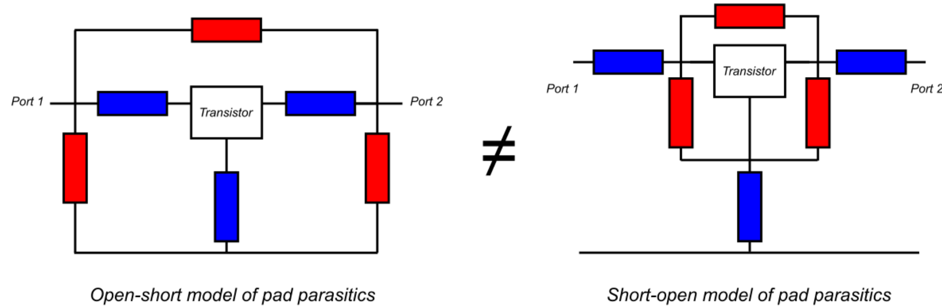

Figure 2.13: Equivalent models for open-short embedding and short-open embedding, where red boxes denote parallel Y-components, and blue series Z-components

Next, to strip pad parasitics embedded around the HBT, both open-short and short-open deembeddings are performed, and the more conservative result is reported. Open-short and short-open deembeddings can be theoretically shown to return different results. Because for a reciprocal passive network, in this case the pad structures, the anti-diagonal terms of their Y- and Z-matrix are identical, leaving 3 distinct circuit components required to model their behaviors *at a given frequency* using either a π-section or a T-section equivalent model. At the specific frequency where a π-section and a T-section equivalent models are found, the two are equivalent. On the other hand, both open-short and short-open deembeddings rely on a hybrid L-section equivalent circuits that can model only 2 distinct components, and, therefore, do not return identical results and are not equivalent even at a given frequency (Fig. 2.13).

For open-short deembedding, the parallel Y-components are assumed to be outside of the series Z-components. Thus, measured S_{meas} are first converted to Y_{meas}, and

$$Y'_{trans} = Y_{meas} - Y_{open}$$

where Y_{open} are the Y-parameters of the open pad structure, Y'_{trans} are the calculated Y-parameters describing the transistor and the series parasitics within which it is still embedded. The Z-parameters of the series parasitics can be then found using

$$Z_{series} = (Y_{short} - Y_{open})^{-1}$$

and the open-short deembedded transistor is given by

$$Z_{trans_{open-short}} = (Y'_{trans})^{-1} - Z_{series} = (Y_{meas} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1}$$

which can be easily converted back to S-parameters in ADS using the native functions.

Short-open deembedding is similarly carried out, but assuming the series parasitics are on the outside of the parallel parasitics, and therefore

$$Y_{trans_{short-open}} = (Z_{meas} - Z_{short})^{-1} - (Z_{open} - Z_{short})^{-1}$$

which can also be converted back to S-parameters easily.

Difference less than 1 dB between open-short and short-open deembeddings can be achieved with off-wafer multiline TRL calibration, and tends to be worse using other calibration methods. However, for transistor measurements above 67 GHz, on-wafer multiline TRL calibration is ideal and should be used instead [57]. Improved TRL layout over [57] has been designed in this work to fully isolate signal pad from the underlying InP substrate for minimized substrate mode coupling.

2.6 Conclusions

In this chapter, the design and scaling of the conventional InP mesa HBT are introduced with correlations between device geometry and equivalent circuit components derived. Two complementary sets of circuit components are identified in terms of device scaling requirements. The first set of circuit components, including various resistances and transconductance, are *extrinsically* constant throughout device scaling, but *intrinsically* improved material/process properties necessitate scaling requirements. Scaling of the second set of circuit components, including the various capacitances and RC delays, is achieved by geometric scaling of the thicknesses of the epitaxial layers as well as lateral lithographic dimensions of the emitter, base, and collector mesa widths. To first order, lithographic feature sizes are scaled quadratically with respect to vertical epitaxial scaling for a net linear decrease in parallel plate capacitances, though an appreciable increase in diffusion capacitances cannot be ignored in highly scaled devices at and beyond the 130 nm technology node.

Conventional figures of merit f_T/f_{max} introduced in Chapter 1 are revisited with geometric device parasitics accounted for. The parasitics add additional RC time delays not present in the simple analysis of the 1D band diagram. High current density effects leading to emitter starvation, Kirk effect, and transconductance degradation are explained with practical solutions detailed in terms of doping engineering. Gunn oscillation due to $\Gamma - L$ scattering in the drift collector is avoided by increasing the dopant concentration above that of the Kirk current density. Three intrinsic InP HBT device epitaxial designs are tabulated, two of which are p-InGaAs based, and the other p-GaAsSb.

Challenges to technology development beyond the 130 nm node are presented. Doping limits and non-decreasing contact resistivities cause resistance scaling to lag the requirements set by the technology roadmap, while quadratic shrinkage in lithographic feature

size and overlay accuracy creates a considerable barrier to entry for not only academic research activities, but also commercial III-V foundries. Other previously negligible parasitics – e.g. emitter-base gap resistance, base metal self-inductance, etc. – start to dominate device performance. An architectural shift in the current triple mesa device structure is needed for InP HBT.

Finally, resistance measurements using transmission line method test structures, and device RF characterization and calibration methods are introduced for accurate extraction of critical device equivalent circuit parameters.

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Chapter 3

Analysis of Regrown p-GaAs Extrinsic Base InP HBT

A detailed analysis of regrown p-GaAs extrinsic base InP HBT is given in this chapter. First, f_{max} non-scaling due to emitter sidewall thickness constraint, and challenges in low contact resistivity base metallization faced by conventional p-InGaAs base mesa HBT are reviewed. A minimum 30 nm emitter sidewall thickness for device reliability considerations leads to actual C_{cb} scaling 20% slower than the technology roadmap, demanding a 20% faster reduction in R_{bb} to compensate for the added RC delay. R_{bb} scaling, however, is hindered by stagnating progress in low contact resistivity metallization technology. Consequently, sub-100 nm HBT scaling fails to deliver an improved f_{max} above 1.1 THz. Regrown p-GaAs extrinsic base HBT holds the promise of enabling further f_{max} scaling to 2.1 THz thanks to its higher achievable active p-type dopant concentration and lower contact resistivity. Device physics of regrown extrinsic base HBT is explained. Finite element modeling in ADS is performed to predict the device's f_{max}.

3.1 Theory of Regrown Extrinsic Base InP HBT

Eq. 2.21 and 2.17 for C_{cb} and R_{bb} in Section 2.2 are together the most important equations for RC time delays that dominates f_{max} scaling in InP HBT, and are, thus, reiterated here

$$R_{bb} = \rho_{bs}\frac{W_e}{12} + \rho_{bs}\frac{W_{b,gap}}{2} + \frac{\sqrt{\rho_{bc}\rho_{bs}}}{2}\coth(\frac{W_{bc}}{L_{T,b}})$$
$$C_{cb,tot} \approx (1 - \Phi_{cancel})\,\frac{\varepsilon_{InP}(2W_{b,gap} + 2W_{b,c} + W_e)}{T_{j,cb}}$$

where Φ_{cancel} is the C_{cb} cancellation factor that decreases C_{cb} by $\sim$ 30% under high collector current injection that is routinely exploited in modern record f_{max} HBT [1, 2].

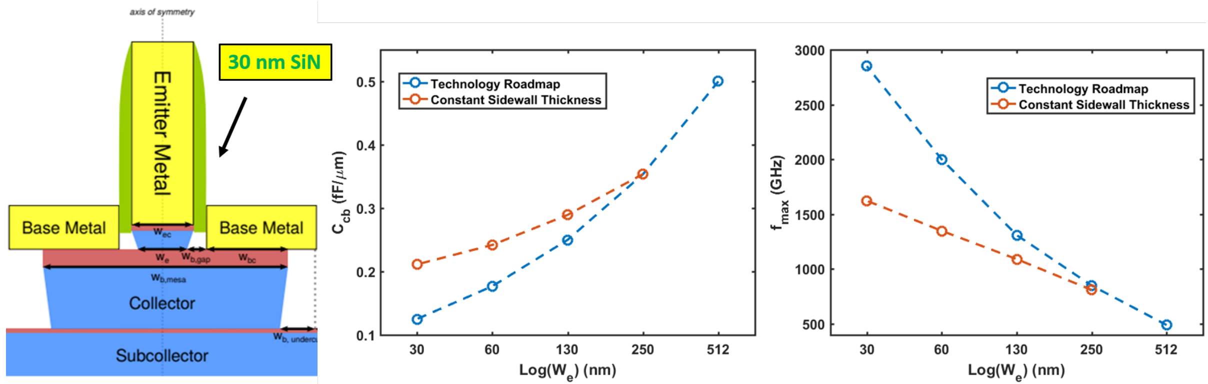

Figure 3.1: C_{cb} non-scaling due to constant emitter dielectric sidewall thickness, and resultant slow-down in f_{max} scaling

Fig. 3.1 shows the first technical problem with C_{cb} scaling using values listed in the scaling roadmap (Table 2.1), with the practical exception that the thickness of the emitter dielectric sidewall cannot be scaled past 30 nm for device reliability issues. At the 130 nm technology node, a $\sim$ 20% expected increase in C_{cb} over the roadmap target is attributed to non-scaling of dielectric sidewall thickness, Therefore, calculated f_{max} at 130 nm is 200 GHz below the roadmap target, and is in excellent agreement with experimental results with a measured 1.1 THz f_{max} [1, 3]. Similarly, calculated f_{max}

at 60 nm is expected to be 1.3 THz, and 700 GHz or 40% below the roadmap target. Virtually, actual C_{cb} scaling is $\sim$ 20% slower than prediction.

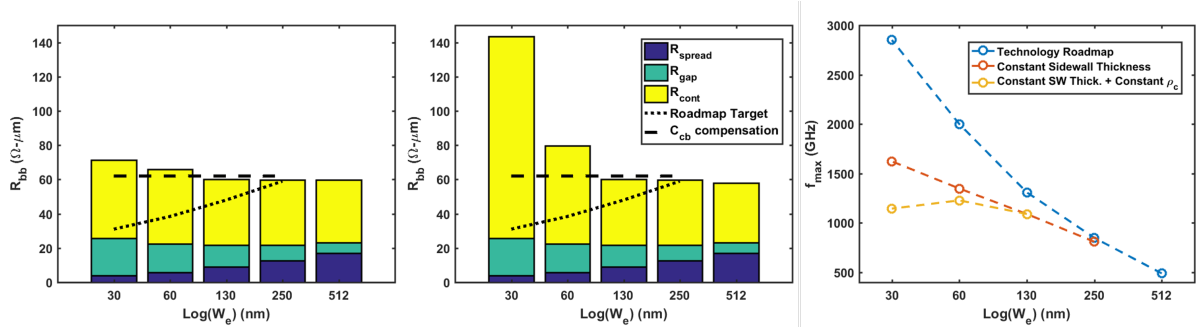

Figure 3.2: R_{bb} non-scaling due to constant sidewall thickness (left), together with non-scaling 5 Ω-μm^2 contact resistivity $\rho_{b,c}$ (center), and resultant slow-down in f_{max} scaling (right)

Further, Fig. 3.2 shows breakdown of base access resistance R_{bb} in terms of spreading resistance below emitter semiconductor R_{spread}, emitter-base gap resistance R_{gap}, and base metal contact resistance $R_{b,c}$ plotted with a constant 30 nm emitter sidewall thickness and a scaling $\times$0.5/generation base contact resistivity $\rho_{b,c}$ (left), and a constant 30 nm emitter sidewall thickness but a non-scaling 5 Ω-μm^2 $\rho_{b,c}$ (center). With the correct $\times$0.5/generation $\rho_{b,c}$ scaling, R_{bb} adheres to the roadmap target down to the 130 nm node, but misses the requirement at 60 nm and below due to a substantial increase in R_{gap}. When the effects of a non-scaling 5 Ω-μm^2 $\rho_{b,c}$ – due to limits of attainable dopant concentration, and surface pinning in p-InGaAs [4, 5, 6, 7, 8] – are included, increases in both R_{gap} and $R_{b,c}$ lead to a base access resistance $>$ 30% worse than the roadmap target. Little to no f_{max} improvement is expected below the 130 nm technology node seen in Fig. 3.2 (right).

Since C_{cb} scaling is directly proportional to lithographic scaling, R_{bb} scaling employing device architectural changes that compensates for slow-down in C_{cb} scaling is desired to enable further f_{max} scaling along the technology roadmap. Dotted lines in Fig. 3.2

indicate the required R_{bb} to reset f_{max} scaling back to the blue roadmap trendline. At 60 nm emitter width, a 30%, or 20 Ω-μm, reduction in R_{bb} is needed. At 30 nm emitter width, overall $R_{bb} < 31$ Ω-μm is required, which is close to R_{gap} alone. Therefore, simultaneous reductions in $R_{b,c}$ and R_{gap} must occur for future f_{max} scaling.

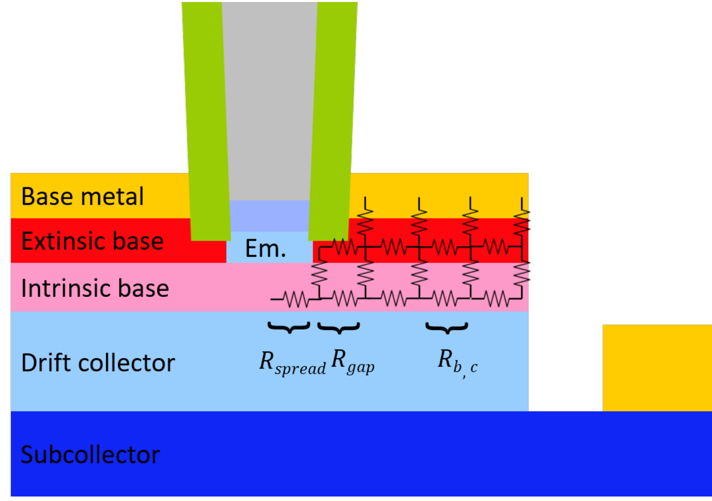

Figure 3.3: Schematic cross section of a regrown extrinsic HBT with gap region underfill

InP HBT with a MOCVD regrown p-GaAs extrinsic base that abuts the emitter semiconductor can lower both $R_{b,c}$ and R_{gap} as shown in Fig. 3.3. $R_{b,c}$ scaling is realized by p-GaAs's high achievable dopant concentration and thus a low ρ_s, and a low contact resistivity $\rho_{b,c}$ afforded by the added semiconductor thickness for reacting intermetallic compound metal contact. Abutment of p-GaAs against the emitter semiconductor lowers R_{gap} by underfilling the resistive gap region with high conductivity extrinsic base semiconductor akin to source/drain and cladding regrowths in HEMTs and lasers [9, 10]. Greater than 1×10^{21} cm^{-3} active p-type carbon doping in GaAs, an order of magnitude above its p-InGaAs:C counterpart, has been reported with a bulk resistivity of 2.34×10^{-4} Ω-cm, again an order of magnitude better than that in the record p-InGaAs results [11, 12, 13]. At 50 nm thickness, 1×10^{21} cm^{-3} p-GaAs would have a sheet resistance of 47 $\Omega/\Box$. In addition, close to or below 1 Ω-μm^2 base contact resistivity $\rho_{b,c}$ on

p-GaAs have been demonstrated [14, 15, 16].

In summary, the use of p-GaAs extrinsic base enables two improvements that are otherwise not possible in intrinsic base only InP HBT. They are

1. Lower base contact resistivity $\rho_{b,c}$ close or below 1 Ω-μm^2 for low $R_{b,c}$

2. Lower composite sheet resistance in the gap region for low R_{gap}

In the next section, base access resistance R_{bb} of a InP HBT with regrown extrinsic base is derived theoretical first, and simulated using a finite element method in Keysight Advanced Design System.

3.2 Derivation and Simulation of R_{bb} with Extrinsic Base

The second-order resistive ladder for contact resistance $R_{b,c}$ per unit emitter finger length shown in Fig. 3.3 is given by the system of equations

$$
\begin{aligned}
\frac{\partial V_{in}(x)}{\partial x} &= -\frac{\rho_{s,in}}{I_{in}(x)} \\
\frac{\partial V_{ex}(x)}{\partial x} &= -\frac{\rho_{s,ex}}{I_{ex}(x)} \\
\frac{\partial I_{in}(x)}{\partial x} &= -\frac{1}{\rho_{c,ss}}[V_{in}(x) - V_{ex}(x)] \\
\frac{\partial I_{ex}(x)}{\partial x} &= -\frac{1}{\rho_{c,ms}}V_{ex}(x) - \frac{1}{\rho_{c,ms}}[V_{ex}(x) - V_{in}(x)]
\end{aligned}
$$

where V_{in} is the voltage of the intrinsic base as a function of lateral distance x, V_{ex} voltage of the extrinsic base, I_{in} lateral current in the intrinsic base, and I_{ex} lateral current in the extrinsic base. $\rho_{s,in}$ & $\rho_{s,ex}$ are the intrinsic and extrinsic base sheet resistances. $\rho_{c,ss}$ and $\rho_{c,ms}$ are the semiconductor-to-semiconductor contact resistivity

and metal-to-semiconductor contact resistivity. With appropriate boundary conditions, $R_{b,c}$ can be found by taking the ratio of V_{in} and I_{in} at $x = 0$. The solutions to the system of equations are transcendental, and, therefore, are easier to calculate numerically in MATLAB, or to simulate in a FEM model in ADS. A 96-section FEM model in ADS agrees with numerical results returned by MATLAB to a precision of 1/10 Ω, and is used for circuit simulations.

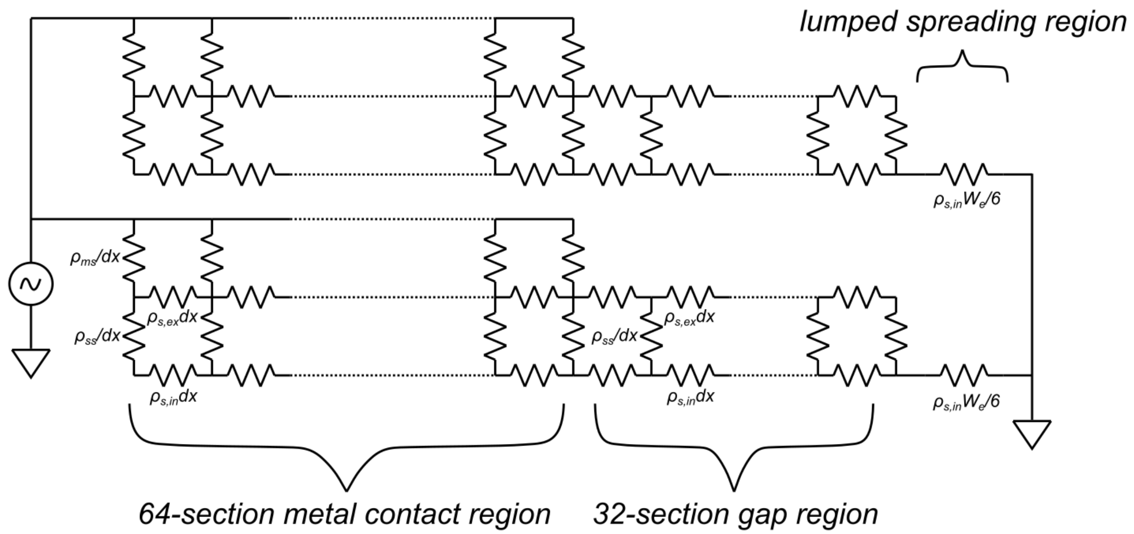

Figure 3.4: 96-section FEM model for R_{bb} ADS simulations

Validation of the FEM model is achieved by setting $\rho_{s,ex}$ to inifinity, $\rho_{s,in}$ 850 $\Omega/\square$, $\rho_{c,ss}$ zero, and $\rho_{c,ms}$ 5 Ω-μm^2 to reduce the second-order resistive ladder down to the simple first-order intrinsic base only equivalent condition. A R_{bb} of 57.3 Ω is simulated, identical that returned by Eq. 2.17 for the 130 nm node (also in Fig. 3.2). When converting the model back to second-order by setting $\rho_{s,ex}$ to a finite extrinsic base sheet resistance, and $\rho_{c,ss}$ a non-zero regrowth interfacial resistivity, one subtly arises that is the inability to accurately partition the bulk of R_{bb} between $R_{b,c}$ and R_{gap}. Because boundaries of $R_{b,c}$ and R_{gap} cannot be modeled as one-port equivalent resistors as they now have 3 terminals. As such, breakout $R_{b,c}$ and R_{gap} are found by forcing a current

through the two output terminals equal to how much it draws when the components are connected, and measuring their equivalent resistances. Therefore, the partition is approximate. The overall R_{bb} is, however, definitively simulated as shown in Fig. 3.4.

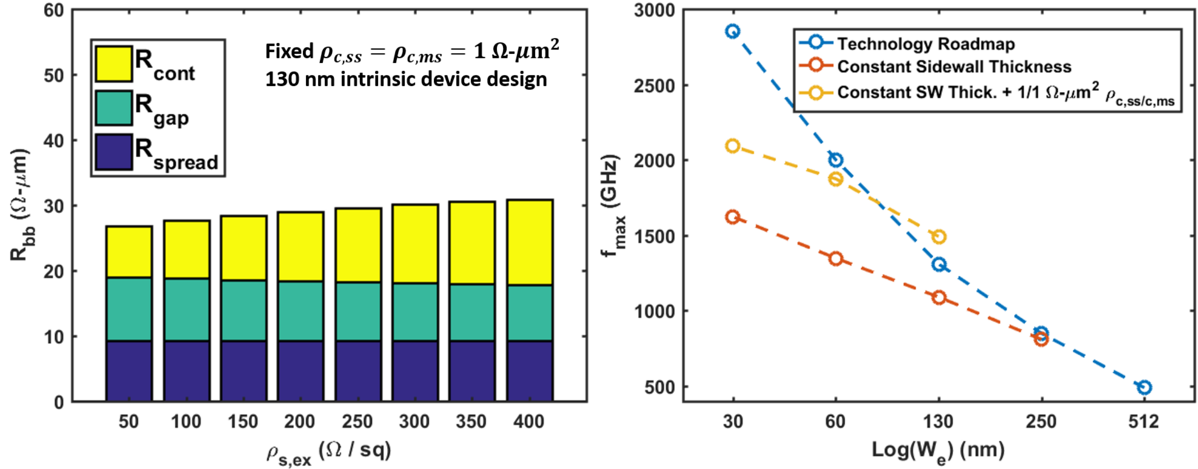

Figure 3.5: R_{bb} as a slow varying function of $\rho_{s,ex}$ between 50 $\Omega/\square$ and 400 $\Omega/\square$ (left), and simulated f_{max} across scaling generations with $\rho_{c,ss} = \rho_{c,ms} = 1$ Ω-μm^2

With a moderate regrowth interfacial resistance $\rho_{c,ss} = 1$ Ω-μm^2, an optimistic $\rho_{c,ms} = 1$ Ω-μm^2 according to best p-GaAs results [16], and 130 nm node intrinsic device parameters ($\rho_{s,in} = 850$ $\Omega/\square$, $W_{b,c} = 130$ nm, $W_{gap} = 30$ nm, and $W_e = 130$ nm), R_{bb} as a function of extrinsic base sheet resistance $\rho_{s,ex}$ is plotted in Fig. 3.5 (left). The first observation is that R_{bb} is a slow varying function of $\rho_{s,ex}$ within an experimentally reasonable range. Next, $R_{b,c}$ sees the most scaling, and corresponds to an conventional equivalent contact resistivity $\rho_{c,eq} = 0.5$ Ω-μm^2, lower than both $\rho_{c,ms}$ and $\rho_{c,ss}$.[i] As a result, overall R_{bb} is scaled by a factor of $\sim$2 to 30 Ω-μm normalized to unit emitter finger length, leading to a $\sim 1.4\times f_{max} = 1.5$ THz for a 130 nm technology with regrown extrinsic base. Similarly, with the same $\rho_{c,ss} = \rho_{c,ms} = 1$ Ω-μm^2, a 60 nm technology with

[i] $\rho_{c,eq}$ defined as the contact resistivity required to yield a given $R_{b,c}$ between the base metal and intrinsic base in a conventional HBT. In this case, $R_{bb} = \frac{\sqrt{\rho_{s,in}\rho_{c,eq}}}{2}\coth(\frac{W_{b,c}}{L_T}) = 30$ Ω-μm, and, therefore, $\rho_{c,eq} = 0.5$ Ω-μm^2.

regrown extrinsic base would have a 1.9 THz f_{max}, a mere 0.1 THz below the roadmap trendline. A 32 nm node technology would have a 2.1 THz f_{max}, including the effects of slow-down of C_{cb} scaling due to constant 30 nm emitter sidewall thickness as shown in Fig. 3.5 (right).

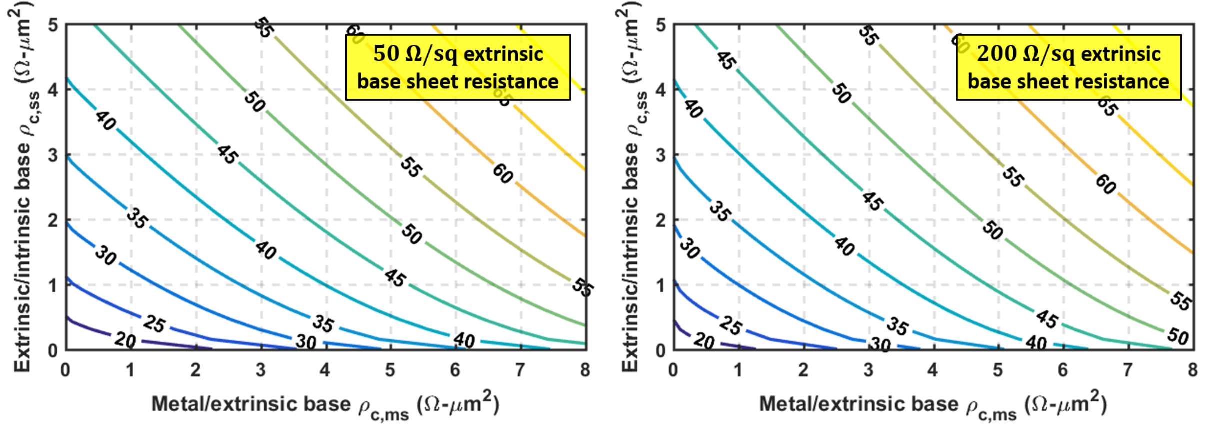

Figure 3.6: R_{bb} (Ω-μm) as a function of contact resistivities $\rho_{c,ss}$ and $\rho_{c,ms}$, assuming 130 nm intrinsic device parameters

R_{bb} as a function of contact resistivities $\rho_{c,ss}$ and $\rho_{c,ms}$, assuming 130 nm intrinsic device parameters, is plotted in Fig. 3.6. Again, extrinsic base sheet resistance $\rho_{s,ex}$ is seen to have negligible effect on overall R_{bb} except for extremely low regrowth interfacial resistivity $\rho_{c,ss} < 1$ Ω-μm^2, where a lower $\rho_{s,ex}$ helps relax the requirement for contact resistivity $\rho_{c,ms}$ between the extrinsic base and base metal contact. For $\rho_{c,ss} > 1$ Ω-μm^2, influence of $\rho_{s,ex}$ is virtually non-existent. The important observation is that R_{bb} reduction is feasible with regrown extrinsic base *without* an improvement in base metallization technology. Even with a conservative 5 Ω-μm^2 base metal contact resistivity, by virtue of a low resistance extrinsic base and an *acceptable* regrown interface, a ∼ 25% reduction in R_{bb} is accessible. With a lower < 5 Ω-μm^2 base metal contact resistivity allowed by the low sheet resistance extrinsic base, a > 35% reduction in R_{bb} can be achieved by careful balancing between $\rho_{c,ms}$ and $\rho_{c,ss}$. Table 3.1 shows the simulated R_{bb} using 3

	Conventional 130 nm HBT	130 nm HBT with 200 $\Omega/\square$ extrinsic base		
$\rho_{s,in}$ ($\Omega/\square$)	850	850	850	850
$\rho_{s,ex}$ ($\Omega/\square$)	-	200	200	200
$\rho_{c,ms}$ (Ω-μm^2)	5	5	2	1
$\rho_{c,ss}$ (Ω-μm^2)	-	4	2	1
$\rho_{c,eq}$ (Ω-μm^2)	5	5	1.3	0.5
R_{bb} (Ω-μm)	60	60	38	30
f_{max} (GHz)	1100	1100	1360	1500

Table 3.1: Simulated R_{bb} in a 130 nm technology with a 200 $\Omega/\square$ extrinsic base

different sets of $\rho_{c,ms}/\rho_{c,ss}$. The equivalent $\rho_{c,eq}$ in all 3 cases are equal or lower than the metal/semiconductor contact resistivity $\rho_{c,ms}$.

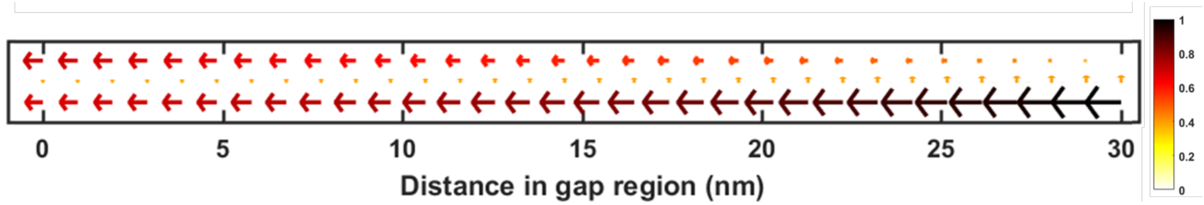

Figure 3.7: Simulated current distribution in the gap region with 850/200 $\Omega/\square$ intrinsic/extrinsic sheet resistances, and 1 Ω-μm^2 regrown interfacial resistivity (Note the small vertical vectors denote current flows across the intrinsic/extrinsic interface)

Simulated current distribution in the 30 nm gap region is highlighted in Fig. 3.7 with 850/200 $\Omega/\square$ intrinsic/extrinsic sheet resistances, and 1 Ω-μm^2 regrown interfacial resistivity. The left side is connected to a 130 nm $W_{b,c}$ base contact region, and the right side a 130 nm W_e emitter. Unity current flows in from the bottom right emitter terminal, whereas 52% flows out of the gap region in the top extrinsic base layer through the top left terminal, and 48% flows out in the intrinsic base layer through the bottom left terminal. Recall exact R_{gap} is ill-defined in this 3-terminal resistive ladder setup. However, overall R_{bb} is exact, and the approximate breakdown is 10.82/9.80/9.18 Ω-μm $R_{b,c}/R_{gap}/R_{spread}$ with the extrinsic base, compared to 35.17/12.65/9.18 Ω-μm $R_{b,c}/R_{gap}/R_{spread}$ without the extrinsic base.

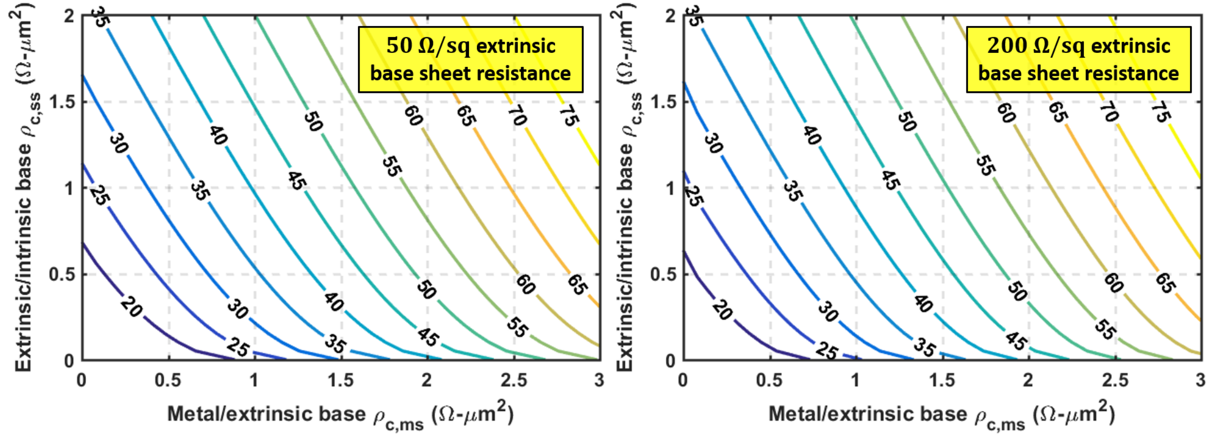

Figure 3.8: R_{bb} (Ω-μm) as a function of contact resistivities $\rho_{c,ss}$ and $\rho_{c,ms}$, assuming 30 nm intrinsic device parameters

At the 30 nm node, where $W_{b,c} = W_{gap} = W_e = 30$ nm, and $\rho_{s,in} \sim 1450$ Ω/□, regrown extrinsic base could be the only viable base contact technology for f_{max} scaling as suggested in Fig. 3.8. A moderate base metal contact resistivity $\rho_{c,ms} = 2$ Ω-μm^2, together with a $\rho_{c,ss} = 1.3$ Ω-μm^2, is needed for the 1.6 THz f_{max} prediction in Fig. 3.5 including C_{cb} non-scaling effects, much more reasonable than the 1 Ω-μm^2 base metal contact resistivity required by the conventional roadmap. Again, if an optimistic yet feasible 1/1 Ω-μm^2 $\rho_{c,ms}/\rho_{c,ss}$ discussed in previous simulation for the 130 nm node is used instead, a f_{max} of 2.1 THz is simulated for the 30 nm technology node.

3.3 Simluated 50 Ω Power Cell Performance

Comparison between simulated common-emitter S-parameters of the conventional 130 nm technology and that with a 30 Ω-μm R_{bb} regrown extrinsic base up to their f_{max} are shown in Fig. 3.9 for a $L_e = 20$ μm power cell. Noticeable differences are the increased voltage gain S_{21}, higher Mason's unilateral gain U, and lower series resistance evident

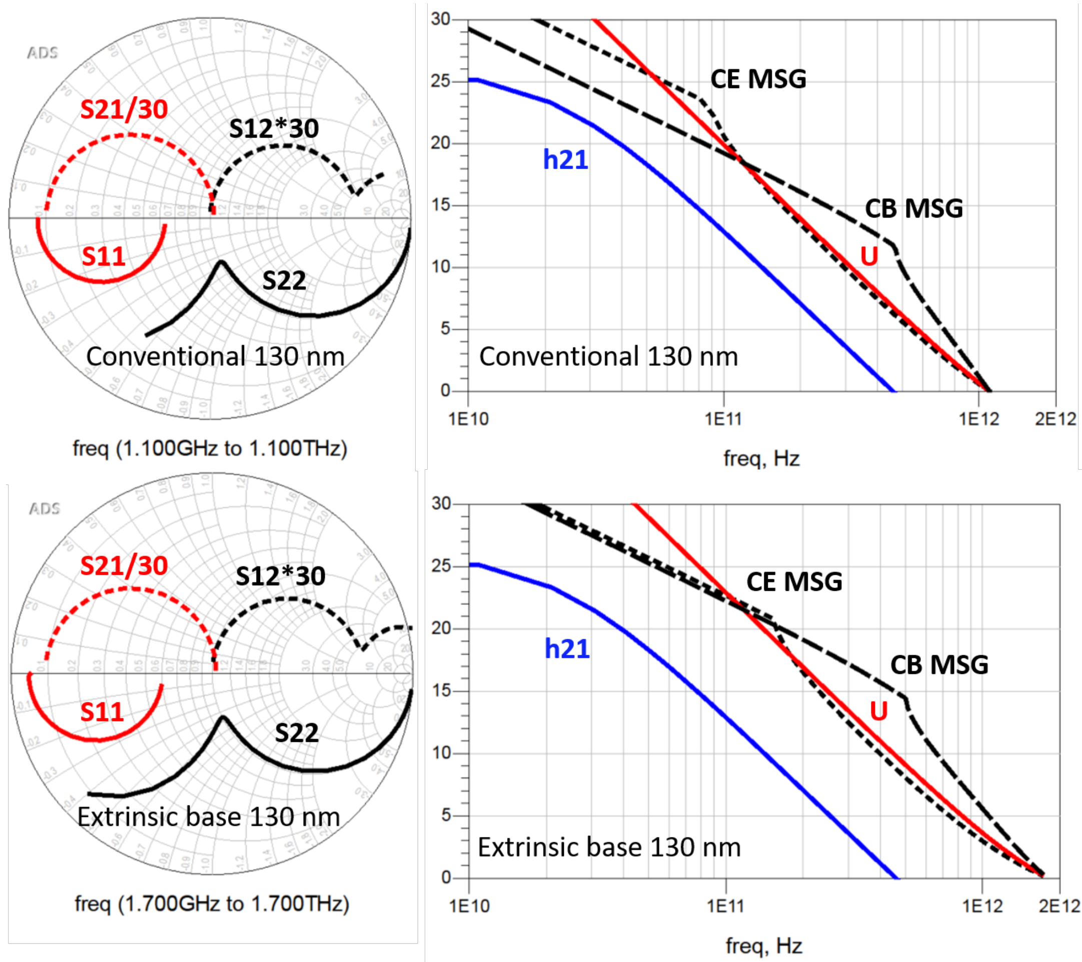

Figure 3.9: Simulated S-parameters of a $L_e = 20$ μm 50 Ω matched power cell in the conventional 130 nm technology (top), compared to that in a regrown extrinsic 130 nm technology with $0.5 \times R_{bb}$

in high frequency S_{11}, whereas S_{12} and S_{22} witness negligible changes as expected. The negligible shift in S_{22} deserves more inspection as Re$\{Z_{out}\}$ is relatively constant as well. Between 100 and 300 GHz, Re$\{Z_{out}\}$ is between 0.914 Z_0 and 1.037 Z_0 for good conjugate gain matching, which coincides with the $L_e = 20$ μm power cell's optimal power matching at 50 Ω ($I_{max} = 3 \times 20 = 60$ mA, and $V_{max} - V_{knee} = 3.5 - 0.5 = 3.0$ V).

However, one potential issue with R_{bb}−only scaling by regrown extrinsic base to achieve a higher f_{max} to a circuit designer is the applicability of its higher gain under

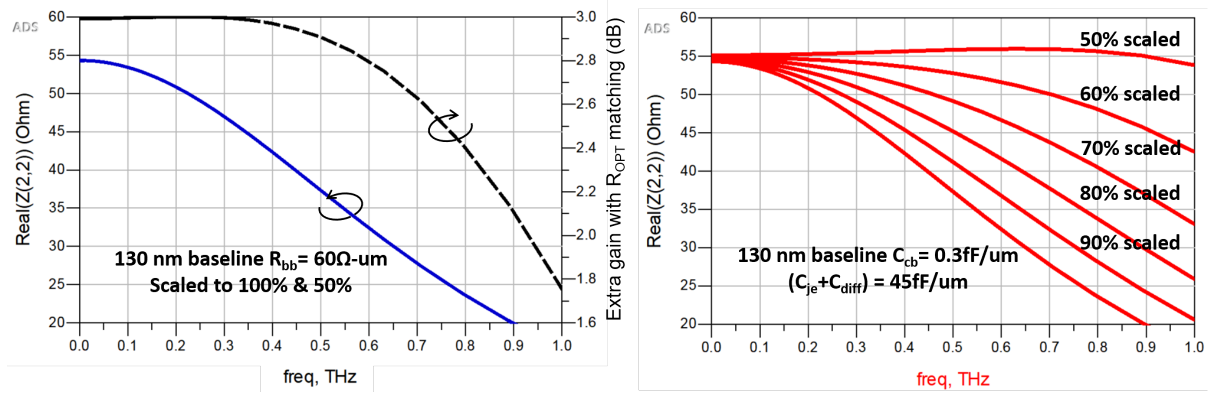

Figure 3.10: Simulated loadline impedance for maximum gain of a $L_e = 20\ \mu$m 50 Ω matched power cell in a regrown extrinsic 130 nm technology with $0.5 \times R_{bb}$, and diminished power gain at high frequency when matched to R_{OPT} (left) vs. in a fictious HBT technology with its C_{cb} scaled to 50%

optimal power matching Z_{OPT} conditions (see Section 1.5). Fig. 3.10 (left) shows Z_{conj} vs. frequency for a $L_e = 20\ \mu$m regrown extrinsic base HBT with R_{bb} scaled at 100% and 50%. The transistor is matched for optimal power matching at 50 Ω ($I_{max} = 3 \times 20 = 60$ mA, and $V_{max} - V_{knee} = 3.5 - 0.5 = 3.0$ V). Simultaneous high gain matching that fully utilizes the extra 3 dB power gain from a $1.4\times f_{max}$ is readily available up to 400 GHz, after which separation of Z_{OPT} and Re$\{Z_{conj}\}$ leads to less power gain improvement. On the contrary, if lithographic $C_{cb}-$only scaling can be achieved for a similar $1.4\times f_{max}$ improvement, the associated 3 dB extra power gain is available beyond 1 THz owing to the higher associated f_T.

Nevertheless, given simultaneous R_{bb} and C_{cb} scaling along the technology roadmap is broken, $R_{bb}-$only scaling by extrinsic base regrowth is still the more technologically viable option, whereas $C_{cb}-$only scaling is hindered by the minimum emitter sidewall thickness discussed above. Attention must be paid to the handling of the higher power gain achieved by regrown extrinsic base on a circuit level. For example, to reverse the adverse effects of the shifting Z_{out} at a higher frequency, neutralization techniques on the circuit level can be employed, though the required impedance can be challenging to

realize in passives[ii].

3.4 Conclusions

In this chapter, C_{cb} and R_{bb} non-scaling due to minimum emitter sidewall thickness for device reliability concerns and the associated increase in gap resistance R_{gap}, together with difficulties with sub-5 Ω-μm^2 base metallization on p-InGaAs are reviewed. Greater than 1 THz f_{max} scaling by conventional lithographic scaling is, therefore, problematic beyond the 130 nm technology node owing to the increased RC time delays. Performance of the regrown extrinsic base process module in reducing both R_{gap} and $R_{b,c}$ for low overall R_{bb} is simulated in ADS using a 96-section FEM model. Two important observations are evident. First, suppression of high R_{gap} can be achieved by using an only moderately conductive extrinsic base. Second, $R_{b,c}$ reduction can be realized more easily with an extrinsic base layer as its low sheet resistance and high dopant concentration relax the requirements for low contact resistivities. Overall R_{bb} as a function of contact resistivities at the metal/semiconductor and regrowth interface are calculated with a 50 $\Omega/\square$ and 200 $\Omega/square$ sheet resistance extrinsic bases. At the 130 nm technology node, a regrown extrinsic base is expected to increase device f_{max} to 1.6 THz. At the 32 nm technology node, a 2.1 THz f_{max} is extrapolated. The applicability of the device's higher theoretical power gain in power amplifiers is briefly discussed, with issues of and circuit-level solutions to diminishing improvement in power gain under optimal power matching at higher frequency demonstrated. In general, the device provides a higher gain up to f_{max}, and is technologically more viable than lithographic scaling.

[ii] e.g. An 8 pH feedback inductor with an appropriate DC block allows the +3 dB power gain to be accessed at 700 GHz, but could be hard to realize in layout.

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Chapter 4

Process Module Development

This chapter details challenges encountered and milestones achieved in the development of compatible process modules for the regrown extrinsic base InP HBT. To enable sub-100 nm scaling, a refractory emitter metal contact technology able to withstand high temperature MOCVD regrowths is demonstrated in co-sputtered $Ti_{4wt\%}W$. Emitter contact resistivity $\sim 2.7\,\Omega\text{-}\mu\text{m}^2$, comparable to conventional dual-layer W/$Ti_{4wt\%}W$ stack is measured. The $Ti_{4wt\%}W$ contact is homogeneous in composition throughout the entire structure, providing a reliable means to deep sub-100 nm emitter metal width scaling with controlled sidewall profile. p-GaAs, as opposed to p-InGaAs, is regrown as the extrinsic base both for its higher maximum active dopant concentration ($\sim 4\times\ 10^{20}$ cm^{-3}), and ease of integration with the device process flow. Design of sub-100 nm emitter DC large area devices are explained as a means for rapid experimentation. Integration between the MOCVD regrowth & dopant re-activation anneal and the bulk of the HBT process is aided by electrical and TEM characterizations of the large area base-collector diode test structures.

4.1 Development of Self-aligned Sub-100 nm Emitter Metal Contact

Conventional ICP dry etched $Ti_{10wt\%}W$ emitter metal used within the group faced challenges in terms of process control and yield beyond 250 nm. Previous generation of students have successfully scaled the process to the 130 nm technology node by employing a dual-layer $W/Ti_{10wt\%}W$ emitter metal stack that provides an overall vertical profile, with noticeable undercut in the W portion, and tapered slope in the $Ti_{10wt\%}W$. Vertical overall profile is achieved by fine tuning $W/Ti_{10wt\%}W$ layer thicknesses and dry etch parameters shown in Fig. 4.1 [1]. Also visible in the figure, however, is strong undercut/notching effect at the $W/Ti_{10wt\%}W$ interface within the dual-layer emitter metal stack that diminishes yield. The conventional process is, therefore, deemed too risky for sub-100 nm scaling at the beginning of the project.

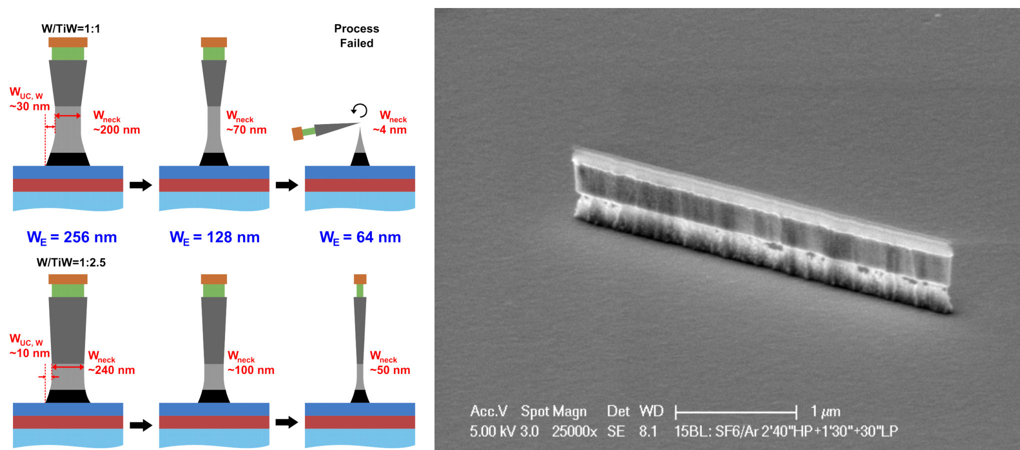


Figure 4.1: Improved conventional dual-layer $W/Ti_{10wt\%}W$ emitter metal stack by previous group members (left), and notching at the dual-layer interface (right) [1]

Atomic layer deposition of refractory TiN and Ruthenium emitter metal in a semi-damascene fashion is explored as an alternative. In the semi-damascene process, Molybdenum liner is first deposited by e-beam evaporation, followed by thick sacrificial silicon

sputtering. Narrow width, high aspect-ratio Si etching is achieved with a single-step deep RIE process. Conformal ALD TiN or Ru is deposited, and etched back together with the supporting Si to reveal the final emitter metal structure (Fig. 4.2). The ALD Ru emitter metal stack is highly resistive, measured at 200 $\Omega/\square$ for a 30 nm thick film. Oxygen signals are found in EDAX analysis, suggesting presence of RuO_x in the film, typically associated with inefficient cracking and reduction of the Ru-precursor in the ALD system. Also emitter metal test structures are more resistive due to formation of teardrops at the seam of the vertical emitter metal contact. Both issues could be related to the low 300 mTorr maximum reactor pressure at the time as normal Ru CVD conditions are in the few to tens of Torr [2, 3, 4]. The process is abandoned due to tool availability at UCSB[i].

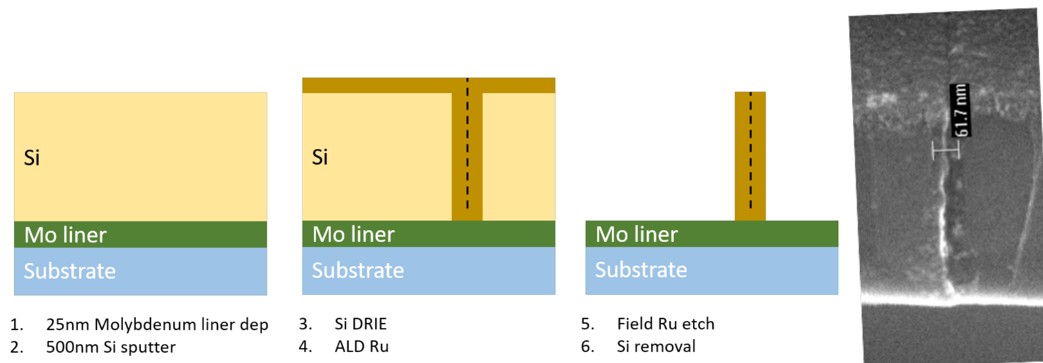


Figure 4.2: ALD Ru semi-damascene process (left), and a 60 nm wide 500 nm via filled with Ru before etch back (right)

The second emitter metal process attempted is similar to the semi-damascene ALD process, where a sacrificial Si mandrel is used to define the emitter metal. Instead of tricky-to-fill high aspect-ratio trenches, Mo is evaporated around the vertical sidewalls of the Si mandrel. A double-patterning lithographic step is introduced to cut the Mo rings into emitter contact strips. The process does not rely on gas phase diffusion of chemical metal precursors, and, thus, has better resistance to void formation. An aspect ratio

[i]The ALD system has since been upgraded to a maximum pressure of 2000 mTorr, and Ru ALD growth seems working for another project within the group.

up to 6 has been demonstrated in emitter metal test structures. However, higher aspect ratios lead to mechanical failure of the metal structures. Horizontal metal nucleation creates cracks that propagate along the width of the emitter contacts, resulting in bends upon Si mandrel removal (Fig. 4.3).

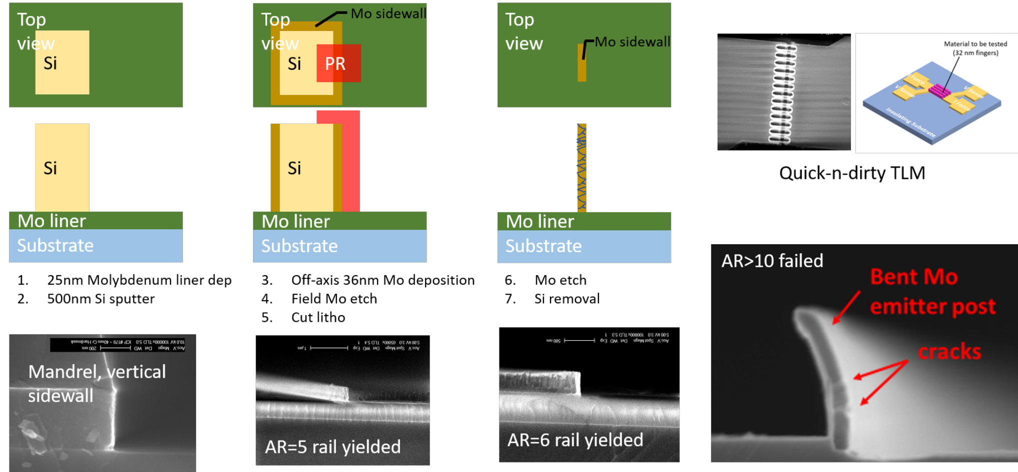


Figure 4.3: Double-patterning Si sidewall process with bent emitter metal structures above 10 aspect ratio

High yield scaling to sub-100 nm and sub-60 nm emitter widths is eventually accomplished with an improvement over the conventional W/Ti$_{10wt\%}$W process. Previous in-house 250 nm node W/Ti$_{10wt\%}$W emitter uses a 1:2.5 thickness ratio for an effective Ti weight fraction of $\sim$ 6.5%. Fig. 4.4 (left) shows that the overall emitter metal contact with a Ti$_{10wt\%}$W composition generates a strongly tapered profile when dry etched, almost vertical with an effective Ti$_{6.5wt\%}$W composition, and undercut with pure W. Co-sputtering with pure Ti and W targets allows fine tuning of alloy composition that should offer a homogeneous emitter metal contact that is vertical from top to bottom when dry etched. Such alloy composition is found to be Ti$_{4wt\%}$W. At 4 weight percent Ti, the emitter metal contact can be even scaled to 45 nm width and 550 nm height with high yield as shown in Fig. 4.4 (right). Electrically, the contact performed similarly compared to the dual-layer counterpart as expected, and has a emitter contact resistivity of 2.7

Ω-μm^2 by emitter-base diode flyback measurements. The refractory nature of $Ti_{4wt\%}W$ also means the emitter metal contact could be placed down before the relatively high temperature MOCVD extrinsic base regrowth, eliminating issues with deep submicron re-alignment of the emitter contact in early regrown extrinsic base InP HBT from the 1990s [5].

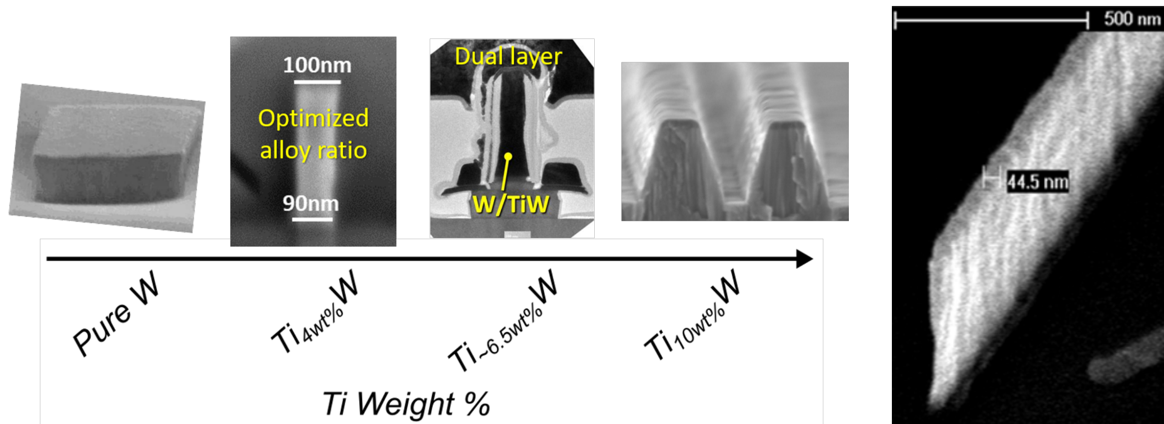


Figure 4.4: Ti weight percent in $Ti_{xwt\%}W$ vs. sidewall profile (left), and sub-60 nm scaling capability of homogeneous $Ti_{4wt\%}W$ alloy composition

Finally, photoresist for the emitter stripe e-beam lithography has been changed from the organic novolac resins to hydrogen silsesquioxane, an inorganic $HSiO_x$ compound, dissolved in methylisobutylketone. After pre-bake, e-beam exposure, and development in an inorganic developer, HSQ turns into a hydrogenated SiO_x film. The exposed EBL patterns are transferred down to a chromium hardmask before emitter metal dry etch. The use of HSQ over organic resists limits redeposition of organic matters on samples to minimize contamination of the MOCVD system used for subsequent extrinsic base regrowth.

4.2 Development of p-GaAs Selective Growth by MOCVD

Chemical vapor deposition regrowth of heavily doped semiconductors has been extensively used in the Si VLSI CMOS technology since the planar 32 nm technology node for raised source/drain [6]. Compared to ion implantation, precise doping and composition profiles can be obtained at desired locations on wafer, together with additional ability to impart strain on the device active region for improved performance [7].

For III-V semiconductors, metalorganic chemical vapor deposition regrowth of heavily doped n++ semiconductors are routinely performed in InGaAs/InP and GaN HEMT for low source/drain resistances [8, 9]. Compared to the other widely used III-V regrowth technique – molecular beam epitaxy, MOCVD exhibits a lower maximum active dopant concentration, but a much higher degree of tunability in growth selectivity [10, 11, 12, 13].

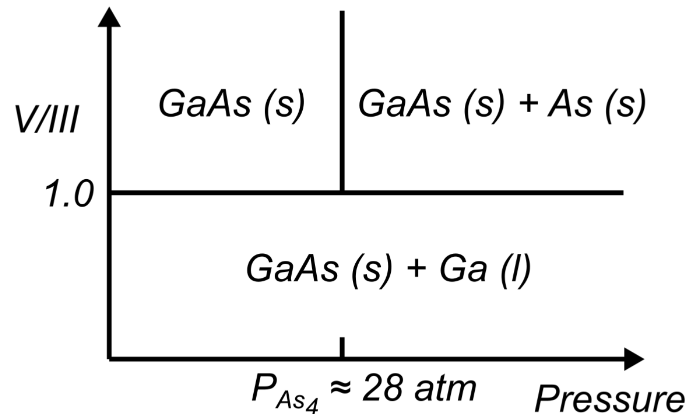


Figure 4.5: GaAs phase diagram appropriate for MOCVD growth

The selectivity of MOCVD regrowth can be tuned by a wide range of growth parameters, including growth temperature, reactor pressure, carrier gas, kinetics of different precursor species and supplied precursor partial pressure, and V/III ratio between the group-V and group-III precursor species. Generally, a high growth temperature and a

low reactor pressure enhance surface diffusion of both group-V and group-III adatoms, leading to better selectivity as adatoms are more likely to reach the correct lattice sites [14]. One important distinction between MOCVD and solid source MBE under normal growth conditions is the high V/III ratio. Because only group-V precursors are volatile at normal growth temperatures. Therefore, when not enough group-V species are present on the growth surface to bond with group-III species, droplets of elemental group-III species, e.g. Ga or In, could form, causing phase separation. Fig. 4.5 shows the GaAs phase diagram with a varying V/III ratio and growth pressure [15]. For a V/III ratio less than 1, two separate phases are stable with a Ga-rich liquid phase present. At both high V/III ratio and extremely high growth pressure >28 atm, again a two-phase system is present as As_4 precipitates out. However, most MOCVD system cannot reach a few atmospheric pressures for safety and practical reasons. Thus, MOCVD growth almost exclusively takes place with a high V/III ratio typically in excess of 100. As a result, MOCVD grown III-V materials are usually group-V rich, introducing deep $EL2$ traps near midgap that lower active dopant concentrations that are virtually absent in MBE grown materials [16, 14].

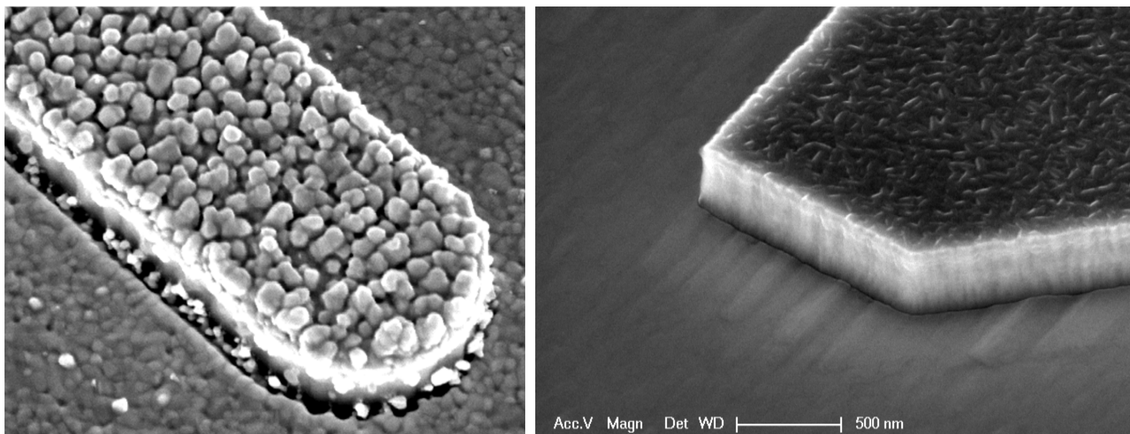


Figure 4.6: In-rich precipitates on a test emitter metal structure (left) vs. good growth selectivity (right)

Fig. 4.6 (left) shows In-rich precipitates on a test emitter metal structure as well as visibly discontinuous regrown p-InGaAs film in the field on the device intrinsic InGaAs base. The nominal V/III in this case is < 1 using tertiarybutylarsine (TBAs) as the group-V source, and trimethylindium (TMIn) and trimethylgallium (TMGa) as the group-III sources. Growth temperature is 500°C. Good selectivity is achieved at 660°C with a nominal V/III ratio of 25 as seen in Fig. 4.6 (right). However, sheet resistance of the 75 nm film shown in Fig. 4.6 (right) is on the order of 10 kΩ/□ with n-type Hall effect conduction. It has been well reported that carbon is an amphoteric dopant in (In)GaAs where successful n- or p-type doping depends on whether the carbon atoms take group-III or group-V lattice sites as seen in Fig. 4.7 [17, 18]

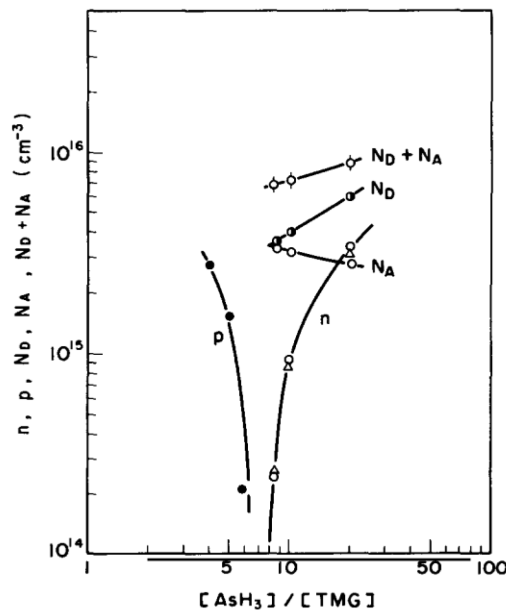


Figure 4.7: Amphoteric doping of carbon in GaAs as a function of V/III ratio [17]; Reprint with Permission © AIP 1984[ii]

A series of p-InGaAs growths at 500°C and a nominal V/III ratio of 18 is performed

[ii]Reproduced from "T. Nakanisi, *The growth and characterization of high quality MOVPE GaAs and GaAlAs*, Journal of Crystal Growth, vol. 68, no. 1, pp. 282–294, 1984.", with the permission of AIP Publishing.

in an attempt to strike a balance between growth selectivity and active p-type dopant concentration. Flow of TMIn, TMGa, and TBAs are kept constant. The free variable in this study is the nominal flow of the carbon precursor CBr_4, ranging from 17 sccm to 150 sccm carried by H_2. The corresponding CBr_4 molar flow can be calculated using the associated values found in Appendix B. A strong shift to smaller lattice constant of the epitaxial layer is observed with increasing amount of CBr_4 flow seen in Fig. 4.8. Dopant-induced lattice mismatch $\sim 0.5\%$ [19] alone cannot explain the large shift in XRD peak position. Therefore, preferential etching of InAs over GaAs by CBr_4 is suspected to be cause of the experimental finding [20].

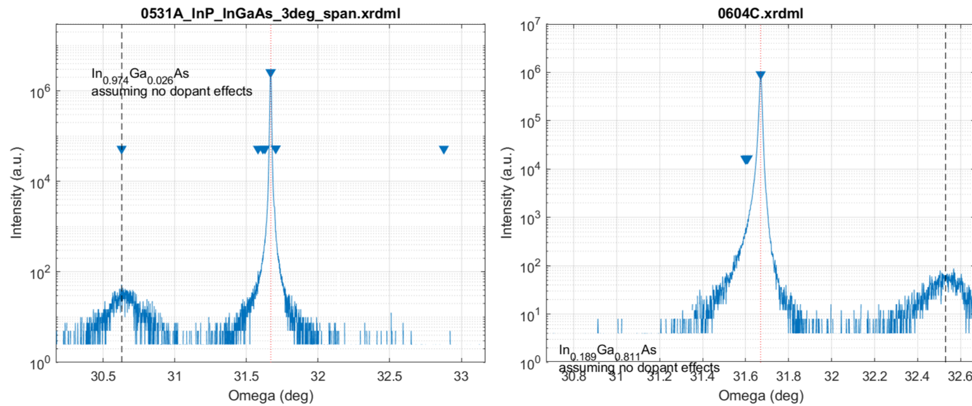


Figure 4.8: At constant TMIn, TMGa, and TBAs flows, a 17 sccm CBr_4 flow yields almost pure relaxed InAs (left), whereas a 150 sccm CBr_4 flow yields almost pure relaxed GaAs (right)

Increasing TMIn flow, or decreasing CBr_4 flow accordingly can yield close to lattice-matched InGaAs on InP shown in Fig. 4.9. But the sheet resistance of 060719D shown in Fig. 4.9 for a thickness of 75 nm is around 4 $k\Omega/\square$. A sister recipe to 060719D with TMIn removed for pure p-GaAs growth on InP returns a sheet resistance of 260 $\Omega/\square$ with p-type Hall carrier concentration of 6×10^{19} cm^{-3}, confirming the suspicion that either TMIn and CBr_4 would consume each other in an etching action leading to lower carbon incorporation, or the weaker In-C bond compared to Ga-C bond would cause

carbon to more easily take group-III lattice sites and self-compensate [21, 22, 23], or a combination of the two effects are present in this case.

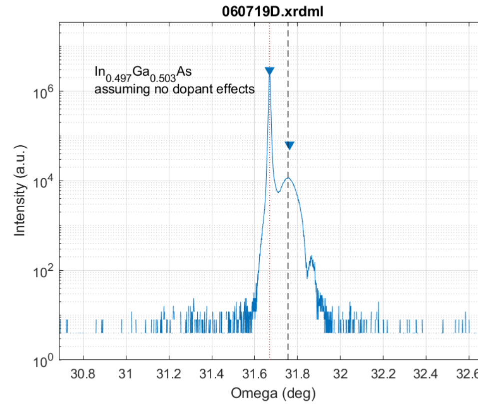


Figure 4.9: Close to lattice-match carbon-doped InGaAs grown at 500°C

CBr_4 is reported to have an etch rate of III-Vs proportional to $\exp\left(-\frac{1}{T}\right)$ [24]. Thus, growth temperature is further lowered to 450°C to suppress potential InAs etching. At 450°C, cracking efficiency of TMGa is found to be reduced to 10%. For economic reasons and to preserve precursors, TEGa is used instead for its lower cracking temperature. $In_{0.3}Ga_{0.7}As$ with a sheet resistance of 300 $\Omega/\square$ is obtained for a 75 nm thick film, corresponding to an active p-type concentration of close to 6×10^{19} cm^{-3}. The sheet resistance is low enough for device application with good selectivity. The recipe is documented in Appendix B. However, cross-hatch patterns are visible under SEM and after device isolation etch, strong undercut along the cross-hatch is visible under the Nomarski interference microscope (Fig. 4.10).

Electrical measurements of the processed base-collector diodes with a p-InGaAs extrinsic base shows appreciable leakage current under reverse bias.

The cross-hatch patterns suggest phase separation of InAs and GaAs at the 450°C growth temperature [25, 26]. Lower growth temperature at 435°C has also been studied as [25] reports cross-hatch patterns could be avoided at even lower temperatures. But

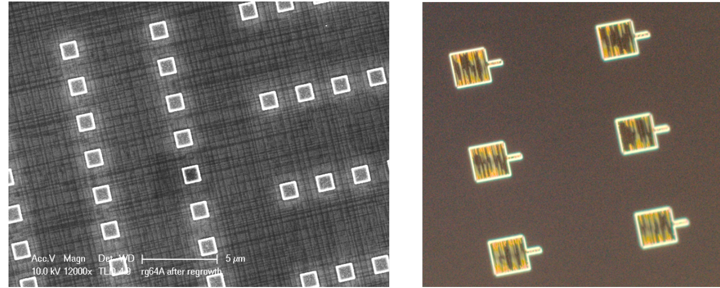


Figure 4.10: Cross-hatches visible after growth (left), and undercut along cross-hatches after isolation (right)

cracking efficiency of TEGa is reduced to 40%. Therefore, further p-InGaAs growth and device integration is put on hold. Instead lattice mismatched regrown p-GaAs extrinsic base on p-InGaAs intrinsic base is used for the remainder of the work. Lattice mismatched regrown contacts have been attempted within the group on n-channel HEMT devices with reasonable results [27].

Heavily carbon doped p-GaAs regrowth is more straightforward as the lack of indium eliminated the aforementioned problems. The current production p-GaAs recipe is developed along p-InGaAs growth experiments. The recipe is documented in Appendix B. For a 60 nm film, sheet resistance is in the range of 200 $\Omega/\square$, with an active dopant concentration $\sim 2 - 4 \times 10^{20}$ cm^{-3}.

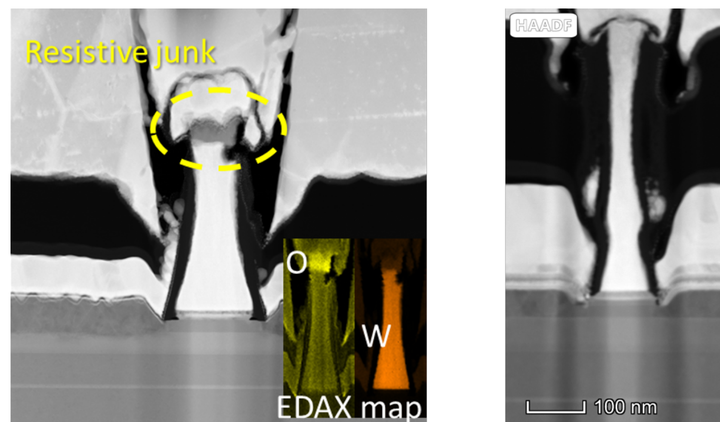


Figure 4.11: Tungsten emitter structure oxidized after RTA anneal (left) vs. no oxidation after in-situ MOCVD anneal

Through large-area DC device runs, it is found that hydrogen radicals specifically from cracking of group-V precursors can passivate the intrinsic p-InGaAs base. Device DC current gain β above 100 (vs. $\sim$ 20 originally) has been observed, indicating a $\sim 3 \times 10^{19}$ cm^{-3} active dopant concentration in the intrinsic p-InGaAs base after regrowth. This represents a 60% passivation of the intrinsic carbon doping by hydrogen incorporation. In order to drive out the hydrogen atoms in the intrinsic base and reverse dopant passivation, ex-situ N_2 rapid thermal anneal and subsequently MOCVD in-situ N_2 anneal are performed. The RTA systems at UCSB have enough stray O_2 content that oxidation of the device tungsten metal contact is observed after ex-situ anneals after MOCVD regrowths evident in Fig. 4.11 (left). By implementing an in-situ N_2 anneal in the MOCVD before cooldown, oxidation of the emitter contact is prevented. Fig. 4.12 shows the overall growth sequence with the in-situ N_2 anneal. Degree of dopant reactivation after the anneal appears to be a function of emitter mesa width, and is discussed in Section 5.2.

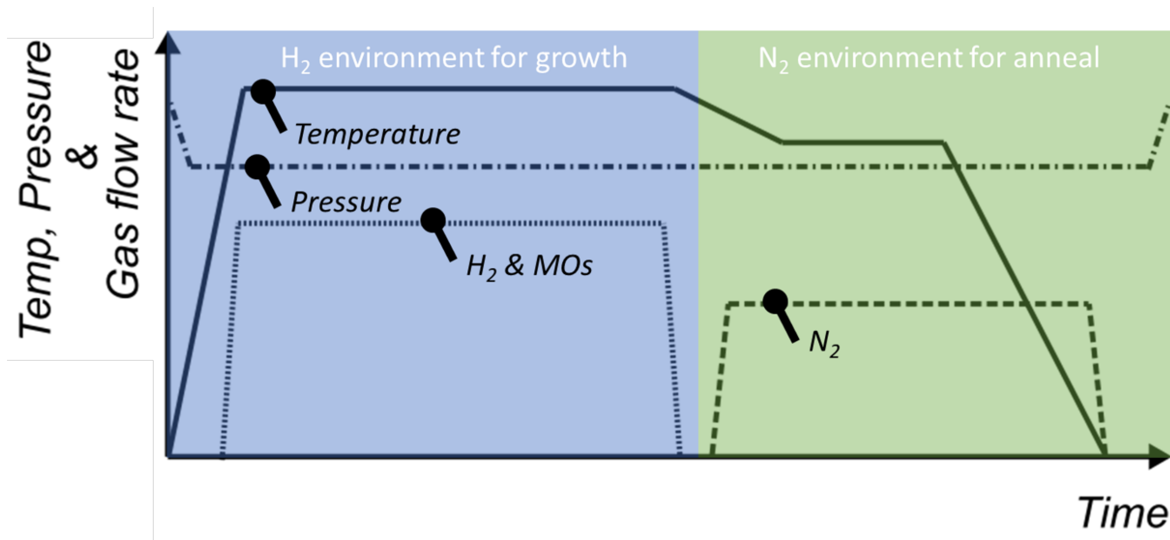


Figure 4.12: Optimized MOCVD regrowth sequence with an in-situ N_2 anneal

Finally, the use of p-GaAs over p-InGaAs for the extrinsic base facilitates simple implementation of regrowth abutment to the intrinsic emitter semiconductor for low

gap resistance R_{gap}. Because the larger bandgap of the extrinsic GaAs compared to that of the intrinsic InGaAs impedes electron diffusion directly from the n-InP emitter semiconductor to the p-GaAs as seen in Fig. 4.13 (left), whereas the negligible valence band discontinuity between p-GaAs and p-InGaAs poses no issue to hole injection at the extrinsic/intrinsic base interface shown in Fig. 4.13 (right). Regrowth abutment of p-GaAs to n-InP, therefore, does not increase the effective intrinsic emitter-base junction area that would otherwise degrade current injection efficiency if a p-InGaAs extrinsic base were to abut the n-InP semiconductor.

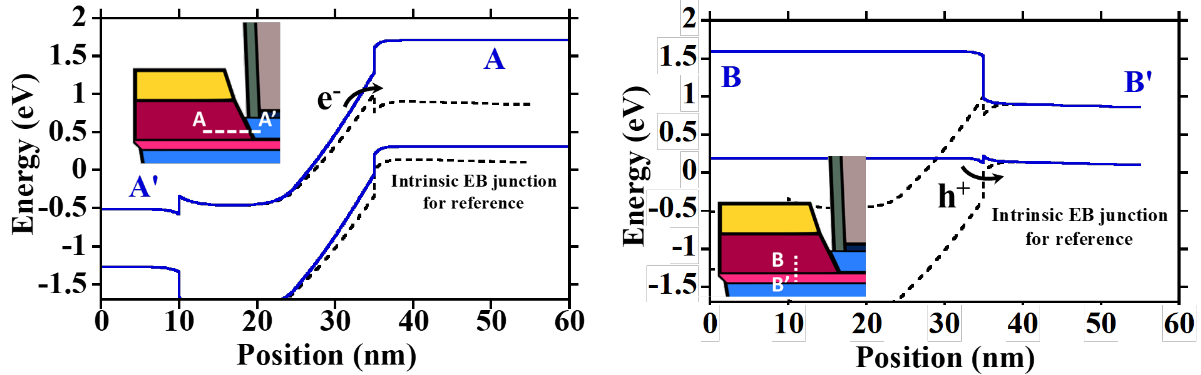


Figure 4.13: Band alignment between the extrinsic/intrinsic base and the intrinsic emitter semiconductor (left), and that between the extrinsic and intrinsic bases (right)

4.3 Sub-100 nm Emitter DC Large Area Regrown Extrinsic Base HBT

The full-fledged RF InP HBT process flow includes submicron base-collector mesa isolation, submicron base & collector metal posts, precise back-end planarization, and interconnect metallization. The usual turn-around time in an academic cleanroom like the one at UCSB is about two months. With the MOCVD regrown extrinsic base process module, one batch of RF devices per three months is expected. In order to expedite pro-

cess development/integration and failure diagnosis, a simplified DC large area process flow is employed for the first half of this thesis.

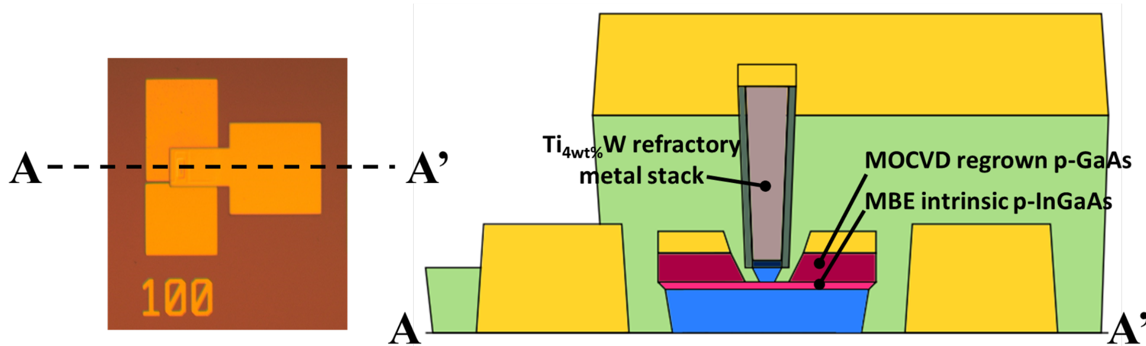


Figure 4.14: Schematic cross section of a DC large area regrown extrinsic base HBT where "100" denotes $W_e = 100$ nm

The DC large area process flow features a nominal 90 nm EBL emitter contact metal width, in line with actual RF device dimensions for the extraction of RF-critical base access resistance R_{bb}. MOCVD extrinsic base regrowth is carried out immediately after emitter semiconductor wet etch. The base contact metal is lifted off in a self-aligned fashion, similar to the RF process, to minimize the distance between emitter and base metal contacts. However, the base post landing pad has been enlarged to $35 \times 35\,\mu\text{m}^2$, to eliminate the need for the low yielding base metal posts. Base-collector mesa is formed with a wet etch process step. After collector metal contact lift-off, the devices are passivated in BCB without isolation and ashed back to reveal the emitter metal contact. Large metal 1 emitter pad is lifted off. Finally, BCB in the field is blanket ashed away to allow access the large base & pads for DC probing. All lithographic definitions, except the EBL emitter metal contact, are achieved with the i-line GCA Autostep 200 system with a relaxed overlay accuracy $\sim 1\mu$m, together with the above simplifications streamlined the process flow, and allow a fast 4-week turnaround time. Fig. 4.15 (right) shows a tilted SEM view of the finish device, where BCB is sandwiched in M1 and the device

active region.

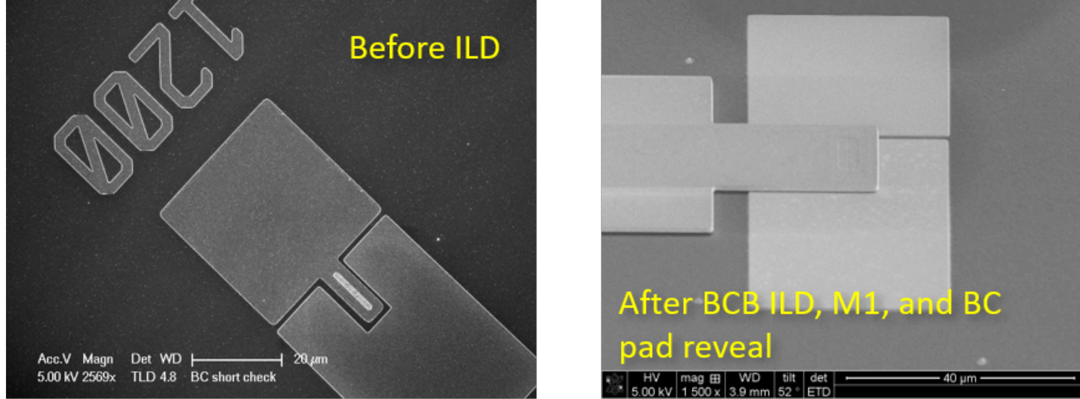


Figure 4.15: A finished DC large area device with a $W_e = 1200$ nm emitter before BCB planarization (left), and after field BCB removal to reveal base & collector contact pads

In terms of device performance, a few distinctive features are expected and, indeed, measured only in the DC devices. First, the large $35 \times 35\,\mu\text{m}^2$ base-collector pads incur a large $C_{cb,ex}$ on the order of ~ 1.5 pF that effectively shorts the input terminal above 10 GHz. As a result, erroneous fitting of small-signal equivalent circuit ensues if one extracts RF parameters from such DC devices. Thus, the devices are relegated to DC testing only. Second, the large $5\,\mu$m base mesa width $W_{b,mesa}$ in the intrinsic device region sees two consequences stemming from a low current density in the drift collector region: 1). a higher safe emitter current density, and 2). better heat dissipation, lacking the typical thermal induced negative resistance feature in device output characteristics at $J_e > 3$ mA/μm and $V_{CE} > 2$ V. Third, the DC devices exhibit a large common-emitter offset voltage $V_{CE,offset}$ that is proportional to the base-collector junction area. As $V_{CE,offset}$ occurs when $I_e = I_c$, or roughly

$$I_e = I_c$$
$$A_e\, J_{e,diff}\, \exp(\frac{qV_{BE}}{\eta_e k_B T}) = A_c\, J_{c,diff}\, \exp(\frac{qV_{BC}}{\eta_c k_B T})$$

assuming $J_{e,diff}$ and $J_{c,diff}$ are area-independent, and η_e, and η_c are unity, since $V_{CE,offset} = V_{CB} - V_{BE}$ then

$$\text{Collector/emitter area ratio} = \frac{A_c}{A_e} = \frac{J_e}{J_c}\exp[\frac{q}{k_B T}(2V_{BE} + V_{CE,offset})]$$
$$V_{CE,offset} \approx C_0 \times \ln(\frac{A_c}{A_e}) \tag{4.1}$$

For comparison, $V_{CE,offset}$ is usually $\sim$ 0.15 V for a typical RF device with a 3:1 collector/emitter area ratio, whereas $V_{CE,offset}$ for the large area DC devices are $\sim$ 0.3 V for a much larger collector/emitter area ratio.

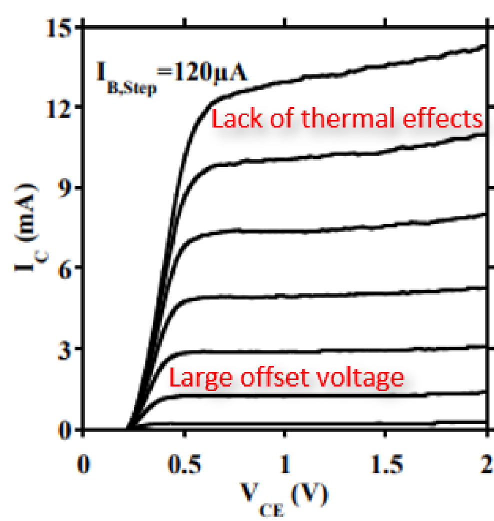


Figure 4.16: Output characteristics of a typical DC large area device with unique features

The above quirkiness of the DC large area devices are shown in the device common-emitter output characteristics in Fig. 4.16.

4.4 Base-collector Diode with Extrinsic Base

The large 35 $\times$ 35 μm^2 base DC probing pads also provide another means to allow fast metrology. After base-collector mesa etch, and even before collector metallization, it is

possible to land one DC needle probe on the large area base contact pad, and another on the field subcollector semiconductor for rapid testing of the extrinsic/intrinsic base-collector diode. Such test structures have proven valuable in device integration as they can be readily measured in the cleanroom with crude probe station setups, and can capture the earliest signs of integration failures.

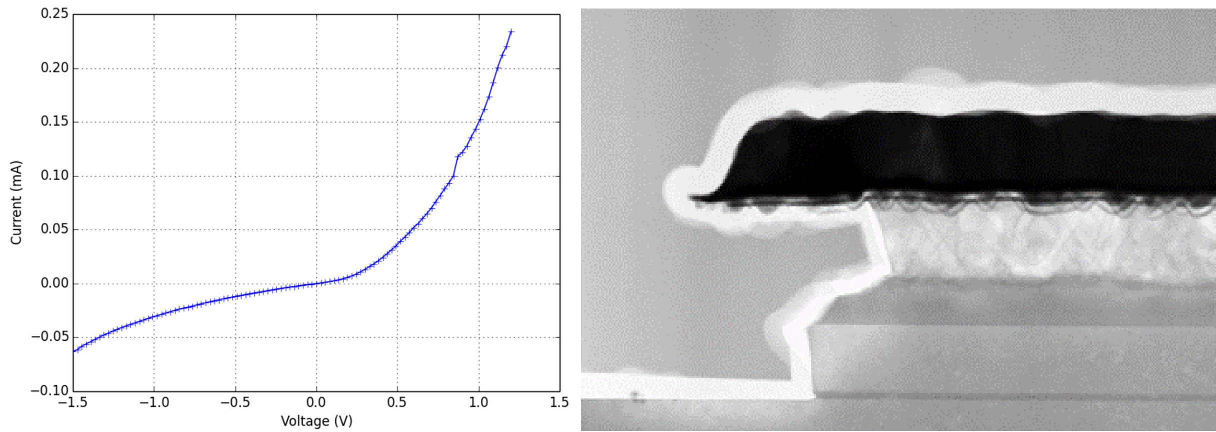


Figure 4.17: Base-collector test diode characteristics of RG62B (left) and TEM cross section of the diode structure

For example, Fig. 4.17 (left) shows an early attempt at integrating the MOCVD regrown extrinsic base and dopant reactivation anneal module process modules with the RG62B device process flow. It is immediately obvious that the base-collector test diode has a strong leakage behavior under reverse bias, as well as a high access resistance limiting current density under forward bias. Transmission electron microscope images are promptly taken of the structure, revealing defect propagation from the regrown extrinsic base down to the intrinsic device structure as well as dislocation-induced surface pits visible at the metal/regrowth interface as shown in Fig. 4.17 (right) [28]. The exact mechanism that causes defect propagation is unknown. However, compared to later base-collector test diodes that are re-activated using an in-situ MOCVD anneal, RG62B undergoes an ex-situ rapid thermal annealing cycle that is proven to have issue like oxygen

contamination, and temperature drifts. Rapid thermal cycling, thermal stress, and high N_2 flow rates in the RTA system could also be responsible for the observed phenomena.

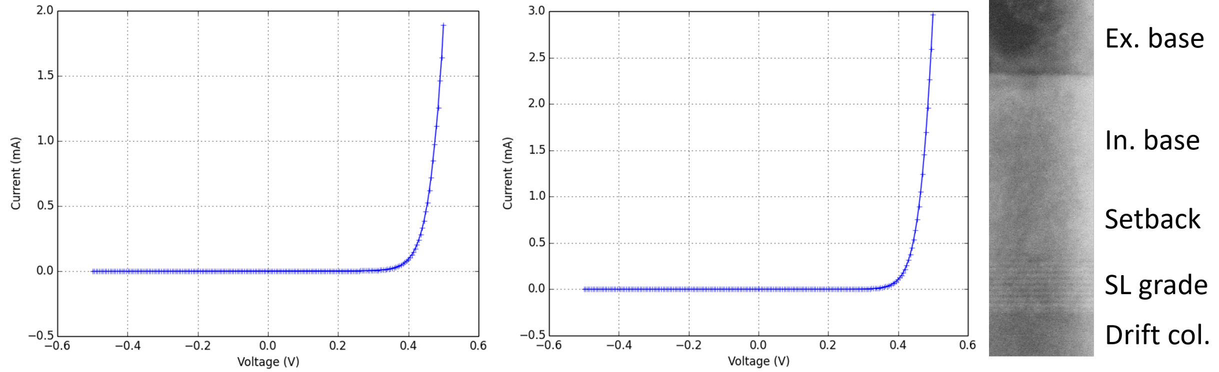


Figure 4.18: Base-collector test diode characteristics of RG67A (left), RG67B (center) with improved leakage current control and access resistance reduction, and good epitaxial quality throughout the extrinsic & intrinsic structure (right)

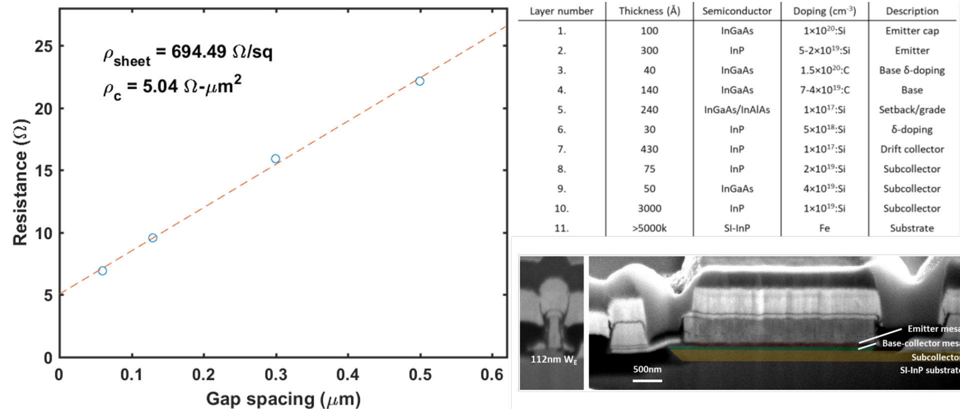
Subsequent base-collector test diodes show negligible reverse leakage, and steady improvement in access resistance as shown in Fig. 4.18 (left & center). RG67A & RG67B both utilizes an MOCVD in-situ re-activation anneal that yield clean regrowth interface with no defect propagation down into the intrinsic device structure. Fig. 4.18 (right) shows a cross-sectional TEM image of RG67B, where the superlattice grade is clearly visible, suggesting good crystal quality after the MOCVD regrowth and dopant reactivation process modules.

4.5 Ultra-low Contact Resistivity to p-type Semiconductors

Ultra-low contact resistivity to p-type InGaAs has been challenging to realize due to an almost universal 0.6 eV Schottky barrier height in the case of most metals. The most widely cited theory for such observation is the formation of the InAs phase (E_g = 0.7

eV) at the interface and its surface pinning in the conduction band [29, 30, 31]. More recently, the platinum group metals (Ru, Rh, Pd, Os, Ir, and Pt) have demonstrated the lowest contact resistivities to p-InGaAs below 1 Ω-μm^2 in TLM test structures, likely due to the formation of a stable (Pt,Pd,Ir,Ru)$_x$-InGaAs phase up to 350 °C, as well as the platinum group's ability to mechanically disperse surface organics and native oxides [32, 33, 34].

The use of Pt, Pd, and Ru in base contact metallization in p-InGaAs based full RF InP HBT process flow has seen less of an success, as contact resistivity $\sim$ 5 Ω-μm^2 is extracted from device R_{bb} measurements [35, 36]. The discrepancy between TLM and device contact resistivities certainly has to do with the added process steps and thermal budget in the HBT process flow. Attempts to identify the cause of higher measured base contact resistivity in RF HBT are detailed in this section.



Layer number	Thickness (Å)	Semiconductor	Doping (cm^{-3})	Description
1.	100	InGaAs	1×10^{20}:Si	Emitter cap
2.	300	InP	$5\text{-}2\times10^{19}$:Si	Emitter
3.	40	InGaAs	1.5×10^{20}:C	Base δ-doping
4.	140	InGaAs	$7\text{-}4\times10^{19}$:C	Base
5.	240	InGaAs/InAlAs	1×10^{17}:Si	Setback/grade
6.	30	InP	5×10^{18}:Si	δ-doping
7.	430	InP	1×10^{17}:Si	Drift collector
8.	75	InP	2×10^{19}:Si	Subcollector
9.	50	InGaAs	4×10^{19}:Si	Subcollector
10.	3000	InP	1×10^{19}:Si	Subcollector
11.	>5000k	SI-InP	Fe	Substrate

Figure 4.19: 5 Ω-μm^2 base metal contact resistivity measured in a 90 nm EBL defined HBT

Fig. 4.19 shows a 90 nm node conventional HBT without regrown extrinsic base, but with a more heavily doped p-InGaAs base layer (1.5 $\times10^{20}$ cm^{-3} for the top 40 Å base layer). Despite the higher dopant concentration and lower base sheet resistance ($\sim$ 700 Ω/□ vs. 850 Ω/□ in earlier epi designs), base metal contact resistivity is measured to be $\sim$ 5 Ω-μm^2. Base metallization is formed by resist lift-off of Pt/Ru/Pd/Au using

e-beam lithography and e-beam evaporation. Careful juxtaposition of process parameters between the 90 nm process run and those in previous group members' theses [37, 38] hints that e-beam lithography could lead to inconsistent base contact resistivity on a run-to-run basis. In addition, record low metal contact resistivities to p-InGaAs in TLM structures reported by previous group members are all fabricated using optical lithography [33, 39]. Therefore, speculation that EBL could degrade base contact resistivity warrants closer inspection. Deposition of organic contaminants on substrate surface in EBL systems due to resist outgassing under high vacuum and trace carbon dioxide under electron radiation has been reported [40, 41]. First-hand experience with the JEOL EBL system at UCSB suggests such concern is reasonable. Because the AE/BE alignment marks need to be replaced every PM cycle due to contamination build-up at the edges of the AE/BE marks (Fig. 4.20). Thus, later base metallization used in this thesis has been reverted back to optical lithography-based lift-offs to avoid EBL surface contamination.

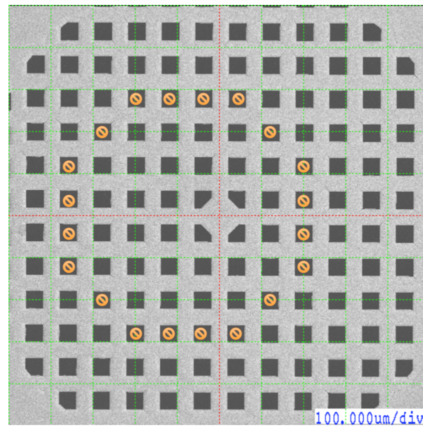


Figure 4.20: AE (Absorbed Electron) mark grid in the JEOL EBL system [42]

A second attempt at reducing base contact resistivity focuses on removing the indium content in the base material as indium-lacking $GaAs_xSb_{1-x}$ has favorable surface Fermi level pinning close to the valence band [43, 44]. Indeed, close to or less than 1 Ω-μm^2 contact resistivity to p-$GaAs_xSb_{1-x}$ has been reported using adequate surface clean

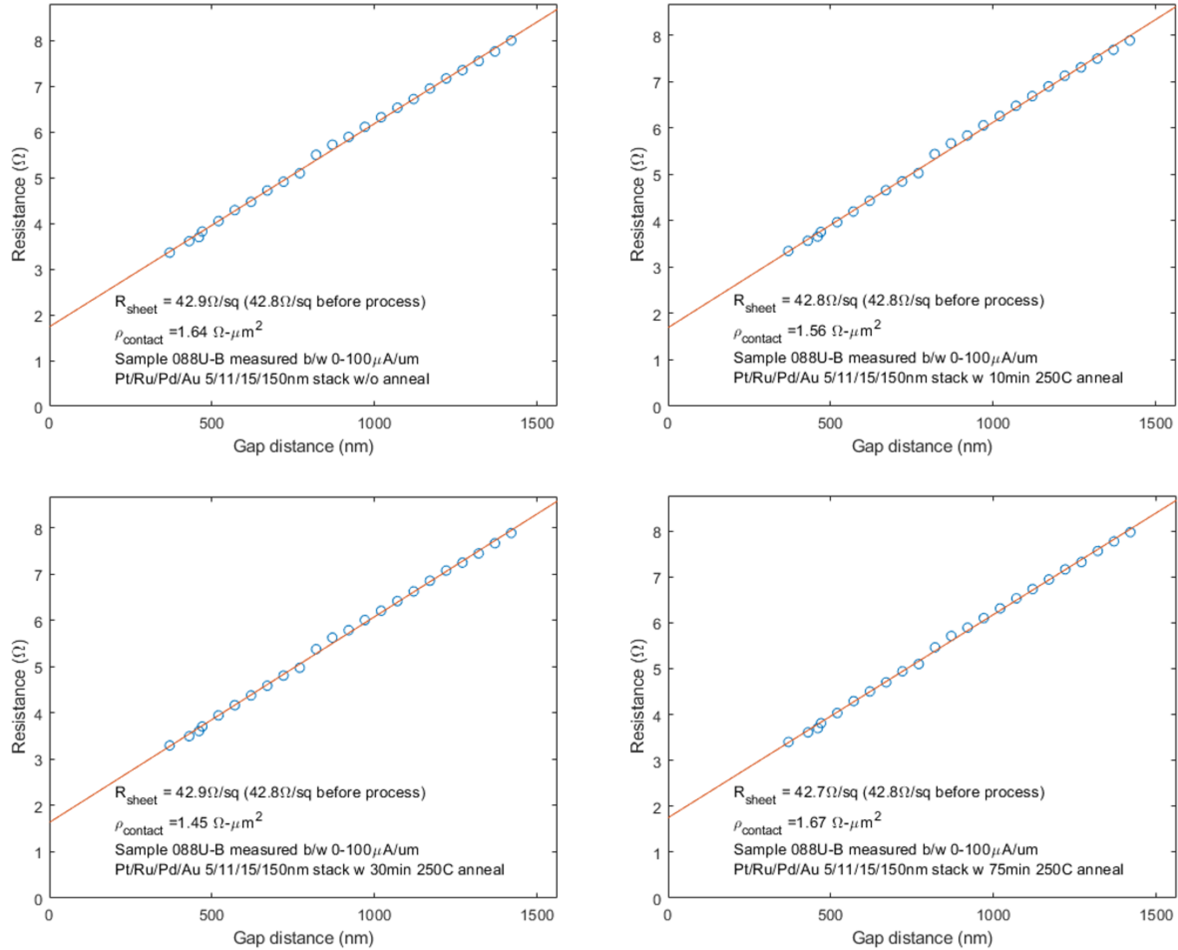


Figure 4.21: TLM results of Pt/Ru/Pd/Au contact to p-GaAsSb as deposited and annealed at 250 °C for up to 75 minutes

[45, 46, 47]. Results of in-house p-contact to GaAsSb are plotted in Fig. 4.21. Prior to e-beam evaporation, the GaAsSb sample is etched in 1:8 HCl:DI for 1 minute to remove native oxides. The base contact metal stack consists of 3 platinum group metal layers with 150 nm of top Au for low sheet resistance, and is lifted off in an optical lithography process as opposed to an EBL process. Isolation of the GaAsSb layer is done in a wet etch into the semi-insulating substrate. Low contact resistivity ∼1.5 Ω-μm^2 is maintained after annealing at 250 °C for 75 minutes. The study concludes that the use of platinum-group metals and optical over EBL lithography can potentially yield consistent

low contact resistivity to p-GaAsSb.

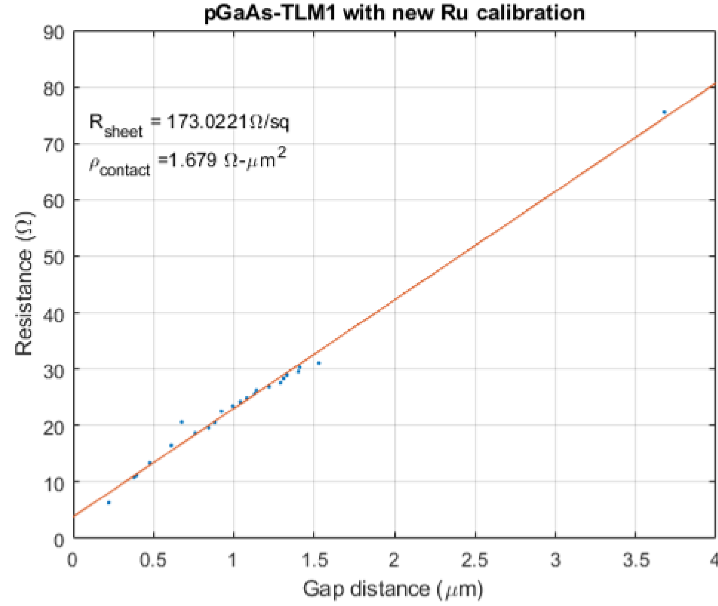


Figure 4.22: TLM results of Pt/Ru/Pd/Au contact to p-GaAs annealed at 250 °C for 75 minutes

The same e-beam evaporated Pt/Ru/Pd/Au base metallization and optical lithography processes are applied to in-house MOCVD p-GaAs with positive results. Fig. 4.22 shows a 1.7 Ω-μm^2 contact resistivity to p-GaAs annealed at 250 °C for 75 minutes. The TLM structures are fabricated on a dummy RF HBT epi substrate with TiW emitters formed and p-GaAs extrinsic base regrown on the InGaAs intrinsic base for process compatibility investigation. Consistently low contact resistivities < 2 Ω-μm^2 are measured when the HBT epi has seen the emitter process module as well as the 250 °C anneal required by the BCB backend process, suggesting the applicability of such metallization technology in full HBT device process flow.

4.6 Conclusions

In this chapter, process module development for the regrown extrinsic HBT is explained

in a logical order. First, the refractory emitter metal contact is formed by co-sputtering of Ti and W sources to enable a composition-specific vertical dry etched profile for consistent high-yield sub-100 nm emitter contact width. Next, growth and integration of the self-aligned MOCVD p-GaAs extrinsic base and dopant activation are discussed in terms of growth selectivity and preservation of the TiW emitter metal contact from oxidation. Fine tuning of the growth and anneal temperature profiles ensures integrity of the intrinsic base-collector junctions. So called DC large area HBT and its simplified process flow vs. the full RF counterpart are introduced. The emitter metal contacts in the DC devices are still patterned by EBL to a nominal 90 nm contact width, in line with future RF devices, for accurate extract of the base access resistance R_{bb}, while dimensions of the rest of the device structure are relaxed to μm-level resolution for ease of fabrication and fast turnaround. Some distinct electrical features of the DC devices are illustrated, including the apparent lack of thermal effects under high current injection conditions and the large common-emitter offset voltage due to the large parasitic base-collector diode area. Finally, low contact resistivities to p-type InP-related materials are pursued in process flows similar to that of InP HBT. Reconciliation between low contact resistivities measured by past group members in TLM test structures and higher values in final RF HBT devices could be potentially reached when e-beam lithography is excluded in favor of optical lithography because of e-beam induced deposition of surface contaminants. Low indium content semiconductors (GaAs, and GaAsSb) appear to have higher p-type active dopant concentrations, as well as favorable surface Fermi level pinning for consistently low contact resistivities $< 2\ \Omega$-μm^2 measured in house at UCSB.

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Chapter 5

Device Results

DC large area devices with scaled sub-100 nm emitter width, as well as integrated RF HBT results are presented in this chapter. Three batches of DC devices, RG62B, RG67A, and RG67D are discussed to illustrate major process integration milestones, including first demonstration of regrowth of MOCVD extrinsic base self-aligned to refractory emitter metal contact with RG62B, identification of intrinsic base dopant passivation with RG67A, and partial dopant re-activation of the intrinsic base with RG67D. Low < 2 Ω-μm^2 base contact resistivity with the regrown extrinsic base is measured in RG67D, paving the way for further RF process integration. After considerable recalibration of process parameters due to drifts accumulated over the COVID-19 lockdown, RF64RF-F shows first demonstration of RF process integration with the regrown extrinsic base process module. Low f_T and f_{max} of RF64RF-F can be attributed to a series of process failures that are examined in detail.

5.1 DC Large Area Device – RG62B

RG62B utilizes the DC large area device layout detailed in Section 4.3 with a narrowest nominal emitter contact width of 90 nm defined by EBL. The actual narrowest emitter contact width after emitter metal stack dry etch is around 180 nm. The difference between the nominal and actual emitter contact width is due to a stronger ICP loading effect during the emitter metal stack dry etch. It is suspected that chamber conditions in the Panasonic E646V ICP system has deteriorated over the course of this thesis. Subsequent device runs are able to restore sub-100 nm emitter feature sizes by including a 1 minute pump and purge cycle for every 30 s of TiW etch.

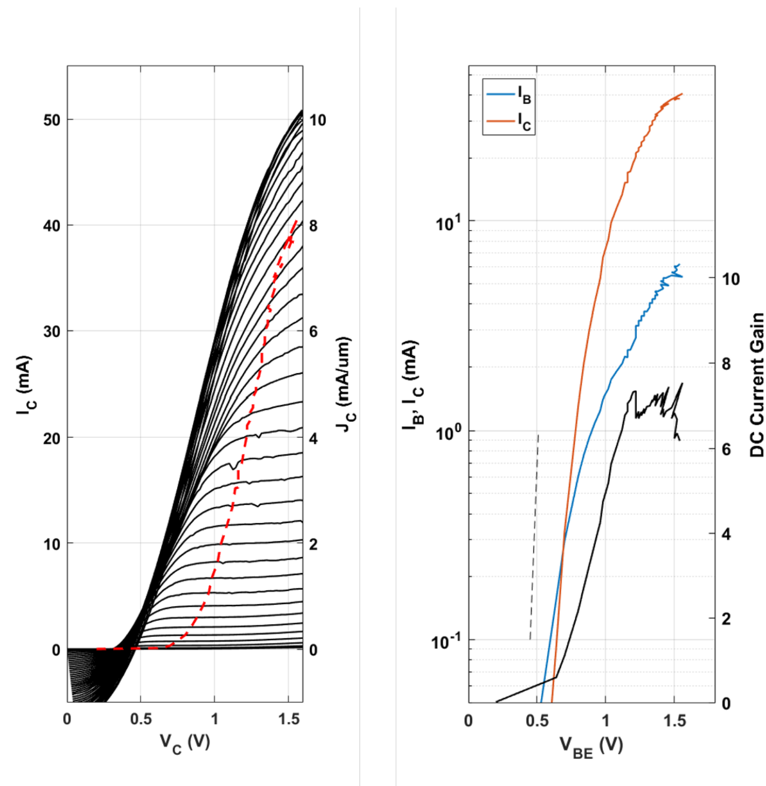

Figure 5.1: Common-emitter output characteristics of RG62B (left), and spurious Gummel characteristics of RG62B (right)

Device DC characteristics are plotted in Fig. 5.1. Common-emitter output character-

istics in Fig. 5.1 (left) show a few expected features of the large area devices discussed in Section 4.3. However, the still anomalously large ~ 0.5 V together with the >1 V knee voltage and graduate slope the saturation region suggest high emitter and base access resistances $R_{ex} + R_{bb}/\beta$. The high R_{bb} suspicion is confirmed by the high and inconsistent resistance values measured in base TLM test structures. Fig. 5.2 shows TLM resistance vs. gap distance on sample RG62B. The large variance in resistance values is coherent with the large absolute magnitude of the TLM resistances, suggesting a poor base contact.

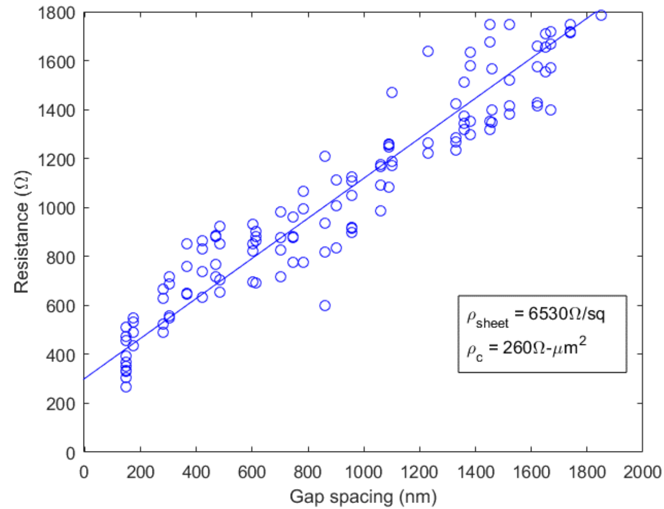

Figure 5.2: Pinched TLM results of RG62B with large absolute resistance values as well as a large variance

The causes of the high R_{ex} and R_{bb} are investigated with transmission electron microscopy of the device cross section. Fig. 5.3 reveals two obvious issues with the device. First, the top of the emitter metal stack is visibly denser than the rest of the emitter contact. Second,

Using the in-situ energy dispersive spectroscopy in the TEM system, a large presence of oxygen is detected in the top 90 nm of the emitter metal stack, suggesting oxidation of the TiW emitter metal. The origin of the oxygen species is found to be the rapid thermal

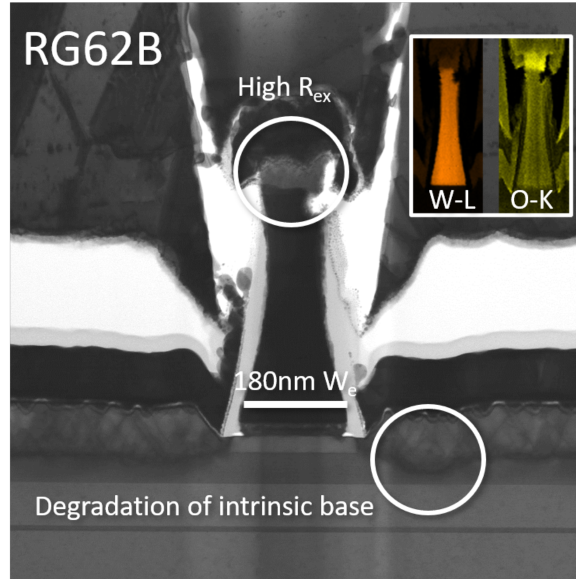

Figure 5.3: TEM cross section of RG62B showing possible causes of the high R_{ex} and R_{bb}

anneal system used for the dopant activation anneal. Though the RTA system at UCSB is nominally N_2 purged, an appreciable amount of trace oxygen can be detected within the chamber even after prolonged N_2 purging. Visible oxidation of initially reflective tungsten metal dummy samples placed in the RTA system confirms such postulate. Therefore, subsequent devices are in-situ annealed in the MOCVD system for dopant activation to avoid the oxidation problem (Section 4.2). Additional EDS mapping of the emitter metal-semiconductor region is performed to make sure no obvious secondary sources of high R_{ex} is present in the form of contact metal and emitter semiconductor interdiffusion (Fig. 5.4). The well confined arsenic signal to the emitter cap region, and clear demarcation between the indium and molybdenum regions serve as absence of proof that such secondary sources are present. However, a definitive proof of absence of other possibilities for high R_{ex} is hard to obtain with RG62B.

The explanation of high R_{bb} is initially believed to be degradation of the intrinsic HBT structure after the regrowth and anneal processes. As evident in Fig. 5.3, poten-

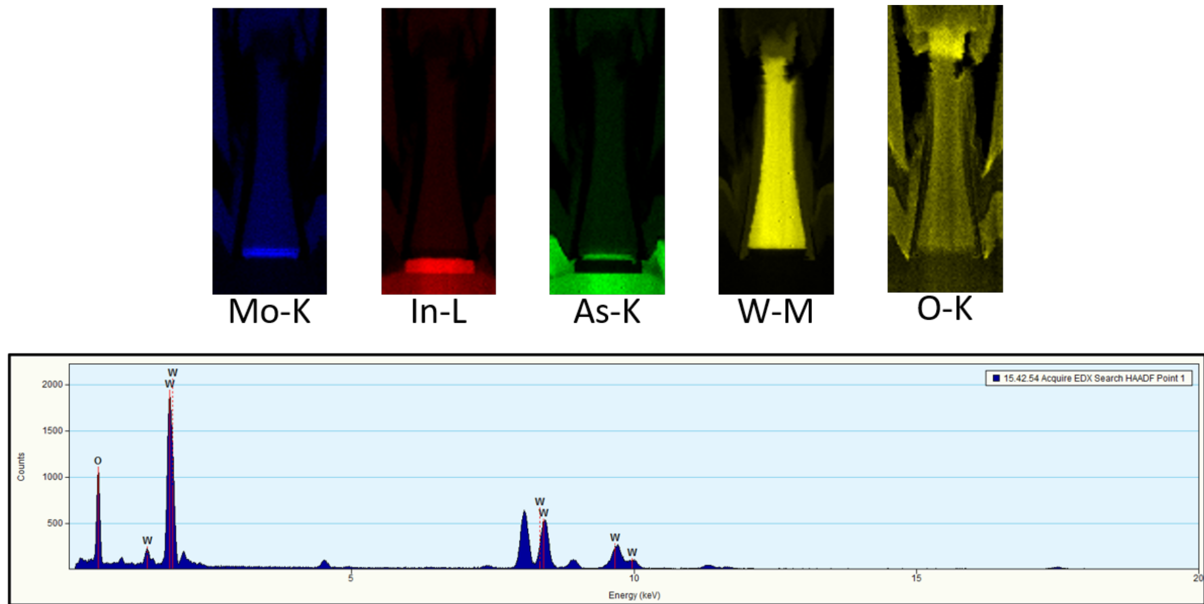

Figure 5.4: EDS mapping of the emitter contact metal and semiconductor region (top), and EDS quasi-quantitative analysis of the top of the emitter metal contact showing a high oxygen peak (bottom)

tial surface desorption of the intrinsic base and/or defect propagation from the regrown extrinsic base down to the intrinsic device structure are responsible for the uneven and diminished thickness of the intrinsic p-InGaAs base. Such postulate could explain the measured variance in TLM resistance in Fig. 5.2 as roughness of the regrowth interface is nonuniform. But the 6500 $\Omega/\Box$ high fitted sheet resistance over the large number of resistance measurements hints at the likeliness that the intact intrinsic base below the emitter-base junction is resistive, a region that is morphologically unchanged after the MOCVD regrowth. As it will become apparent in later sections, a great part of the high R_{bb} is due to passivation of the p-type carbon dopant in the intrinsic base during MOCVD regrowth. But the glaring unevenness in the extrinsic and intrinsic layers prompts a great amount of work to be done in trying to better control the growth morphology. Fig. 5.5 shows a comparison between atomic force microscopy scans of a dummy RG62B intrinsic base sample before the regrowth, and after the regrowth. Compared to subsequent device

runs with improved regrowth sequences, RG62B exhibits a rough surface after MOCVD regrowth.

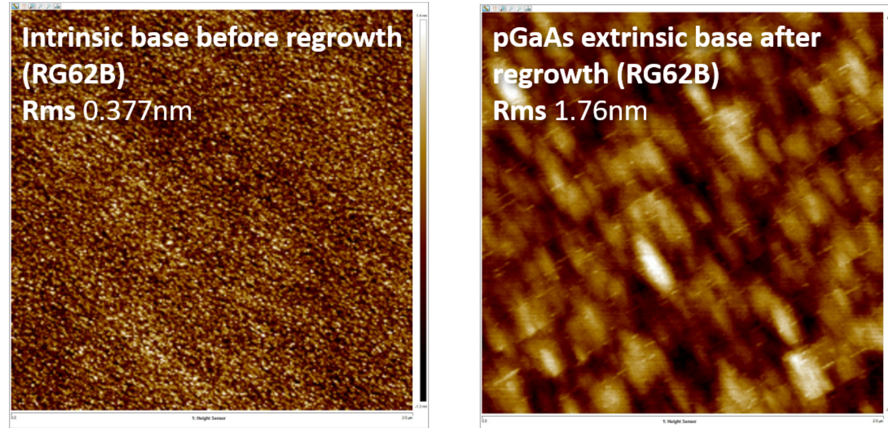

Figure 5.5: Surface morphology before the RG62B regrowth process (left), and after the RG62B regrowth process (right)

Despite the many issues discussed above in RG62B, the device run demonstrates feasibility of process integration between the MOCVD regrowth and the HBT process flow. Another important observation is that regrowth abutment to the intrinsic n-InP emitter semiconductor is realized as designed for low gap resistance R_{gap} (Fig. 5.6).

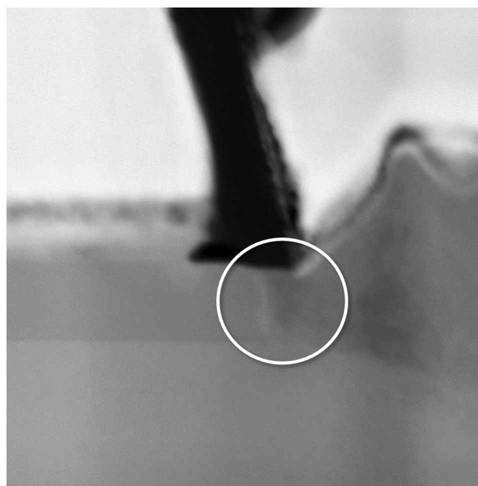

Figure 5.6: Abutment of regrown extrinsic base to intrinsic n-InP semiconductor observed in RG62B, suggesting possible reduction in R_{gap} as designed

5.2 DC Large Area Device – RG67A

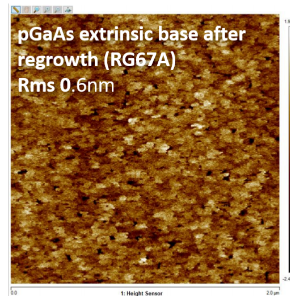

Figure 5.7: Improved surface morphology of regrown extrinsic base of device run RG67A

RG67A benefits from the extensive failure mode analysis of RG62B, and is regrown at a lower reactor temperature in the MOCVD for minimized surface desorption. Optimized temperature ramps and in-situ N_2 dopant activation anneal also leads to surface morphology closer to the intrinsic base with a rms surface rough less than 1 nm (Fig. 5.7).

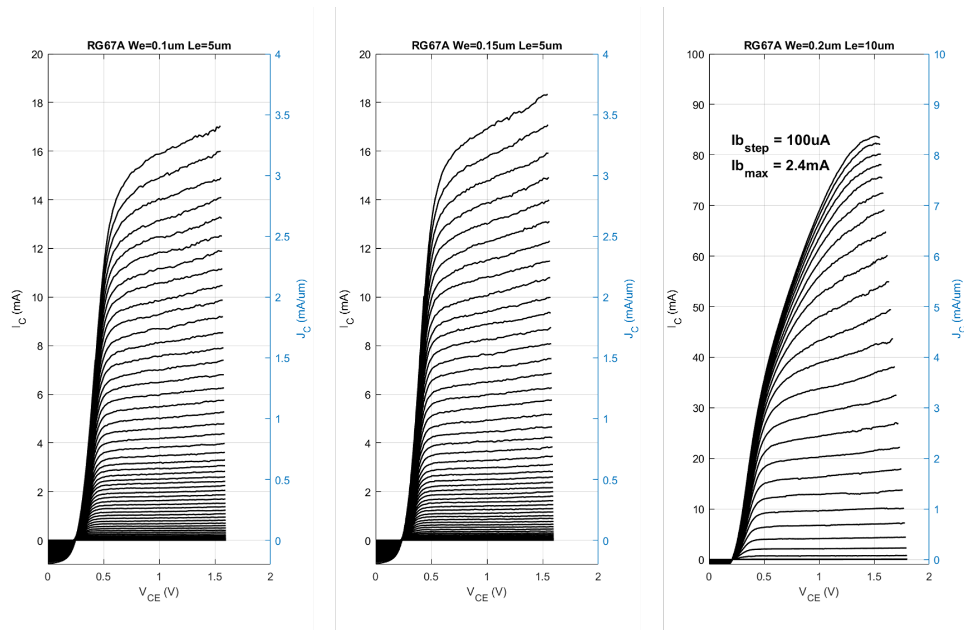

Figure 5.8: Common-emitter output characteristics of RG67A device run with 100 nm (left), 150 nm (center), and 200 nm emitter width (right)

Common-emitter output characteristics of three devices of 100 nm, 150 nm, and 200 nm emitter contact widths are shown in Fig. 5.8. The offset voltage in these devices is reduced from 0.5 V in RG62B to 0.25 V, whereas the knee voltage is around 0.5 V. No excessive R_{bb} or R_{ex} is immediately obvious from the output characteristics suggesting the improved regrowth parameters have a positive effect on device performance in accordance with postulates raised by failure analysis of RG62B.

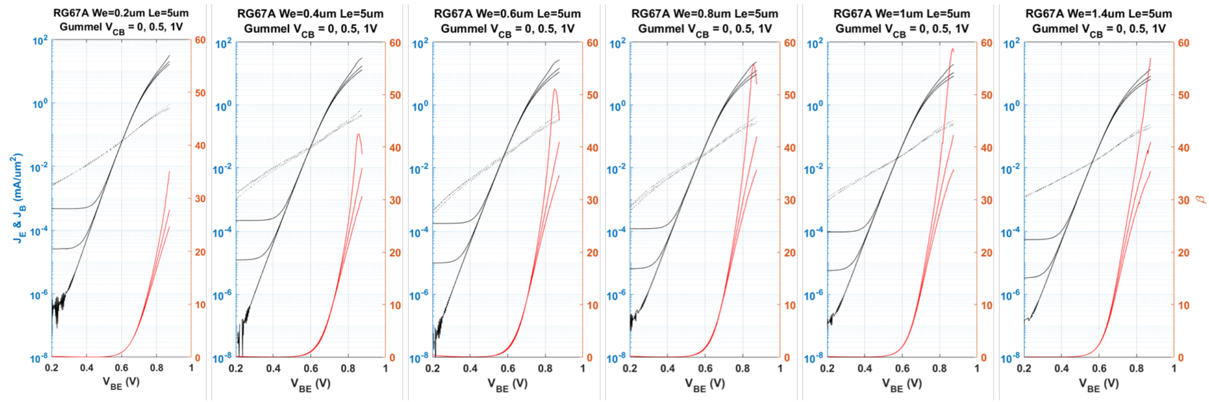

Figure 5.9: Gummel characteristics of devices of increasing emitter contact width in RG67A

Gummel characteristics of devices of increasing emitter contact width shown in Fig. 5.9 exhibit a monotonic positive correlation with device DC current gain β up to $\sim$60, and a dispersive β vs. V_{CE} relation. Both phenomena are indictive of lower than usual active dopant concentration in the intrinsic base. In the Auger recombination limited region where the intrinsic is degenerately doped, a β of 20 is calculated for the DHBT67 epi design. The significant deviation to $\beta = 60$ means the electron minority carrier life-time in the p-type intrinsic base is tripled, too much to be accounted for by other possible means. The dispersive β vs. V_{CE} relation is the classic manifestation of the Early effect, where an applied V_{CB} depletes the moderately doped base layer next to the drift collector, thereby decreasing thickness of the quasi-neutral base region and increasing apparent current gain [1]. To extract the active intrinsic base dopant concentration, $1/\beta$ vs. $1/W_e$ is plotted in

Fig. 5.10 to get a bulk intrinsic current gain $\beta_{bulk} > 80$ [2], corresponding to an active dopant concentration of 1-2 $\times$ 10^{19} cm^{-3}, about 85% less than the nominal value of the intrinsic base. The lower extracted dopant concentration is in agreement with the pinched TLM resistance measurement results shown in Fig. 5.11, where an intrinsic base sheet resistance of 4300 $\Omega/\Box$ is measured, with a $\rho_{c,total} = 1.9$ Ω-μm^2. Also in Fig. 5.11 is the results of unpinched TLM resistance measurements of the regrown extrinsic base, showing a 290 $\Omega/\Box$ extrinsic base sheet resistance and a metal contact resistivity of 0.9 Ω-μm^2. The contact resistivities indicate good regrowth interface and adequate surface clean of the extrinsic base prior to metallization, both crucial for low $R_{b,c}$. However, the high 4300 $\Omega/\Box$ intrinsic base sheet resistance significantly increases R_{gap} and R_{spread} by 5 times. Overall R_{bb} is extrapolated to be 46.6/33.4/9.6 Ω-μm $R_{spread}/R_{gap}/R_{b,c}$, or about 1.5 times higher than the 60 Ω-μm conventional baseline.

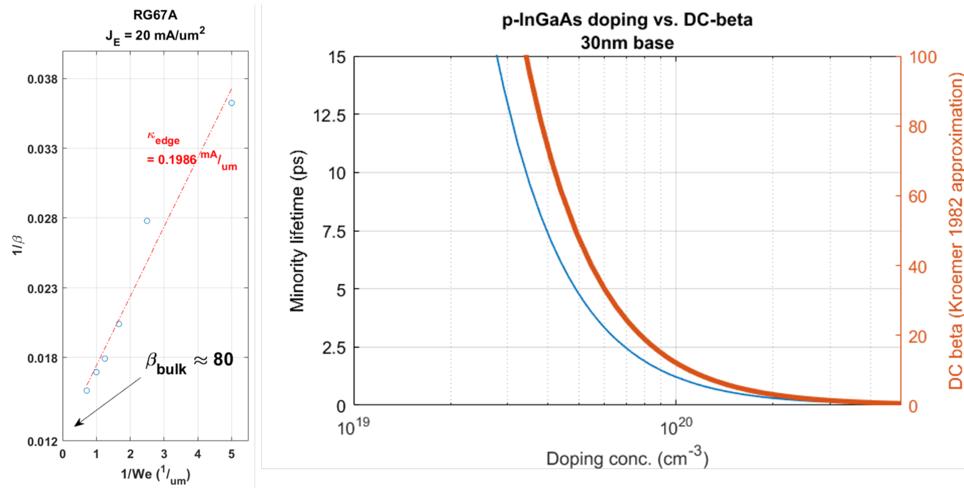

Figure 5.10: $1/\beta$ vs. $1/W_e$ of RG67A suggesting a $\beta_{bulk} = 80$ (left), and a corresponding 1-2 $\times$ 10^{19} cm^{-3} active dopant concentration in the intrinsic base (right)

To meet the 1/2 $\times$ goal in overall R_{bb}, or 30 Ω-μm, the increase in R_{gap} and R_{spread} caused by the higher intrinsic base sheet resistance after extrinsic base regrowth must be reversed. Possible causes of the apparent lower intrinsic base dopant concentration

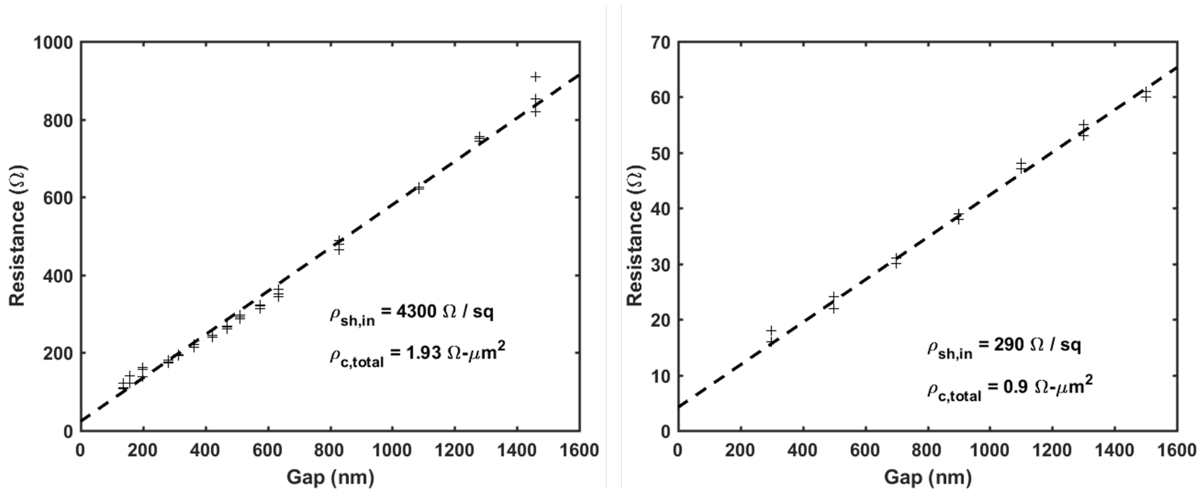

Figure 5.11: TLM resistance measurements of RG67A showing pinched intrinsic base sheet and contact resistances (left), and unpinched extrinsic base sheet and contact resistances (right)

include 1). n-type Si dopant in-diffusion from the emitter and drift collector to the intrinsic p-type base, 2). p-type C dopant out-diffusion from the intrinsic base to the emitter and drift collector, 3). carbon dopant self-compensation by movement to group-III lattice sites at elevated temperatures, and 4). hydrogen passivation of carbon dopants by cracked hydrogenated radicals during MOCVD regrowth. The in- and out-diffusions of Si and C dopants are quickly ruled out as the reason for the low apparent active dopant concentration in the intrinsic base both by theoretical calculations and experimental results. Assuming supply of the diffusing dopant species is infinite, dopant concentration as a function of time and position is given by the "thin-film" solution to the Fick's equation of diffusion [3]

$$c(x,t) = \frac{(N_{diff})^{2/3}}{\sqrt{4\pi Dt}} \exp(\frac{-x^2}{4Dt}) \tag{5.1}$$

where N_{diff} is the initial volumetric concentration of the diffusing dopants ($\sim 5 \times 10^{18}$ cm^{-3} for Si, and $\sim 1.5 \times 10^{20}$ cm^{-3} for C), D is the diffusivity of the diffusing species

($< 10^{17}$ cm^2/s for Si at 600 °C, and $< 10^{14}$ cm^2/s for C at 600 °C [4, 5]). Less than 2% of the C dopants in the intrinsic base would be diffuse out or be compensated by the Si dopants from the emitter and collector layers even after 1 hour at 600 °C. The regrowth and anneal in this thesis is less than 30 minutes in duration and performed at < 500 °C. Experimentally, it is found that with the emitter layer completely removed, a 60 % lower active dopant concentration in the intrinsic base is measured after exposure to group-V metalorganic precursors only at regrowth temperature, and can be re-activated to > 80 % its original value upon the in-situ N_2 anneal. Hydrogen passivation by hydrogenating cracked group-V metalorganic species is, therefore, deemed responsible for passivation of the carbon dopants in the intrinsic base. The inability to re-activate the carbon dopants beneath the InP/InGaAs emitter-base diode is suspected to be electric field induced retardation of hydrogen out-diffusion, and has been reported in various III-V material systems [6, 7, 8, 9, 10, 11, 12]. Subsequent device runs include an in-situ N_2 anneal of a longer duration (450 s) in the MOCVD system to combat the persistent hydrogen passivation.

5.3 DC Large Area Device – RG67D

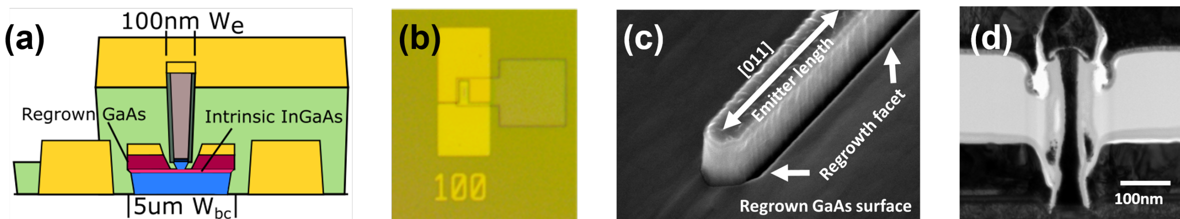

Figure 5.12: Schematic cross section of an 100 nm emitter width DC device in RG67D (a), top view of an nominal 100 nm emitter width HBT (b), tilted SEM view of the regrown p-GaAs extrinsic base surrounding the emitter metal stack with (111) and (113) crystal facets (c), and TEM cross section of a nominal 100 nm emitter width device (d)

RG67D shown in Fig. 5.12 includes an optimized loading effect free vertical dry

etched $Ti_{4wt\%}W$ emitter metal contact stack that has an emitter contact width of ∼80 nm. Excellent crystal quality of the regrown extrinsic base is visible in the (111) and (113) crystal facets of along the emitter strip length. The favorable (111) and (113) crystal facets also help prevent shorts between the emitter and base metal contacts, as the n-InP emitter semiconductor is fully encapsulated by the abutment of the extrinsic base, and the emitter TiW metal contact is protected by the SiN sidewall. A thick 200 nm base metal stack can be, therefore, deposited right against the SiN sidewall as illustrated in Fig. 5.13 without the fear of emitter-base shorts to minimize metal sheet resistance as well as gap resistance R_{gap}. The gap distance in RG67D is around 15 nm, set by the SiN sidewall thickness, 1/2 of that in the conventional HBT.

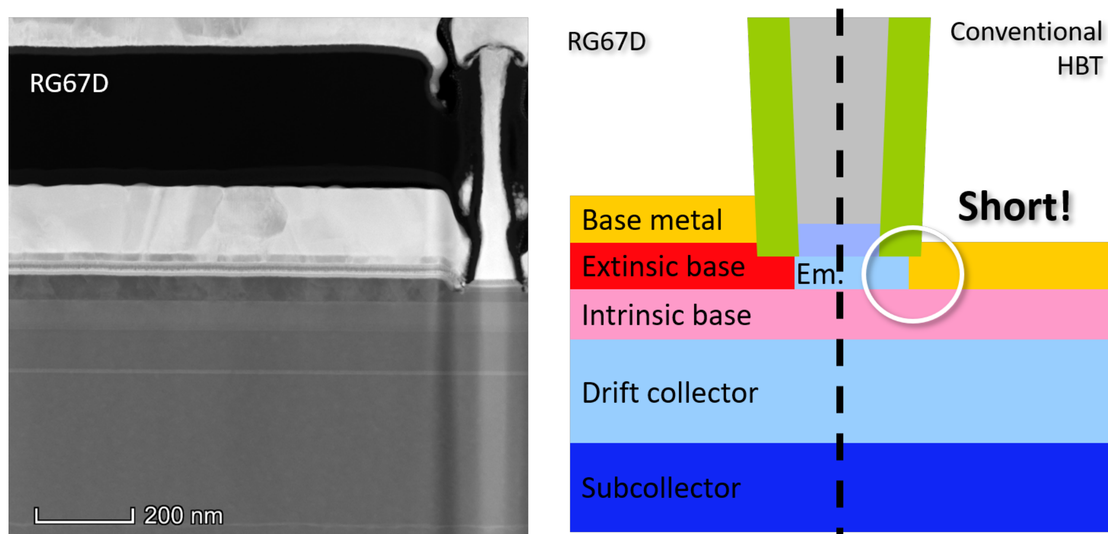

Figure 5.13: TEM cross sectional view of an 80 nm (100 nm nominal) device in RG67D showing excellent regrown extrinsic base crystal quality as well as intrinsic device epi structure (left), and prevention of base-emitter junction shorts by abutment of extrinsic base regrowth (right)

The base metallization is Pt/Ru/Pd/Au 7.5/16/24/150 nm measured by TEM[i]. An extremely low contact resistivity ∼ 0.4 Ω-μm^2 to the p-GaAs extrinsic base is extracted,

[i]Or nominal 5/11/16.5/100 nm deposition in E-beam evaporator #1, as tooling factors are off by 50 % in the specific system.

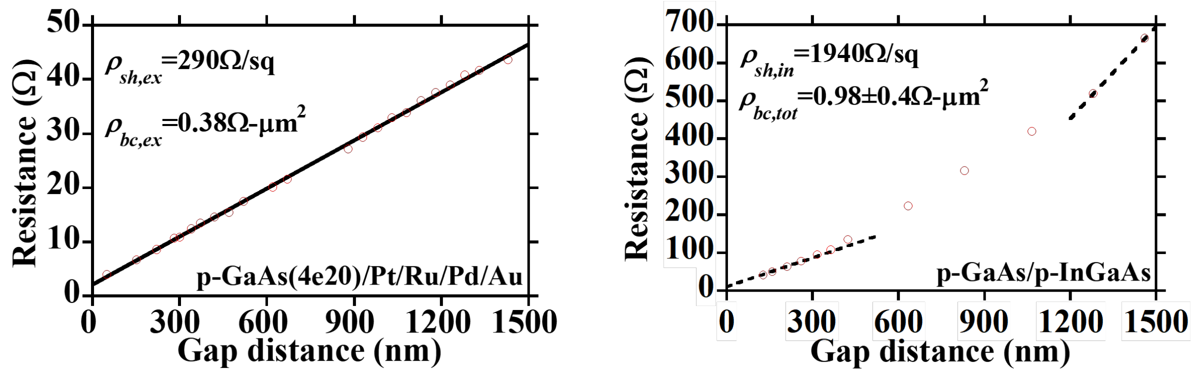

Figure 5.14: TLM resistance measurements of RG67D showing a low base metallization resistance (left), and a non-linear TLM resistance vs. gap distance relation indictive of incomplete intrinsic base dopant reactivation (right)

together with a 290 Ω-μm^2 extrinsic base sheet resistance. Thanks to the extended intrinsic base dopant re-activation anneal, the intrinsic base is partially re-activated. Fig. 5.14 (right) illustrates a non-linear TLM resistance vs. gap distance relation, suggesting the degree of dopant reactivation is inversely proportional to the width of the emitter contact width. The observation is consistent with findings in the literature, where the built-in potential of the emitter-base junction would suppress lateral diffusion of hydrogen outgassing [7, 8, 13]. Nevertheless, the extracted R_{bb} for a 100 nm emitter width device in RG67D is below the 60 Ω-μm^2 conventional baseline, at 20.6/12.1/9.4 Ω-μm $R_{spread}/R_{gap}/R_{b,c}$ for an overall R_{bb} of 42.1 Ω-μm. The bulk of R_{bb} reduction is attributed to the low $R_{b,c}$, whereas R_{gap} and R_{spread} remain high due to the lower active dopant concentration in the intrinsic base. The active dopant concentration in the intrinsic base is around 3-4 $\times$ 10^{19} cm^{-3}, or about half of the original dopant concentration before regrowth, fitted for devices with an emitter contact width less than 300 nm seen by the dashed trendline in Fig. 5.14 (right). Because of the fact that hydrogen outgassing is easier for devices with narrower emitter contact width, it is likely that the narrowest 80 nm (100 nm nominal) devices would have a R_{bb} lower than the 42.1 Ω-μm extraction.

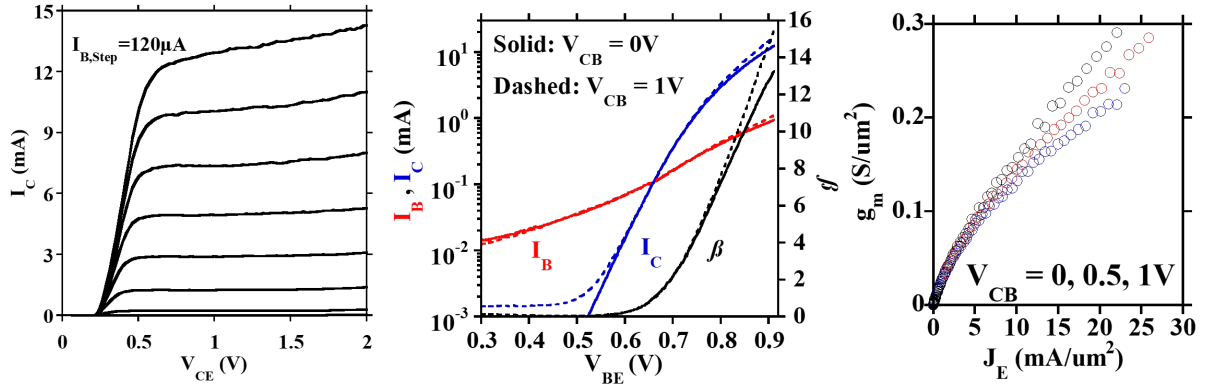

Figure 5.15: Common-emitter output characteristics of an 80 nm emitter width device in RG67D (left), Gummel characteristics at different V_{CB} (center), and transconductance g_m vs. J_E (right)

Therefore, process integration of RG67D is considered a success that warrants further RF adaptation.

Common-emitter output and Gummel characteristics of an 80 nm (100 nm nominal) emitter contact width device are shown in Fig. 5.15. Compared to RG67A, RG67D suffers less from the Early effect, and DC current gain at $V_{CB} = 0, 1$ V only differs by a maximum of 2 parts per 15. Fig. 5.15 (right) shows g_m as a function of emitter current density J_E under different V_{CB} bias conditions. Again, limited dispersion is observed. At $V_{CB} = 0$ V, g_m vs. J_E is consistent with values found in [14], suggesting a low R_{ex} and an intact emitter metal contact after the extrinsic base regrowth. Overall, the extracted device parameters of RG67D, together with its 80 nm emitter contact width, are projected to have an f_{max} in excess of 1.5 THz[ii] for an overall 35 % improvement in f_{max}.

[ii] Assuming negligible improvement in f_T, and ~ 80 % C_{in} & ~ 68 % R_{bb}

5.4 RF Process Integration – RG64RF-F

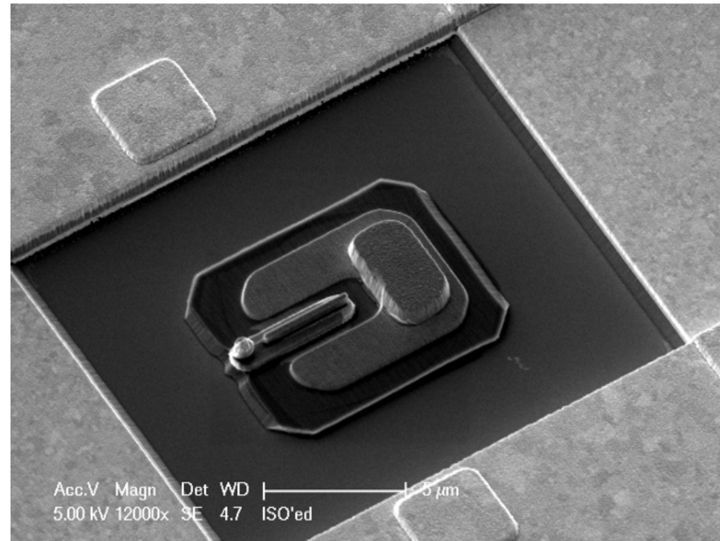

Figure 5.16: SEM image of a RG64RF-F HBT in TRL environment before BCB ILD planarization

Full RF integration is eventually realized in batch RG64RF-F after considerable recalibration of process parameters due to drifts accumulated over the COVID-19 lockdown. Fig. 5.16 shows a nominal 100 nm emitter width RF HBT embedded in the TRL calibration environment before BCB ILD planarization. A few noticeable differences in layout over usually RF devices include the relaxed base-collector and mesa isolation lithographic feature sizes, and misalignment of the collector contact metal in the direction away from the base post. These changes are made either intentionally, or unintentionally because of a decline in the conditions of the UV stepper system. Also, very poor yield is observed for RG64RF-F as a result of a significant drift in the undercut behavior of the $Ti_{4wt\%}W$ emitter metal stack towards the end of this thesis. Exact cause of the failure mode remains elusive. But it is most likely because of local temperature hot spots on wafer during the ICP dry etch. The chiller circuit of the ICP system has been replaced after the process campaign. As a result, only transistors with an emitter contact width

greater than 300 nm are yielded.

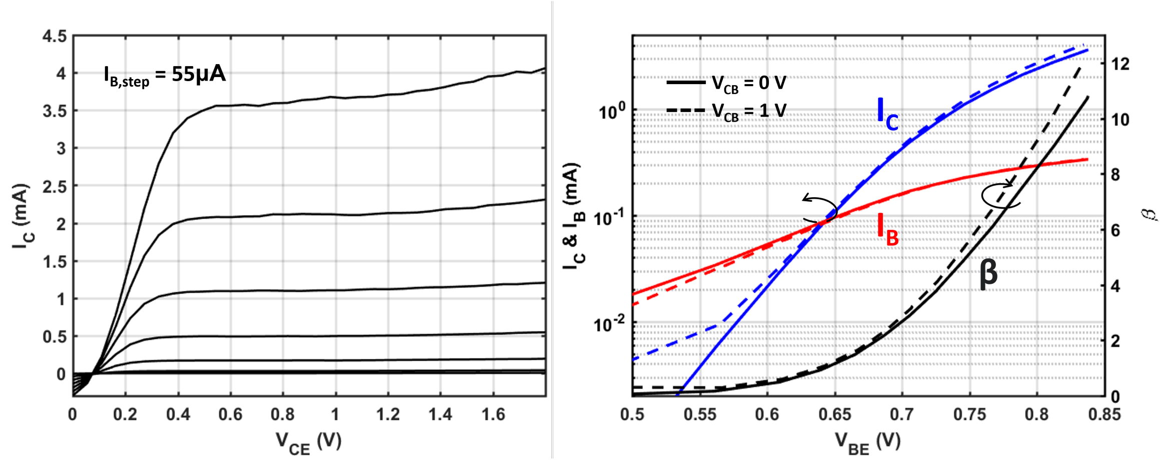

Figure 5.17: Common-emitter output and Gummel characteristics of a 300 nm emitter contact width RF HBT in RG64RF-F

Fig. 5.17 shows the DC common-emitter output and Gummel characteristics of a 300 nm emitter contact width 3 μm emitter finger length device in RG64RF-F. Compared to previous DC devices with a large parasitic base-collector pad area, the RF device shows a lower common-emitter offset voltage as expected owing to less diffusion current from the smaller base-collector junction. DC current gain β sees an appreciable dispersion as a function of V_{CB}, suggesting an *inadequate* reactivation of the intrinsic base.

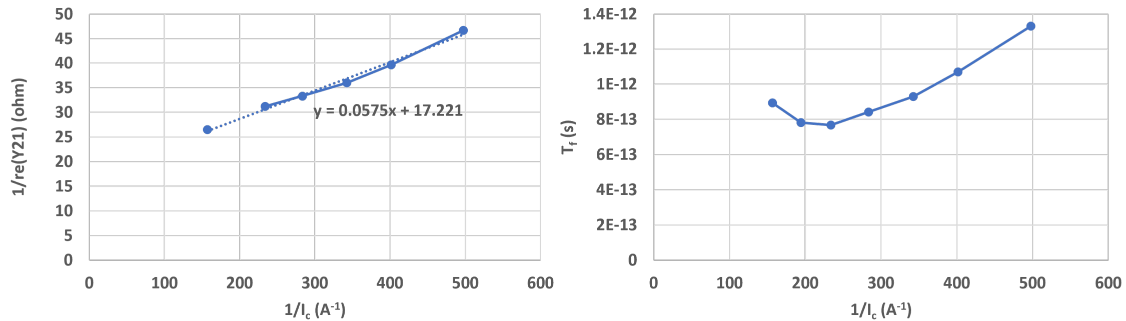

Figure 5.18: Low frequency extraction of $R_{ex} + R_{bb}/\beta$ with limited accuracy (left) due to strong collector Kirk and/or emitter starvation effects (right)

Initial low frequency small-signal parameter extraction of $R_{ex} + R_{bb}/\beta$ and τ_f shows a

low collector Kirk and/or emitter starvation current densities at around $J_c = 2$ mA/μm^2 or $J_e = 6$ mA/μm^2 as shown in Fig. 5.18. Such low current densities prohibit accurate extraction of $R_{ex} + R_{bb}/\beta$, and more importantly device high frequency performance.

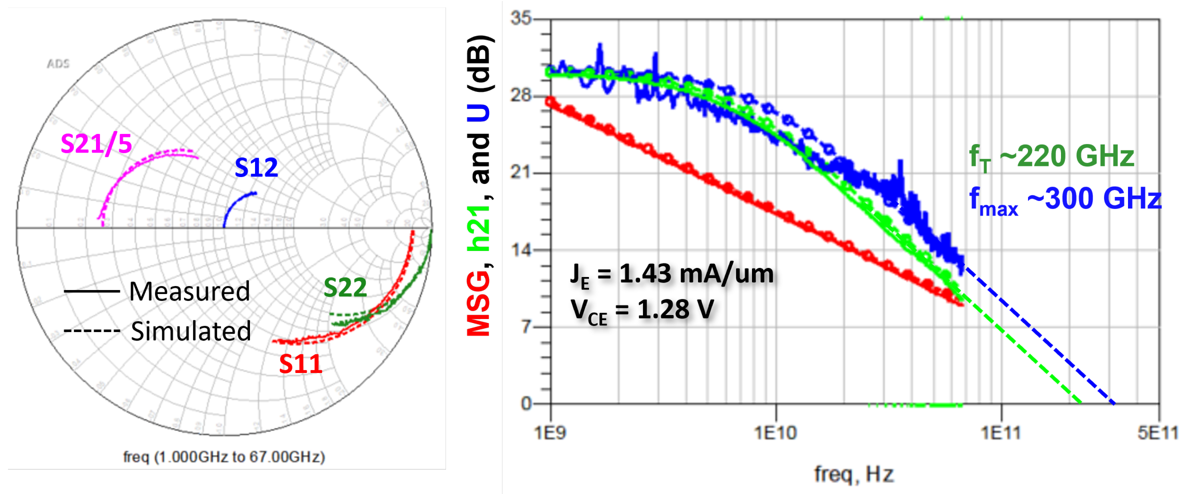

Figure 5.19: Measured small-signal S-parameters of a 0.3 $\times$ 3 μm^2 device in RG64RF-F (left), and h_{21}, MSG, and U of the same device with 220/300 GHz f_T/f_{max} (right)

At a low 1.43 mA/μm emitter current density, or about 1.6 mA/μm less than the usual optimal f_T current density of an InP HBT, and $V_{CE} = 1.28$ V, the 0.3 $\times$ 3 μm^2 device exhibits a peak f_T/f_{max} of 220/300 GHz as shown in Fig. 5.19. f_{max} quickly declines beyond such bias conditions. Device small-signal modeling with a hybrid-π model is performed using the standard Y-parameter fitting procedure found in literature [15, 16]. Excellent agreement between the fitted small-signal equivalent model and measured Y-parameters is displayed in Fig. 5.20.

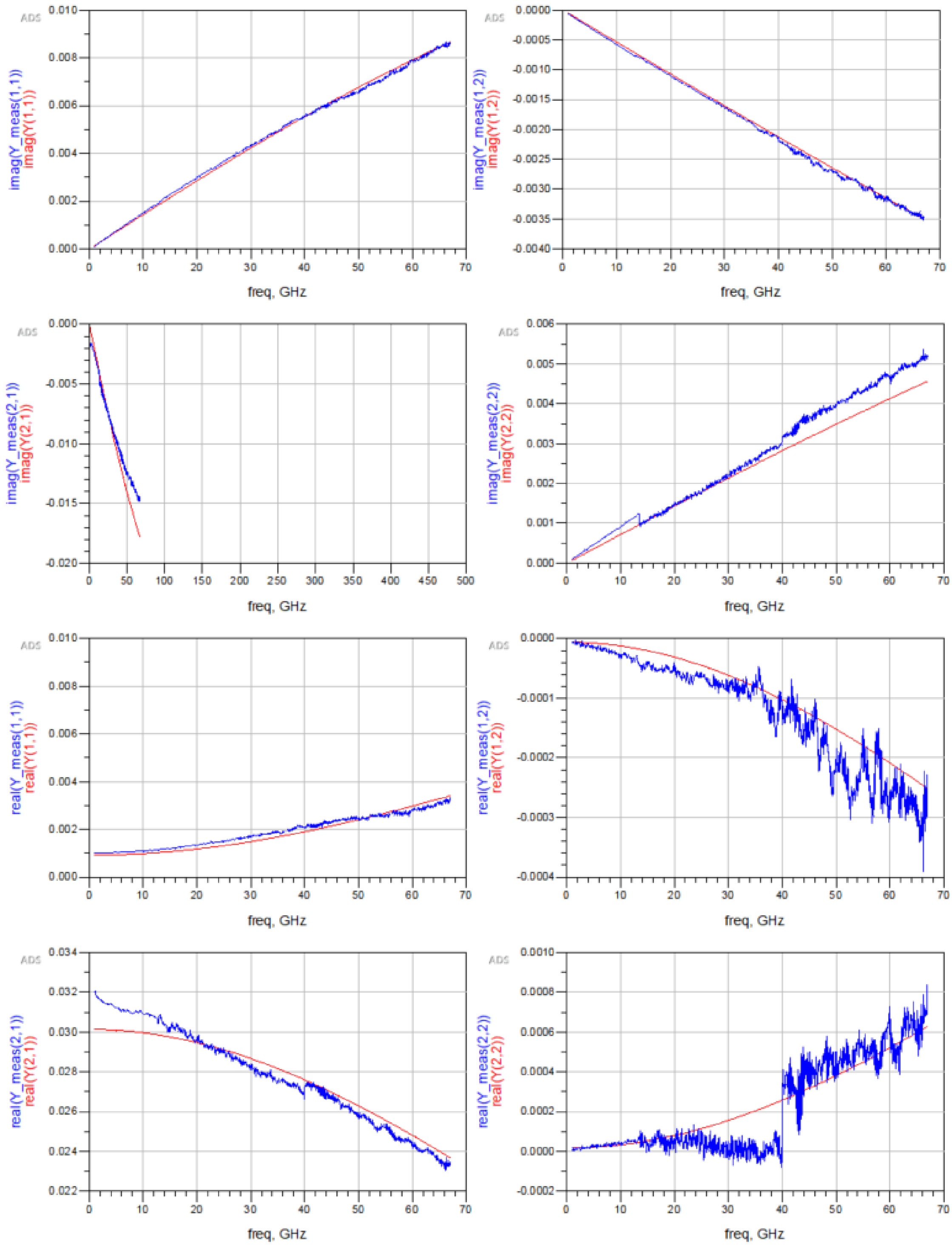

Figure 5.20: Y-parameter fitting between the measured $0.3 \times 3\ \mu\text{m}^2$ device (blue) and the equivalent small-signal model (red)

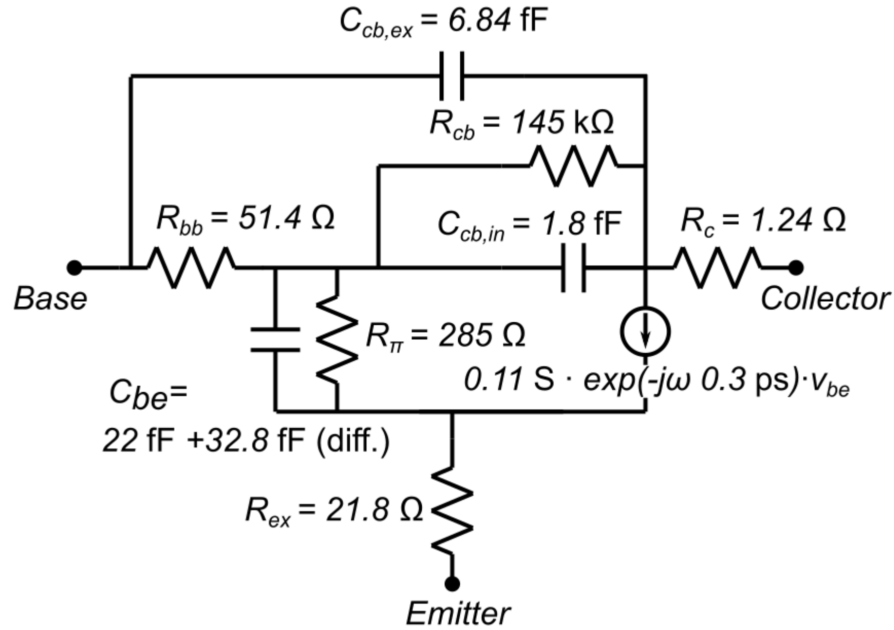

Figure 5.21: A hybrid-π small-signal equivalent circuit for the HBT at peak f_{max}

A number of issues are present in RG64RF-F in addition to the 300 nm wide emitter contact width. First, a high current gain $h_{21} \sim 30$ is observed at low frequency, corresponding to a high $R_\pi \sim \beta/g_m$ seen in Fig. 5.21. The intrinsic base sheet resistance is found to be almost identical to that in RG62A at 4350 $\Omega/\Box$. Both observations lead to the suspicion that the intrinsic base is not activated. Using sheet resistances $\rho_{s,in}/\rho_{s,ex}$ of 4350/290 $\Omega/\Box$, contact resistivities $\rho_{c,ss}/\rho_{c,ms}$ of 0.5/1 Ω-μm^2, and a gap distance W_{gap} of 15 nm, calculations show that the base access resistance is dominated by the high intrinsic sheet resistance. Theoretical $R_{spread}/R_{gap}/R_{b,c}$ are 36.2/6.1/7.1 Ω, for a total of 49.4 Ω that is within $\pm$ 4 % of the value extracted from high frequency measurements (Fig. 5.21). Therefore, it is very likely that the intrinsic base is, indeed, not activated. The MOCVD system suffered a process chamber pump failure the day before the regrowth of RG64RF-F, and N_2 gas line shutdown two days prior. It is possible that the

regrowth sequence is botched.[iii] Second, the emitter access resistance R_{ex} is twice of the usual value, suggesting either again oxidation of the TiW emitter metal stack took place at some point along the process flow, or other previously unidentified failure modes of the emitter process module are at play. With limited access to the TEM facility and shift in lab personnel during the pandemic, it is hard to pinpoint the exact cause of the high R_{ex}. Finally, the low optimal f_{max} bias conditions could be potentially explained by the high R_{ex} and R_{bb}, and associated RC time delays. Scaling the bias dependent parameters in the small-signal model – C_{diff}, R_{π}, and g_m – by an appropriate amount to the normal 3 mA/μm emitter current density only increases f_T by $\sim$ 50 GHz, and f_{max} by $\sim$ 100 GHz. Clearly, device performance is severely limited by the resistive components.

5.5 Conclusions

Three generations of large area DC HBT with steadily improved device characteristics are presented in this chapter. The latest DC device run, RG67D, offers a base access resistance R_{bb} $\sim$50 % less than the conventional baseline (42.1 Ω-μm vs. 60 Ω-μm). The bulk of R_{bb} reduction is a result of the lower base metal contact resistance $R_{b,c}$, and gap resistance R_{gap} provided by the low extrinsic base sheet resistance $\rho_{s,ex}$, and optimized low resistivity base metallization to p-GaAs. The low $R_{b,c}/R_{gap}$ values are offset to some degree by an increase in the spreading resistance R_{spread} due to the incomplete re-activation of the intrinsic base, and the accompanying higher intrinsic base sheet resistance $\rho_{s,in}$. Therefore, overall R_{bb} improvement obtained in the DC devices is less than the 1:2 scaling simulated with a fully activated intrinsic base discussed in previous chapters. The improvement is, however, significant enough for proof-of-concept RF device integration. Multiple runs of RF device integration are thwarted by the logistical

[iii]Though sensibly not the most ideal day for extrinsic base regrowth, logistically it was the only option because of limited access to the MOCVD lab during the pandemic, see pp. 183.

difficulties encountered towards the end of the thesis. Finally, one batch of RF devices, RG64RF-F, is completed with some issues, including a high emitter access resistance R_{ex}, and a high base access resistance R_{bb} that could have to do with the untimely MOCVD regrowth. Potential mechanisms of the failure modes are discussed.

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Chapter 6

Conclusions

6.1 Summary

MOCVD p-GaAs regrown extrinsic base self-aligned to dry etched sub-100 nm refractory TiW emitter metal stack for reduced base access resistance R_{bb} is demonstrated in DC large area InP HBT. Major process development includes a high-yield cosputtered vertical sidewall profile $Ti_{4wt\%}W$ emitter metal contact technology (Section 4.1), and low temperature (490 °C) MOCVD growth of heavily carbon doped p-GaAs (Section 4.2). A 42.1 Ω-μm R_{bb} extracted from a DC large area device with an ∼80 nm emitter contact width W_e and 15 nm emitter sidewall thickness T_{SiN} are projected to offer an improved f_{max} = 1.6 THz (Section 5.3), or 1.5 times over the state-of-the-art 130 nm InP HBT. Proof-of-concept RF process integration establishes the feasibility of the technology with a 300 nm W_e device exhibiting a 300 GHz f_{max} (Section 5.4). Issues with the first RF devices are discussed and are expected to be solved in future process runs. Theoretical analysis of the regrown extrinsic base process module reveals that conventional lithographic scaling of InP HBT is limited to an $f_{max} \approx 1.3$ THz even at the 32 nm technology node (Section 3.1) due to non-scaling of emitter SiN sidewall thickness,

plateauing base metallization technology, and requirements for sub-10 nm lithographic overlay accuracy, etc. Moreover, diminishing maximum saturated output power limited by loadline matching questions the applicability of lithographically scaled InP HBT beyond the 130 nm node for power amplifiers below 300 GHz (Section 1.4). Therefore, the insertion of the regrown extrinsic base process module at the 130 nm technology node with a 100 nm thick drift collector appears to be a good solution that both retains the favorable high saturated output power as well as increases attainable power gain under optimal power matching conditions (Section 3.3).

6.2 Future Work

In-house RF process integration of the regrown extrinsic base process module still needs many iterations of device optimization before the promised 1.6 THz f_{max} is achieved with the 130 nm node intrinsic epi design. It remains to be seen whether scaling to the 60 nm and eventually 30 nm technology nodes are beneficial to power amplifier designs at 100-300 GHz due to the issues discussed above. Therefore, more architectural innovations instead of conventional scaling are desired to extend the high-frequency capabilities of InP HBT, such as the low thermal resistivity transferred-substrate technology for higher current densities, and the collector-up HBT concept envisioned by Professor Herbert Kroemer 40 years ago that minimizes the base-collector capacitance [1]. Unlike GaN HEMT, which leverages the mature LED and increasingly power transistor markets, InP HBT research faces challenges in terms of economy of scale, and a lack of commercial applications in the civilian space.

A few ideas related to the regrown extrinsic base process module in InP HBT are worth exploring in the future.

First, the intrinsic base layer studied extensively in this thesis is p-InGaAs, which can

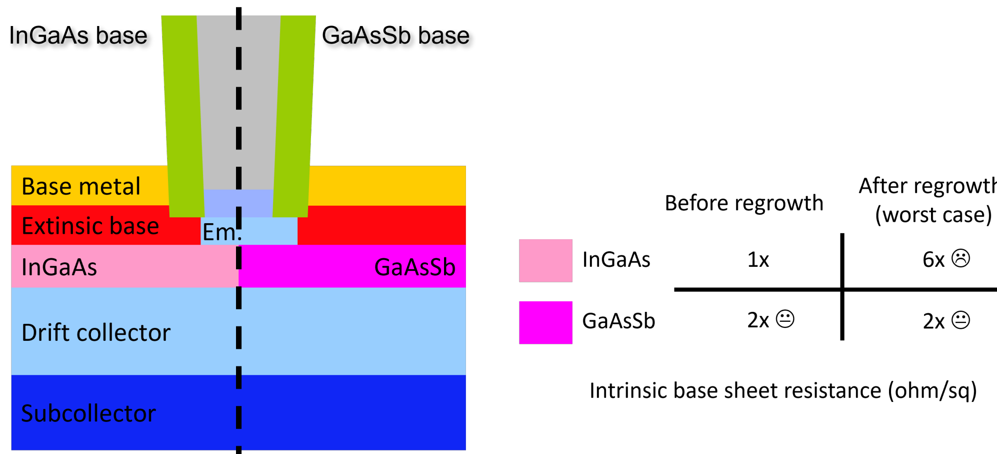

Figure 6.1: Comparison between InGaAs and GaAsSb intrinsic base HBT

be replaced by the other widely adopted intrinsic base material – p-GaAsSb. Compared to p-InGaAs, p-GaAsSb's type-II conduction band alignment to the n-InP drift collector supposedly simplifies the intrinsic epitaxial design by avoiding the need for a superlattice grade at the base-collector interface[i] [2]. The strength p-GaAsSb possesses, in the context of the regrown extrinsic base, is its lack of indium, and immunity to hydrogen passivation that plagues the p-InGaAs HBT. The tradeoff is p-GaAsSb has a higher sheet resistance to begin with compared to p-InGaAs. At the same doping level, in-house and reported sheet resistance of p-GaAsSb is twice that of p-InGaAs [3]. But given R_{gap} and $R_{b,c}$ can be minimized by the regrown extrinsic base process module, p-GaAsSb's higher sheet resistance can be offset for a low overall base access resistance R_{bb} without including a tricky hydrogen out-diffusion or dopant reactivation anneal in the process flow. A comparison between the two intrinsic base materials are shown in Fig. 6.1.

Second, a completely new intrinsic base material of interest is strained p-GaAs on InP. p-GaAs is ~ 5 times more conductive than p-InGaAs at a given doping concentration [4], meaning only 4 nm of p-GaAs is needed to give a 750 $\Omega/\Box$ sheet resistance required for the 130 nm technology node. When strained to InP, p-GaAs has a type-I conduction

[i] Though the growth of superlattice grade in p-InGaAs InP HBT has been already a solved issue.

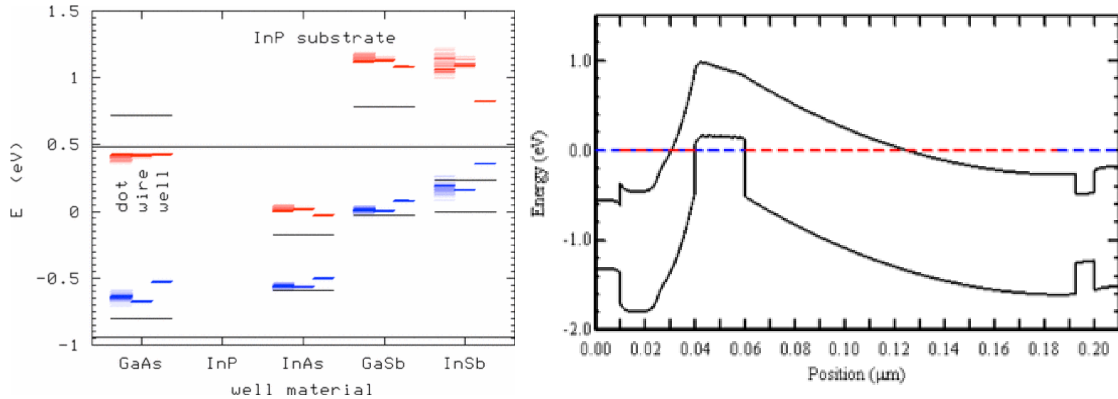

Figure 6.2: Calculated band alignment of common III-V semiconductors strained to InP (left), Reprint with Permission © APS 2005 [ii], and simulated intrinsic band alignment of the proposed InP/GaAs/InP HBT (right)

band alignment similiar to that of p-InGaAs as seen in Fig. 6.2 (left) [5]. Thus, the base-collector superlattice grade required in this case would be almost identical. The advantages of p-GaAs over p-InGaAs are 1). again, a lack of indium for ease of process integration and no need for hydrogen outgassing, 2). a much lower base transit time $\tau_b = \frac{T_b{}^2}{2D_n} + \frac{T_b}{v_e}$ that reduces C_{diff} for a higher f_T, and 3). a higher Auger-limited current gain $\beta = \frac{\tau_{e,p}}{\tau_b} \approx \frac{\tau_{e,p}\, v_e}{T_b}$. A potential issue with the p-GaAs intrinsic base HBT is junction spiking or base metal sinking that penetrates into the drift collector. Therefore, the added thickness of the regrown extrinsic base process module is suitable for the p-GaAs intrinsic base HBT to prevent excessive metal sinking and improve device reliability. In terms of intrinsic layer epitaxial growth, 4 nm of p-GaAs strained to InP exceeds the Matthews-Blakeslee equilibrium thickness ~ 17.3 Å [6], but should not be an issue as fully strained layers of thicknesses above the Matthews-Blakeslee equilibrium thickness are routinely obtained by MBE at a growth temperature below the relaxation temperature. The band alignment of the proposed InP/strained-GaAs/InP HBT is shown in Fig. 6.2 (right) with a 20 nm thick p-GaAs intrinsic base layer for visual clarity.

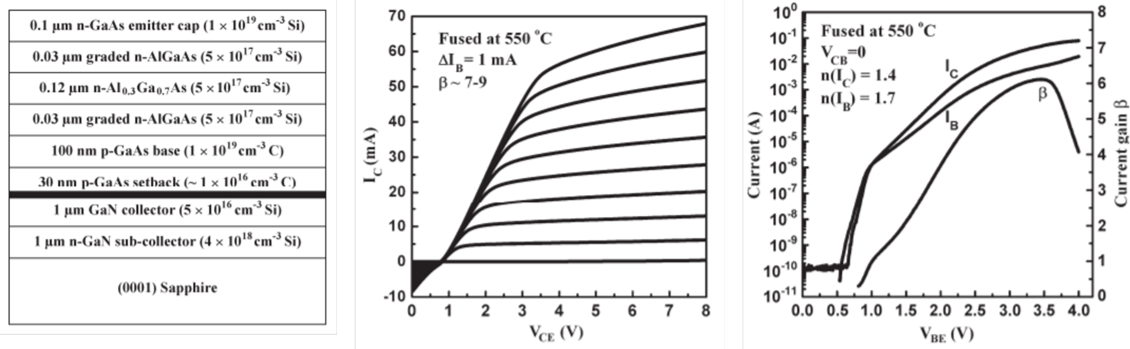

Figure 6.3: Device layer structure of the fused AlGaAs/GaAs/GaN HBT, with the fused interfaced highlighted (left), common-emitter I-V characteristics of a 100 × 120 μm^2 emitter mesa device, and the associated Gummel characteristics (right) [7]

Third, extending the idea of using a fully strained lattice-mismatched material for the intrinsic base of an HBT, a GaN-based HBT with a highly conductive p-type GaAs intrinsic base could be the ultimate transistor technology for RF PA applications that combines GaN's high power handling capability and GaAs's low sheet resistance for a high f_{max}. Previously, an AlGaAs/GaAs/GaN HBT by direct wafer fusion has shown adequate device DC characteristics [7]. The base-collector junction of the AlGaAs/GaAs/GaN HBT is formed by thermally fusing a n-AlGaAs/p-GaAs emitter/base epi grown on a GaAs substrate to a n-GaN drift collector epi grown on a sapphire substrate. Fig. 6.3 shows the relevant device information. Since GaN's wurtzite crystal structure consists of alternating ABCABC layers of close-packed atoms along the basal direction that are compatible with the alternating ABAB stacking of the close-packed (111) planes of GaAs, strained growth of GaAs on GaN is theoretically possible. However, GaN's zinc-blende equivalent lattice constant is 4.49 Å, whereas GaAs has a lattice constant of 5.65 Å. The large mismatch poses challenges in strained growth technologies. One possible solution could be to use an aggressive $\ll 4$ nm thick strained GaAs intrinsic base in conjunction

[ii]Reproduced from "Pryor, C. E., and M-E. Pistol. *Band-edge diagrams for strained III–V semiconductor quantum wells, wires, and dots.* Physical Review B 72.20 (2005): 205311. DOI: 10.1103/PhysRevB.72.205311", with the permission of the American Physical Society.

with a regrown extrinsic base for reliable base metallization.

All of the above proposals require process capabilities *potentially* beyond the ones currently offered at UCSB for full RF device integration. Yet, process module development of some parts of them is reasonable for academic research.

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Appendix A

Regrown Extrinsic Base HBT Process Flows

This appendix describes the process flows for both the quick-and-dirty (QAD) DC diagnostic devices with a large parasitic base-collector mesa, and RF HBTs with a scaled base-collector junction as of May 2021 (Fig. A.1).

Sample Preparation

- Determine substrate orientation. MBE wafers purchased from IQE and IntelliEpi can come in either EJ or US orientation. The difference can be told by holding the wafer up with the major flat pointing upward at 12 o'clock position. If the minor flat is to the right of the major flat at 3 o'clock position, the wafer is clockwise, and EJ cut. If the minor flat is at 9 o'clock position, the wafer is counter-clockwise, and US cut. Emitter stripes should run vertically on a EJ cut wafer, and horizontally on a US cut wafer.

- Cleave the 4" MBE wafers into pieces with appropriate sizes. The Thomas-Swan

InP MOCVD system can only accommodate samples smaller than the size of a 2" wafer (51 mm diagonal), while the cassette for piece samples in the JEOL EBL system at UCSB has a window opening of 22×45 mm^2. One side of the sample must be greatly than 22 mm for the cassette to hold it in place.

- Document sample shape and orientation for future reference.

Emitter Metal Stack Deposition

- Standard solvent clean of sample: 3 min acetone, IPA, running DI water. Be sure to use solvent beakers labeled "Clean MBE wafers only, no prior processing," and MBE-only tweezers.
- Prepare an 1:8 HCl:DI water solution with >250 rpm magnetic stirring for 15 minutes. Dip the sample in the solution for 1 min with slight agitation. While the sample is still in the solution, rinse with DI water and transfer to a rinse beaker. Rinse with DI for 2 min. Sample should be hydrophobic when pulled out. If not, repeat step to clean surface oxides. Dry with 20 psi N_2.
- *Immediately* load the sample into E-beam evaporator #1, and pump down.
- When pressure reaches 1.0e-6 Torr, evaporate ~10 nm Mo with shutter closed to outgas the source material. When pressure is back to 1.0e-6 Torr, open shutter and deposit 20nm Mo at ~ 0.5 Å/s.
- Calibrate TiW alloy composition while waiting for E-beam #1 to cool down. Load Si samples with half of their area covered into Sputter #5. Run a 20 min deposition of pure Ti. Measure Ti film thickness with the Dektak profilometer. Repeat step for pure W. Calculate alloy composition using film thickness and metal density,

and adjust for $Ti_{4wt\%}W$ accordingly. Refer to Appendix B for specific process parameters.

- *Immediately* transfer sample to Sputter #5. Deposit 550 nm $Ti_{4wt\%}W$.

SiON/Cr Hard Mask Deposition

- Clean PECVD #1 with DI water and wipes, and run a 30 min CF_4 plasma clean.
- Season chamber with 20 nm of SiO_x
- Load sample into PECVD #1. Pump down.
- Deposit 80 nm of SiO_x followed by 40nm of SiN_x without breaking vacuum
- Load sample into Thermal evaporator #1, and deposit 30nm of Cr.

Note: The above process steps should be done in succession, and should take a whole day to complete.

Emitter E-beam Lithography

- Retrieve 6% HSQ from the resist fridge, and allow it to reach room temperature before use.
- Place sample on *PRIVATE* spinner chuck free of any resist residue, and apply 6% HSQ. Spin coat at 3000 rpm for 1 min. Bake at 200 °C for 2 min.
- Load the sample into the EBL piece cassette. Ensure angular alignment between sample crystallographic directions and cassette baseline using the fine adjustment knob and Quadra-Chek coordinate measuring machine.

- Expose the sample with appropriate emitter pattern/job with the JEOL 6300 system.
- Develop in a 2 g : 8 g : 200 mL NaOH:NaCl:DI water solution for 2 min. Rinse vigorously with DI water while pulling out the sample from the solution. Place sample under running DI water for 10 min.
- Verify developed pattern using an optical microscope.

Note: Sub-100nm emitter features would be invisible under the microscope. Look for the larger alignment/test structures for verification. HSQ tends to have many particles if not thoroughly rinsed after development.

Cr Hard Mask ICP Dry Etch

- Make sure all gas line switches are in proper positions, and MFC values are correct at ICP #1.
- Run a 15 min oxygen plasma clean. Wait for the ESC chuck to cool down to 10-11°C, and both chamber and column temperatures 50°C.
- Prepare a corral with diced 2" Si pieces mounted on a 6" SEMI standard ICP carrier wafer using mounting grease.
- Season the carrier wafer with recipe #166 for 2 min.
- Place the sample in the center of the corral structure without using any organic mounting grease. Slightly wiggle the assembly to check if the sample can slide off. Rearrange the corral pieces if necessary.
- Etch the Cr hard mask for 90 s with recipe #166.

- Carefully remove sample from the carrier without touching any mounting grease that oozed out from the Si corral.
- Run a 10 min CF_4/O_2 plasma clean.

Emitter Metal Stack ICP Dry Etch

- Make sure all gas line switches are in proper positions, and MFC values are correct at ICP #1.
- Run a 15 min oxygen plasma clean. Wait for the ESC chuck to cool down to 10-11°C, and both chamber and column temperatures 50°C.
- Prepare a corral with diced 2" Si pieces mounted on a 6" SEMI standard ICP carrier wafer using mounting grease.
- Season the carrier wafer with recipe #162 for 1 min.
- Place the sample in the center of the corral structure without using any organic mounting grease. Slightly wiggle the assembly to check if the sample can slide off. Rearrange the corral pieces if necessary.
- Etch the SiON/$Ti_{4wt\%}W$/Mo stack in 30 s increments with recipe #162 to prevent WF_x loading effect and rising chuck temperature that undercuts $Ti_{4wt\%}W$. Rotate sample 90° after each 30 s etch to ensure good uniformity.
- Time recipe #162 etch to remove 40 nm SiN_x, 80 nm SiO_x, and 520 nm of $Ti_{4wt\%}W$, at which point the etch should have completely remove all emitter metal stack around the edges of the sample. But the center of the sample is still covered by ~30/20nm $Ti_{4wt\%}W$/Mo. Etch an additional 20 s to finish the dry etch process.

- Carefully remove sample from the carrier without touching any mounting grease that oozed out from the Si corral.

Note: Recipe #162 rough etch rate = 4 nm/s. If etch rate significantly exceeds 4 nm/s, stop process step *immediately*, and go back to the first line of the process step.

SiON/Cr Hard Mark Lift-off & Residual WO_x Removal

- Pipette 2 drops of Tergitol NP-10 surfactant into a 600 mL teflon beaker. Add 10 mL DI water and mix with a clean pipette to disperse the surfactant.
- Pour in 500 mL of buffered HF. Mix using a magnetic stirrer until foam appears.
- Place the sample vertically in a wafer boat. Submerge sample for 4 min with constant agitation and rotation. Be careful not to pull the sample out of the solution as surface tension would draw lifted off Cr hard mask back to sample surface.
- Rinse vigorously with DI water while pulling out the sample from the solution. Place sample under running DI water for 10 min. Dry with 20 psi N_2.
- Inspect with SEM.
- Standard solvent clean of sample: 3 min acetone, IPA, running DI water. Be sure to use solvent beakers labeled "Clean MBE wafers only, no prior processing," and MBE-only tweezers.

Note: Sample should be hydrophobic after process step. Repeat if otherwise.

First SiN_x Sidewall Formation

- Clean PECVD #1 with DI water and wipes, and run a 30 min CF_4 plasma clean.
- Season chamber with 20 nm of SiN_x.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.
- *Immediately* load the sample along with a 2" Si witness sample. Deposit 15 nm of SiN_x.
- Measure SiN_x thickness with the Woollam ellipsometer.
- Make sure all gas line switches are in proper positions, and MFC values are correct at ICP #1.
- Run a 15 min oxygen plasma clean. Wait for the ESC chuck to cool down to 10-11°C, and both chamber and column temperatures 50°C.
- Prepare a corral with diced 2" Si pieces mounted on a 6" SEMI standard ICP carrier wafer using mounting grease.
- Season the carrier wafer with recipe #187 for 2 min.
- Etch the Si witness for 1 min. Rough etch rate = 11.5 nm/s.
- Place the sample in the center of the corral structure without using any organic mounting grease. Slightly wiggle the assembly to check if the sample can slide off. Rearrange the corral pieces if necessary.
- Etch the SiN_x layer with 20% overetch.

- Carefully remove sample from the carrier without touching any mounting grease that oozed out from the Si corral.

InGaAs Emitter Cap Wet Etch

- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Sample should be hydrophobic when pulled out. If not, repeat step to clean surface oxides. Dry with 20 psi N_2.
- Turn off bench light to prevent illumination-enhanced etching effects.
- Prepare an 1:1:25 H_2O_2:H_3PO_4:DI water solution with >250 rpm magnetic stirring for 15 minutes. Etch the sample in the solution for 10 s with constant agitation. While the sample is still in the solution, rinse with DI water and transfer to a rinse beaker. Rinse with DI for 2 min. Dry with 20 psi N_2.
- Turn on bench light.

Note: H_2O_2 decomposes over time. Be sure to open a new 500 mL bottle every time before use.

Second SiN_x Sidewall Formation

Refer to "First SiN_x Sidewall Formation."

InP Emitter Wet Etch

- Standard solvent clean of sample: 3 min acetone, IPA, running DI water. Be sure to use solvent beakers labeled "Clean MBE wafers only, no prior processing," and MBE-only tweezers.

- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Sample should be hydrophobic when pulled out. If not, repeat step to clean surface oxides. Dry with 20 psi N_2.

- Digital etch $\times 3$ to remove surface contaminants: Oxidize the InP surface with the UV-ozone lamp for 15 min. Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Sample should be hydrophobic when pulled out. Dry with 20 psi N_2.

- Prepare an 1:4 $HCl:H_3PO_4$ solution with >250 rpm magnetic stirring for 15 minutes. Etch the sample in the solution for 10 s with constant agitation. While the sample is still in the solution, rinse with DI water and transfer to a rinse beaker. Rinse with DI for 2 min. Dry with 20 psi N_2.

Note: After InP wet etch, the sample should be *immediately* loaded into the MOCVD system for extrinsic base regrowth to prevent surface oxidation. Doping calibration growth should be done prior to InP wet etch.

MOCVD Extrinsic Base Regrowth

- Calibrate p-type carbon incorporation by growing ~50 nm of p-GaAs or p-InGaAs on one half of 2" SI-InP and one half of 2" SI-GaAs samples. Kelvin probe sheet resistance of the InP substrate sample should be $\sim \times 2$ of the GaAs counterpart, with $\rho_{s,GaAs-on-GaAs} \approx 100\,\Omega/\Box$. The calibration growth also coats the reactor for actual device growth. Refer to Appendix B for MOCVD recipes.

- Grow 50 nm of p-GaAs or p-InGaAs on the sample.

Note: Base metallization should follow base regrowth *immediately*. With the InP emitter

wet etch ($\sim$ 1 hr), and 2 MOCVD growths ($\sim$ 3 hr), it is prudent to start early in the morning, and expect to finish late the night.

Base Contact Lithography and Metallization

- Apply nLoF 2020 on the sample, and spin-coat at 3000 rpm for 60 s. Pre-bake at 110 °C for 60 s.
- Apply SPR 955 on the 4” stepper calibration wafer, and spin-coat at 3000 rpm for 60 s. Pre-bake at 90 °C for 90 s.
- Test expose 9 dies with -100/0/+100 nm pass shift in both X & Y directions on the 4” stepper calibration wafer using the Autostep 200 system. Exposure time = 0.25 s.
- Post-bake the calibration wafer at 110°C for 90 s.
- Develop the calibration wafer in 300MIF for 70 s. Rinse in DI water for 3 min.
- Determine correct pass shift to include for the actual sample by evaluating vernier structures on the calibration wafer under an optical microscope. Overlay accuracy within 100 nm is attainable.
- Expose the sample with the correct pass shift, and appropriate mask. Exposure time = 0.173 s.
- Post-bake the sample at 110°C for 90 s.
- Develop the sample in 300MIF for 70 s. Rinse in DI water for 3 min.
- Verify alignment using the vernier structures. Rework if misalignment is unacceptable.

- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.
- Deposit 35/100/150/1300 Å Pd/Ti/Pd/Au in E-beam #1. Deposition rate < 0.5 Å/s for Pd/Ti/Pd, and $1 \sim 3$ Å/s for Au.
- Strip and lift off in NMP at 80°C for 1 hour, followed by standard solvent clean of sample: 3 min acetone, IPA, running DI water.

Note: Stepper calibration should be good for the rest of the day. Thus, if group members had calibrated the system prior, it is possible to skip re-calibration.

Third SiN_x Sidewall Formation

Refer to "First SiN_x Sidewall Formation."

Base Post Lithography and Metallization (RF Process Only)

- Apply nLoF 2020 on the sample, and spin-coat at 3000 rpm for 60 s. Pre-bake at 110 °C for 60 s.
- Apply SPR 955 on the 4" stepper calibration wafer, and spin-coat at 3000 rpm for 60 s. Pre-bake at 90 °C for 90 s.
- Test expose 9 dies with -100/0/+100 nm pass shift in both X & Y directions on the 4" stepper calibration wafer using the Autostep 200 system. Exposure time = 0.25 s.
- Post-bake the calibration wafer at 110°C for 90 s.
- Develop the calibration wafer in 300MIF for 70 s. Rinse in DI water for 3 min.

- Determine correct pass shift to include for the actual sample by evaluating vernier structures on the calibration wafer under an optical microscope. Overlay accuracy within 100 nm is attainable.
- Expose the sample with the correct pass shift, and appropriate mask. Exposure time = 0.173 s.
- Post-bake the sample at 110°C for 90 s.
- Develop the sample in 300MIF for 70 s. Rinse in DI water for 3 min.
- Verify alignment using the vernier structures. Rework if misalignment is unacceptable.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.
- Deposit 200/5000 Å Ti/Au in E-beam #1. Deposition rate < 1 Å/s for Ti, and $1 \sim 4.5$ Å/s for Au.
- Strip and lift off in NMP at 80°C for 1 hour, followed by standard solvent clean of sample: 3 min acetone, IPA, running DI water.

Base-collector Mesa Lithography

- Clean PECVD #1 with DI water and wipes, and run a 30 min CF_4 plasma clean.
- Season chamber with 20 nm of SiN_x.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.

- *Immediately* load the sample along with a 2" Si witness sample. Deposit 3.5 nm of SiN_x.
- Measure SiN_x thickness with the Woollam ellipsometer.
- Apply SPR 955 on the sample, and spin-coat at 3000 rpm for 60 s. Pre-bake at 90 °C for 90 s.
- Apply SPR 955 on the 4" stepper calibration wafer, and spin-coat at 3000 rpm for 60 s. Pre-bake at 90 °C for 90 s.
- Test expose 9 dies with -100/0/+100 nm pass shift in both X & Y directions on the 4" stepper calibration wafer using the Autostep 200 system. Exposure time = 0.25 s.
- Post-bake the calibration wafer at 110°C for 90 s.
- Develop the calibration wafer in 300MIF for 70 s. Rinse in DI water for 3 min.
- Determine correct pass shift to include for the actual sample by evaluating vernier structures on the calibration wafer under an optical microscope. Overlay accuracy within 100 nm is attainable.
- Expose the sample with the correct pass shift, and appropriate mask. Exposure time = 0.25 s.
- Post-bake the sample at 110°C for 90 s.
- Develop the sample in 300MIF for 70 s. Rinse in DI water for 3 min.
- Verify alignment using the vernier structures. Rework if misalignment is unacceptable.

- Make sure all gas line switches are in proper positions, and MFC values are correct at ICP #1.
- Run a 15 min oxygen plasma clean. Wait for the ESC chuck to cool down to 10-11°C, and both chamber and column temperatures 50°C.
- Prepare a corral with diced 2" Si pieces mounted on a 6" SEMI standard ICP carrier wafer using mounting grease.
- Season the carrier wafer with recipe #187 for 2 min.
- Etch the Si witness for 1 min. Rough etch rate = 11.5 nm/s.
- Place the sample in the center of the corral structure without using any organic mounting grease. Slightly wiggle the assembly to check if the sample can slide off. Rearrange the corral pieces if necessary.
- Etch the SiN_x layer with 20% overetch.
- Carefully remove sample from the carrier without touching any mounting grease that oozed out from the Si corral.

Base-collector Mesa Wet Etch

- Measure resist height profile at $>$ 9 points across the sample using the Dektak profilometer.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Sample should be hydrophobic when pulled out. If not, repeat step to clean surface oxides. Dry with 20 psi N_2.
- Turn off bench light to prevent illumination-enhanced etching effects.

- Prepare an 1:1:25 H_2O_2:H_3PO_4:DI water solution with >250 rpm magnetic stirring for 15 minutes. Etch the sample in the solution for 45 s with constant agitation. While the sample is still in the solution, rinse with DI water and transfer to a rinse beaker. Rinse with DI for 2 min. Dry with 20 psi N_2.
- Turn on bench light.
- Measure resist height profile at > 9 points across the sample using the Dektak profilometer. A height difference of 120 nm is expected to ensure all GaAs/InGaAs/InAlAs in the field has been removed.
- Prepare an 1:4 HCl:H_3PO_4 solution with >250 rpm magnetic stirring for 15 minutes. Etch the sample in the solution for 14 s with constant agitation. While the sample is still in the solution, rinse with DI water and transfer to a rinse beaker. Rinse with DI for 2 min. Dry with 20 psi N_2.
- Measure resist height profile at > 9 points across the sample using the Dektak profilometer. A height difference of 80 nm is expected to ensure all InP in the field has been removed.
- Verify sheet resistance of the n-type subcollector using Kelvin probing.

Note: The 1:1:25 H_2O_2:H_3PO_4:DI water solution undercuts GaAs/InGaAs/InAlAs at 4 nm/s. Therefore, base-collector lithographic dimensions have been adjusted accordingly to accommodate the undercut.

Fourth SiN_x Sidewall Formation

Refer to "First SiN_x Sidewall Formation."

Collector Contact Lithography and Metallization

- Apply nLoF 2020 on the sample, and spin-coat at 3000 rpm for 60 s. Pre-bake at 110 °C for 60 s.
- Expose the sample with the appropriate mask. Exposure time = 0.173 s.
- Post-bake the sample at 110°C for 90 s.
- Develop the sample in 300MIF for 70 s. Rinse in DI water for 3 min.
- Verify alignment using the vernier structures. Rework if misalignment is unacceptable.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.
- Deposit 150/200/2050 Å Ti/Pd/Au in E-beam #1. Deposition rate $<$ 1 Å/s for Ti/Pd, and 1 $\sim$ 4.5 Å/s for Au.
- Strip and lift off in NMP at 80°C for 1 hour, followed by standard solvent clean of sample: 3 min acetone, IPA, running DI water.

Collector Post Lithography and Metallization (RF Process Only)

- Apply nLoF 2020 on the sample, and spin-coat at 3000 rpm for 60 s. Pre-bake at 110 °C for 60 s.
- Expose the sample with the appropriate mask. Exposure time = 0.173 s.
- Post-bake the sample at 110°C for 90 s.
- Develop the sample in 300MIF for 70 s. Rinse in DI water for 3 min.

- Verify alignment using the vernier structures. Rework if misalignment is unacceptable.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.
- Deposit 200/5000 Å Ti/Au in E-beam #1. Deposition rate < 1 Å/s for Ti, and 1 $\sim$ 4.5 Å/s for Au.
- Strip and lift off in NMP at 80°C for 1 hour, followed by standard solvent clean of sample: 3 min acetone, IPA, running DI water.

Device Isolation Lithography (RF Process Only)

- Clean PECVD #1 with DI water and wipes, and run a 30 min CF_4 plasma clean.
- Season chamber with 20 nm of SiN_x.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.
- *Immediately* load the sample along with a 2" Si witness sample. Deposit 15 nm of SiN_x.
- Measure SiN_x thickness with the Woollam ellipsometer.
- Apply SPR 955 on the sample, and spin-coat at 3000 rpm for 60 s. Pre-bake at 90 °C for 90 s.
- Apply SPR 955 on the 4" stepper calibration wafer, and spin-coat at 3000 rpm for 60 s. Pre-bake at 90 °C for 90 s.

- Test expose 9 dies with -100/0/+100 nm pass shift in both X & Y directions on the 4” stepper calibration wafer using the Autostep 200 system. Exposure time = 0.25 s.
- Post-bake the calibration wafer at 110°C for 90 s.
- Develop the calibration wafer in 300MIF for 70 s. Rinse in DI water for 3 min.
- Determine correct pass shift to include for the actual sample by evaluating vernier structures on the calibration wafer under an optical microscope. Overlay accuracy within 100 nm is attainable.
- Expose the sample with the correct pass shift, and appropriate mask. Exposure time = 0.25 s.
- Post-bake the sample at 110°C for 90 s.
- Develop the sample in 300MIF for 70 s. Rinse in DI water for 3 min.
- Verify alignment using the vernier structures. Rework if misalignment is unacceptable.
- Make sure all gas line switches are in proper positions, and MFC values are correct at ICP #1.
- Run a 15 min oxygen plasma clean. Wait for the ESC chuck to cool down to 10-11°C, and both chamber and column temperatures 50°C.
- Prepare a corral with diced 2” Si pieces mounted on a 6” SEMI standard ICP carrier wafer using mounting grease.
- Season the carrier wafer with recipe #187 for 2 min.

- Etch the Si witness for 1 min. Rough etch rate = 11.5 nm/s.
- Place the sample in the center of the corral structure without using any organic mounting grease. Slightly wiggle the assembly to check if the sample can slide off. Rearrange the corral pieces if necessary.
- Etch the SiN_x layer with 20% overetch.
- Carefully remove sample from the carrier without touching any mounting grease that oozed out from the Si corral.

Device Isolation Wet Etch (RF Process Only)

- Measure resist height profile at > 9 points across the sample using the Dektak profilometer.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Sample should be hydrophobic when pulled out. If not, repeat step to clean surface oxides. Dry with 20 psi N_2.
- Turn off bench light to prevent illumination-enhanced etching effects.
- Prepare an 1:1:25 H_2O_2:H_3PO_4:DI water solution with >250 rpm magnetic stirring for 15 minutes. Etch the sample in the solution for 15 s with constant agitation. While the sample is still in the solution, rinse with DI water and transfer to a rinse beaker. Rinse with DI for 2 min. Dry with 20 psi N_2.
- Turn on bench light.
- Prepare an 1:4 HCl:H_3PO_4 solution with >250 rpm magnetic stirring for 15 minutes. Etch the sample in the solution for 30 s with constant agitation. While the sample

is still in the solution, rinse with DI water and transfer to a rinse beaker. Rinse with DI for 2 min. Dry with 20 psi N_2.

- Measure resist height profile at $>$ 9 points across the sample using the Dektak profilometer. A height difference of 295 nm is expected to ensure all InGaAs/InP subcollector in the field has been removed.
- Turn off bench light to prevent illumination-enhanced etching effects.
- Prepare a *new* 1:1:25 H_2O_2:H_3PO_4:DI water solution with >250 rpm magnetic stirring for 15 minutes. Etch the sample in the solution for 15 s with constant agitation. While the sample is still in the solution, rinse with DI water and transfer to a rinse beaker. Rinse with DI for 2 min. Dry with 20 psi N_2.
- Turn on bench light.
- Prepare a *new* 1:4 HCl:H_3PO_4 solution with >250 rpm magnetic stirring for 15 minutes. Etch the sample in the solution for 15 s with constant agitation. While the sample is still in the solution, rinse with DI water and transfer to a rinse beaker. Rinse with DI for 2 min. Dry with 20 psi N_2.
- Measure resist height profile at $>$ 9 points across the sample using the Dektak profilometer. A height difference of 280 nm is expected to ensure device isolation is complete, and reaches SI-InP substrate below the MBE growth interface.

SiN_x Anchor Layer Deposition

- Clean PECVD #1 with DI water and wipes, and run a 30 min CF_4 plasma clean.
- Lower chuck temperature to 150°C.

- Season chamber with 20 nm of SiN_x.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.
- *Immediately* load the sample along with a 2" Si witness sample. Deposit 25 nm of SiN_x using the 150°C recipe.
- Reset chuck temperature to 250°C.
- Measure SiN_x thickness with the Woollam ellipsometer.

Note: SiN_x thickness on device mesa includes 15 nm from the device isolation process step and 25 nm from the anchor layer deposition step for a total of 40 nm.

BCB Planarization

- Turn on Blue oven and purge with 100 scfh N_2 for 15 min.
- Apply BCB on the sample. Wait 60 s and spin-coat at 2500 rpm.
- *Immediately* transfer the sample into Blue oven. Set N_2 flow to 60 scfh.
- Ramp to 50°C over 5 min, and soak for 5 min.
- Ramp to 100°C over 15 min, and soak for 15 min.
- Ramp to 150°C over 15 min, and soak for 15 min.
- Ramp to 250°C over 60 min, and soak for 60 min.
- Wait $\sim$ 10 hr for the chamber to cool down with the chamber door closed.
- Measure cured BCB thickness with the Woollam ellipsometer using the "BCB on Au" recipe. Expect 3 um thickness.

- Make sure all gas line switches are in proper positions, and MFC values are correct at ICP #1.
- Run a 15 min oxygen plasma clean. Wait for the ESC chuck to cool down to 50°C, and both chamber and column temperatures 50°C.
- Prepare a corral with diced 2" Si pieces mounted on a 6" SEMI standard ICP carrier wafer using mounting grease.
- Season the carrier wafer with recipe #328 for 5 min.
- Place the sample in the center of the corral structure without using any organic mounting grease. Slightly wiggle the assembly to check if the sample can slide off. Rearrange the corral pieces if necessary.
- Etch the BCB layer in 30 s increments with recipe #328 to prevent strong loading effect. Rotate the sample 90° after each 30 s etch to ensure good uniformity.
- Measure cured BCB thickness with the Woollam ellipsometer using the "BCB on Au" recipe. Repeat recipe #328 is necessary. For DC process, first target 800 nm remaining BCB thickness. For RF process, first target 1.4 um remaining BCB thickness.
- Etch the BCB layer in 15 s increments with recipe #328. Rotate the sample 90° after each etch to ensure good uniformity. Measure emitter, base and collector posts with the Bruker AFM at >9 points across the sample. As soon as average emitter protrusion is 100 nm tall, BCB planarization is complete.

SiN_x Adhesion Layer Deposition

- Clean PECVD #1 with DI water and wipes, and run a 30 min CF_4 plasma clean.

- Lower chuck temperature to 150°C.
- Season chamber with 20 nm of SiN_x.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.
- *Immediately* load the sample along with a 2" Si witness sample. Deposit 45 nm of SiN_x using the 150°C recipe.
- Reset chuck temperature to 250°C.
- Measure SiN_x thickness with the Woollam ellipsometer.

Adhesion Layer Via Opening

- Apply SPR 955 on the sample, and spin-coat at 3000 rpm for 60 s. Pre-bake at 90 °C for 90 s.
- Expose the sample with the correct pass shift, and appropriate mask. Exposure time = 0.25 s.
- Post-bake the sample at 110°C for 90 s.
- Develop the sample in 300MIF for 70 s. Rinse in DI water for 3 min.
- Verify alignment using the vernier structures. Rework if misalignment is unacceptable.
- Make sure all gas line switches are in proper positions, and MFC values are correct at ICP #1.

- Run a 15 min oxygen plasma clean. Wait for the ESC chuck to cool down to 10-11°C, and both chamber and column temperatures 50°C.

- Prepare a corral with diced 2" Si pieces mounted on a 6" SEMI standard ICP carrier wafer using mounting grease.

- Season the carrier wafer with recipe #187 for 2 min.

- Etch the Si witness for 1 min. Rough etch rate = 11.5 nm/s.

- Place the sample in the center of the corral structure without using any organic mounting grease. Slightly wiggle the assembly to check if the sample can slide off. Rearrange the corral pieces if necessary.

- Etch the SiN_x layer with 20% overetch.

- Carefully remove sample from the carrier without touching any mounting grease that oozed out from the Si corral.

- Strip in NMP at 80°C for 1 hour, followed by standard solvent clean of sample: 3 min acetone, IPA, running DI water.

Metal 1 Lithography and Metallization

- Apply nLoF 2020 on the sample, and spin-coat at 3000 rpm for 60 s. Pre-bake at 110 °C for 60 s.

- Apply SPR 955 on the 4" stepper calibration wafer, and spin-coat at 3000 rpm for 60 s. Pre-bake at 90 °C for 90 s.

- Test expose 9 dies with -100/0/+100 nm pass shift in both X & Y directions on the 4" stepper calibration wafer using the Autostep 200 system. Exposure time = 0.25 s.
- Post-bake the calibration wafer at 110°C for 90 s.
- Develop the calibration wafer in 300MIF for 70 s. Rinse in DI water for 3 min.
- Determine correct pass shift to include for the actual sample by evaluating vernier structures on the calibration wafer under an optical microscope. Overlay accuracy within 100 nm is attainable.
- Expose the sample with the correct pass shift, and appropriate mask. Exposure time = 0.173 s.
- Post-bake the sample at 110°C for 90 s.
- Develop the sample in 300MIF for 70 s. Rinse in DI water for 3 min.
- Verify alignment using the vernier structures. Rework if misalignment is unacceptable.
- Etch the sample in 1:10 HCl:DI water solution for 1 min. Rinse with DI water for 2 min. Dry with 20 psi N_2.
- Deposit 20/1100 nm Ti/Au in E-beam #1. Deposition rate < 1 Å/s for Ti, and $1 \sim 7.0$ Å/s for Au.
- Strip and lift off in NMP at 80°C for 1 hour, followed by standard solvent clean of sample: 3 min acetone, IPA, running DI water.

Note: M1 lithography is a critical alignment step as spacing between base and emitter wiring can be small.

Field BCB Removal (DC Process Only)

- Make sure all gas line switches are in proper positions, and MFC values are correct at ICP #1.
- Run a 15 min oxygen plasma clean. Wait for the ESC chuck to cool down to 50°C, and both chamber and column temperatures 50°C.
- Prepare a corral with diced 2" Si pieces mounted on a 6" SEMI standard ICP carrier wafer using mounting grease.
- Season the carrier wafer with recipe #328 for 5 min.
- Place the sample in the center of the corral structure without using any organic mounting grease. Slightly wiggle the assembly to check if the sample can slide off. Rearrange the corral pieces if necessary.
- Etch the BCB layer in 30 s increments with recipe #328 to prevent strong loading effect. Rotate the sample 90° after each 30 s etch to ensure good uniformity.
- Measure cured BCB thickness with the Woollam ellipsometer using the "BCB on Au" recipe. Repeat recipe #328 is necessary. First target 300 nm remaining BCB thickness.
- Etch the BCB layer in 15 s increments with recipe #328. Rotate the sample 90° after each etch to ensure good uniformity. Measure base and collector pads with the Bruker AFM at >9 points across the sample. As soon as average base and collector pad protrusion is 100 nm tall, field BCB removal is complete.

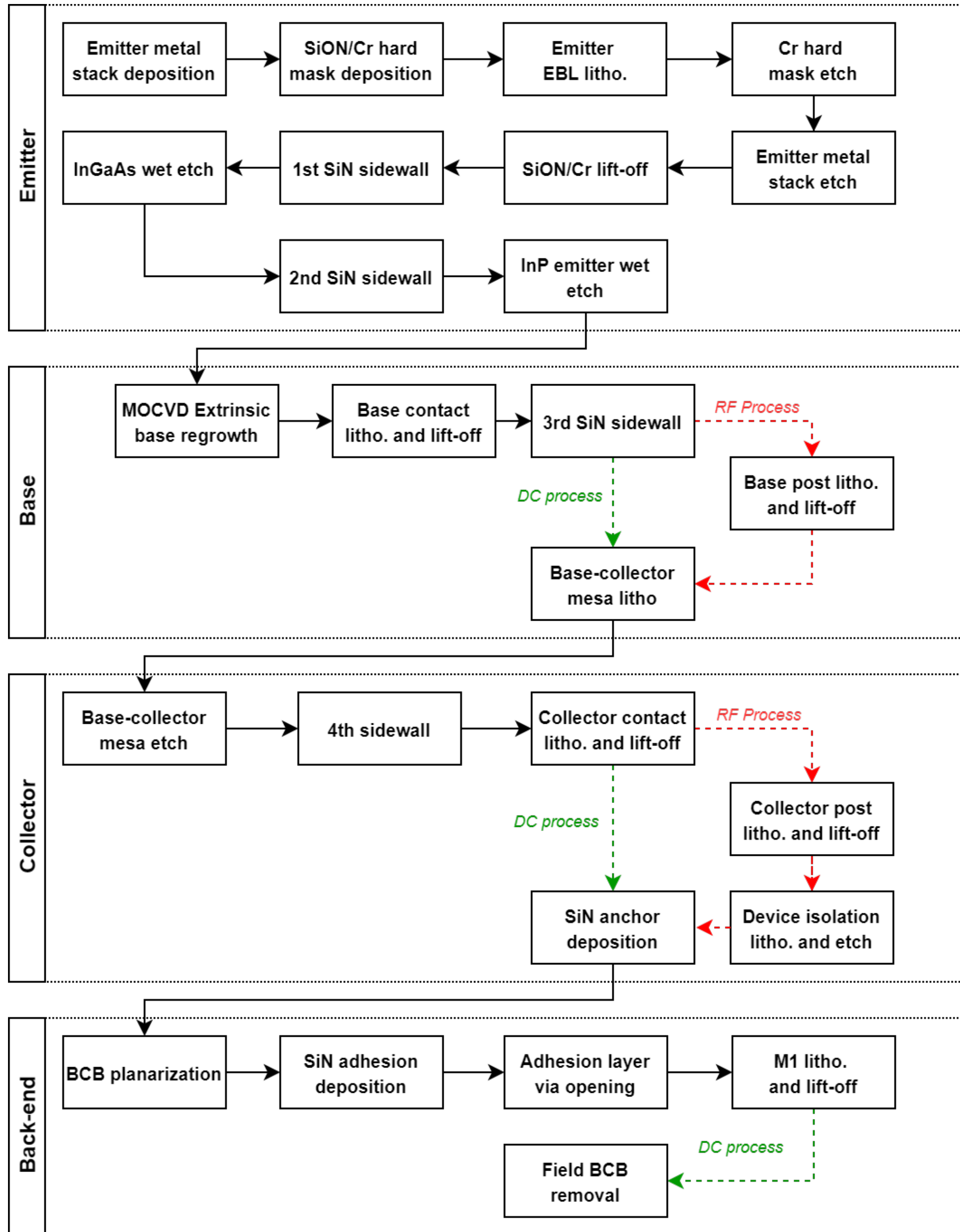

Figure A.1: Process flow chart for DC and RF processes

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Appendix B

Process Recipes

This appendix attempts to document minute details of the regrown extrinsic base HBT process flows for future reproduction. Previously, only electronic copies were kept for process recipes within the group. Due to hard drive failures, however, all process recipes had to be painstakingly re-established. Therefore, it is prudent to preserve the trope of process knowledge in a thesis.

List of Wet Chemicals

Chemical	Concentration	Vendor	Abbreviation
Acetone	ACS grade	Fisher Scientific	Acetone
Isopropyl alcohol	Optima grade	Fisher Scientific	IPA
Deionized water	-	In-house	DI water
Hydrochloric acid	36.5 - 38.0 wt%	Fisher Scientific	HCl
Buffered hydrofluoric acid	4 - 8 %	Transene Company	BHF
Tergitol NP-10	-	Fisher Scientific	Tergitol
Phosphoric acid	$\geq$ 85.0 wt%	Fisher Scientific	H_3PO_4
Hydrogen peroxide	30.0 - 32.0 %	Fisher Scientific	H_2O_2
AZ nLoF 2020 negative resist	-	Merck	nLoF 2020
AZ 300 MIF Developer	-	Merck	300MIF
AZ NMP photoresist stripper	-	Merck	NMP
MICROPOSIT SPR 955 resist	-	MICROCHEM CORP.	SPR 955
Hydrogen silsesquioxane resist	6%	Dow Corning	HSQ 6%
Cyclotene 3022-46	-	Dow	BCB

List of ICP #1 Recipes

ICP #1 is a Panasonic E646V ICP etching system. All recipes have a He back pressure of 400 Pa.

#166 Cl_2/O_2 Cr dry etch recipe

Gas flow (sccm)	Step 1	Step 2	Step 3	Step 4	Step 5
Cl_2	24.0	24.0	24.0	0	0
O_2	6.0	6.0	6.0	0	0
He	0	0	0	100	100
Pressure (Pa)	2.00	1.33	1.33	2.50	2.50
Vacuum time (m:s)	0:00	0:00	0:45	0:00	0:00
RF wait time (m:s)	0:15	0:00	0:00	0:15	0:00
Source power (W)	600	600	600	100	50
Bias power (W)	0	0	50	0	0
Dead time (m:s)	0:05	0:05	0:05	0:05	0:05
Step time (m:s)	0:03	0:03	1:30	0:03	0:05

#162 SF_6/Ar $Ti_{4wt\%}W$ dry etch recipe

Gas flow (sccm)	Step 1	Step 2	Step 3	Step 4	Step 5
SF_6	20.0	20.0	20.0	0	0
Ar	5.0	5.0	5.0	0	0
He	0	0	0	50	50
Pressure (Pa)	2.00	1.00	1.00	2.00	2.50
Vacuum time (m:s)	0:00	0:00	1:00	0:00	1:00
RF wait time (m:s)	0:10	0:00	0:00	0:15	0:00
Source power (W)	600	600	600	100	50
Bias power (W)	0	0	200	0	0
Dead time (m:s)	0:05	0:05	0:05	0:10	0:05
Step time (m:s)	0:03	0:03	0:30	0:10	0:05

#187 CF_4/O_2 SiN_x dry etch recipe

Gas flow (sccm)	Step 1	Step 2	Step 3	Step 4	Step 5
CF_4	20.0	20.0	20.0	0	0
O_2	2.0	2.0	2.0	0	0
He	0	0	0	50	50
Pressure (Pa)	1.00	0.50	0.30	2.50	2.50
Vacuum time (m:s)	0:00	0:00	0:15	0:00	0:45
RF wait time (m:s)	0:15	0:00	0:00	0:15	0:00
Source power (W)	200	100	25	100	50
Bias power (W)	0	0	19	0	0
Dead time (m:s)	0:05	0:05	0:05	0:05	0:05
Step time (m:s)	0:05	0:05	1:45	0:05	0:05

#328 CF_4/O_2 BCB dry etch recipe

Gas flow (sccm)	Step 1
O_2	200.0
CF_4	50.0
Pressure (Pa)	40.0
Vacuum time (m:s)	1:00
RF wait time (m:s)	0:10
Source power (W)	1000
Dead time (m:s)	0:10
Step time (m:s)	0:30

List of Sputter #5 Recipes

Sputter #5 is an AJA International ATC 2200-V sputter system. All metal films are deposited with DC sputtering.

Pure Ti calibration recipe

Parameter	Value
Substrate Z height	1.50
Substrate rotation (rpm)	20
Pressure (mTorr)	3
Ar flow (sccm)	45
Target enabled	Ti
Gun tilt	10
Ramp time (s)	20
Power setpoint (W)	280
Shutter delay (s)	60
Coat time (s)	1260

Pure W calibration recipe

Parameter	Value
Substrate Z height	1.50
Substrate rotation (rpm)	20
Pressure (mTorr)	3
Ar flow (sccm)	45
Target enabled	W
Gun tilt	10
Ramp time (s)	20
Power setpoint (W)	300
Shutter delay (s)	60
Coat time (s)	1260

$Ti_{4wt\%}W$ deposition recipe

Substrate Z height	1.50
Substrate rotation (rpm)	20
Pressure (mTorr)	3
Ar flow (sccm)	45
Target enabled	Ti/W
Gun tilt	10/10
Ramp time (s)	20/20
Power setpoint (W)	280/300
Shutter delay (s)	60/60
Coat time (s)	3960/3960

List of PECVD #1 Recipes

PECVD #1 is a Plasma-Therm Series 790 System VII dielectric PECVD system.

250°C SiN_x recipe

Chuck temperature (°C)	250
Deposition time (s)	74
Pressure (mTorr)	900
RF power (W)	22
SiH_4 flow (sccm)	150
N_2 flow (sccm)	450
NH_3 flow (sccm)	1.54

150°C SiN_x recipe

Parameter	Value
Chuck temperature (°C)	150
Deposition time (s)	180
Pressure (mTorr)	900
RF power (W)	22
SiH_4 flow (sccm)	150
N_2 flow (sccm)	450
NH_3 flow (sccm)	1.54

250°C SiO_x recipe

Parameter	Value
Chuck temperature (°C)	250
Deposition time (s)	115
Pressure (mTorr)	900
RF power (W)	22
SiH_4 flow (sccm)	100
N_2O flow (sccm)	300

List of MOCVD Recipes

The InP MOCVD system is a Thomas-Swan 2" horizontal laminar flow reactor with TMGa, TEGa, TMAl, TMIn, TBP, TBAs, CBr_4, DEZn, and DiSi bubbler sources installed. The system uses H_2 as carrier gas, and is capable of in-situ switching to N_2 for post-growth anneal. Heat is provided by 2 sets of infrared heating elements. TMGa bubbler is maintained at -3.9 °C, TEGa 18 °C, TMIn 21.9 °C, TBAs 1.9 °C, and CBr_4 21 °C. Real-time metalorganic flows are measured and controlled individually with Epison acoustic impedance monitors attached to the outlets of the bubblers. Group III/V precursors are premixed in 2 parallel gas manifolds, labeled as "upper manifold" and "lower manifold", before being fed into the reactor. Each manifold has a nominal gas flow rate of 8,000 sccm with H_2 makeup lines to compensate for flow differences caused by switching of precursors. The nominal total gas flow rate is 16,000 sccm. Growth pressure is set to 350 Torr.

Carbon is amphoteric, and can take both III- and V- sites, causing self-compensation. For carbon-doped p-type growths, extremely low V/III ratio is required to drive carbon atoms to take group V lattice sites.

4e20 cm^{-3} 490 °C p-GaAs with in-situ N_2 activation anneal

Step	ID	Time (s)	Temp. (°C)	Pressure (Torr)	Carrier	TBAs	CBr_4	TMGa
1	Mfld	-	-	-	H_2	H_2	H_2	H_2
2	Tox	mfld	mfld	mfld	mfld	mfld	mfld	mfld
3	Ord	10	-	770.00	500.00/500.00	44.400	25.000	8.0000
4	Tox	mfld	mfld	mfld	mfld	mfld	mfld	mfld
5	Loop x3	-	-	-	-	-	-	-
6	Ramp	15.0	-	720.00	500.00/500.00	44.400	25.000	8.0000
7	Ramp	100	-	30.000	500.00/500.00	44.400	25.000	8.0000
8	Ord	15.0	-	30.000	500.00/500.00	44.400	25.000	8.0000

9	Ramp	15.0	-	30.000	5000.0/5000.0	44.400	25.000	8.0000
10	Ramp	150	-	720.00	5000.0/5000.0	44.400	25.000	8.0000
11	Loop end	-	-	-	-	-	-	-
12	Ramp	15.0	-	720.00	8000.0/8000.0	100.00	115.00	8.0000
13	Ramp	60.0	-	350.00	8000.0/8000.0	100.00	115.00	8.0000
14	Ord	60.0	300	350.00	8000.0/8000.0	100.00	115.00	8.0000
15	Tox	-	-	350.00	-	Tox	Tox	Tox
16	Ord	120	300	350.00	8000.0/8000.0	100.00	115.00	8.0000
17	Epis	-	-	-	-	4.080	0.129	0.465
18	Ord	90.0	300	350.00	8000.0/8000.0	100.00	115.00	8.0000
19	Ord	60.0	540	350.00	8000.0/8000.0	100.00	115.00	8.0000
20	Ord	90.0	540	350.00	8000.0/8000.0	100.00	115.00	8.0000
21	Ord	60.0	490	350.00	8000.0/8000.0	100.00	115.00	8.0000
22	Ord	410	490	350.00	8000.0/8000.0	100.00	115.00	8.0000
23	Tox	-	-	-	-	-	mfld	mfld
24	Ramp	60.0	490	650.00	8000.0/8000.0	33.000	115.00	8.0000
25	Ord	10.0	490	650.00	8000.0/8000.0	33.000	25.000	8.0000
26	Tox	-	-	-	-	mfld	-	-
27	Ramp	30.0	490	720.00	8000.0/8000.0	44.400	25.000	8.0000
28	Mfld	-	-	-	N_2	-	-	-
29	Ord	450	490	720.00	500.00/500.00	44.400	25.000	8.0000
30	Loop x3	-	-	-	-	-	-	-
31	Ramp	15.0	-	720.00	500.00/500.00	44.400	25.000	8.0000
32	Ramp	120	-	30.000	500.00/500.00	44.400	25.000	8.0000
33	Ord	15.0	-	30.000	500.00/500.00	44.400	25.000	8.0000
34	Ramp	15.0	-	30.000	5000.0/5000.0	44.400	25.000	8.0000
35	Ramp	120	-	720.00	5000.0/5000.0	44.400	25.000	8.0000
36	Loop end	-	-	-	-	-	-	-
37	Ramp	60.0	-	770.00	5000.0/5000.0	44.400	25.000	8.0000
38	Ord	30.0	-	770.00	500.00/500.00	44.400	25.000	8.0000
39	End	-	-	-	-	-	-	-

Note: All gas flow rates are in sccm. Solid color indicates open bubbler valves. Nominal

TMGa flow = 2.59e-5 mol/min, nominal TBAs flow = 3.3e-4 mol/min, nominal CBr_4 flow = 5.1e-6 mol/min, and nominal V/III ratio = 12.85. Growth rate ~ 1.3 Å/s

5e18 cm^{-3} 450 °C p-InGaAs with in-situ N_2 activation anneal

Step	ID	Time (s)	Temp. (°C)	Pressure (Torr)	Carrier	TBAs	CBr_4	TEGa	TMIn
1	Mfld	-	-	-	H_2	H_2	H_2	H_2	H_2
2	Tox	mfld	mfld	mfld	mfld	mfld	mfld	mfld	mfld
3	Ord	10	-	770.00	500.00/500.00	44.400	25.000	125.00	165.00
4	Tox	mfld	mfld	mfld	mfld	mfld	mfld	mfld	mfld
5	Loop x3	-	-	-	-	-	-	-	-
6	Ramp	15.0	-	720.00	500.00/500.00	44.400	25.000	125.00	165.00
7	Ramp	100	-	30.000	500.00/500.00	44.400	25.000	125.00	165.00
8	Ord	15.0	-	30.000	500.00/500.00	44.400	25.000	125.00	165.00
9	Ramp	15.0	-	30.000	5000.0/5000.0	44.400	25.000	125.00	165.00
10	Ramp	150	-	720.00	5000.0/5000.0	44.400	25.000	125.00	165.00
11	Loop end	-	-	-	-	-	-	-	-
12	Ramp	15.0	-	720.00	8000.0/8000.0	23.000	50.000	125.00	165.00
13	Ramp	60.0	-	350.00	8000.0/8000.0	23.000	50.000	125.00	165.00
14	Ord	60.0	300	350.00	8000.0/8000.0	23.000	50.000	125.00	165.00
15	Tox	-	-	350.00	-	Tox	Tox	Tox	Tox
16	Ord	120	300	350.00	8000.0/8000.0	23.000	50.000	125.00	165.00
17	Epis	-	-	-	-	2.600	0.129	-	0.125
18	Ord	90.0	300	350.00	8000.0/8000.0	23.000	50.000	125.00	165.00
19	Ord	60.0	540	350.00	8000.0/8000.0	23.000	50.000	125.00	165.00
20	Ord	90.0	540	350.00	8000.0/8000.0	23.000	50.000	125.00	165.00
21	Ord	60.0	450	350.00	8000.0/8000.0	23.000	50.000	125.00	165.00
22	Ord	756	450	350.00	8000.0/8000.0	23.000	50.000	125.00	165.00
23	Tox	-	-	-	-	-	mfld	mfld	mfld
24	Ramp	60.0	450	650.00	8000.0/8000.0	23.000	50.000	125.00	165.00
25	Ord	10.0	450	650.00	8000.0/8000.0	23.000	25.000	125.00	165.00
26	Tox	-	-	-	-	mfld	-	-	-
27	Ramp	30.0	490	720.00	8000.0/8000.0	44.400	25.000	125.00	165.00
28	Mfld	-	-	-	N_2	-	-	-	-

29	Ord	300	490	720.00	500.00/500.00	44.400	25.000	125.00	165.00
30	Loop x3	-	-	-	-	-	-	-	-
31	Ramp	15.0	-	720.00	500.00/500.00	44.400	25.000	125.00	165.00
32	Ramp	120	-	30.000	500.00/500.00	44.400	25.000	125.00	165.00
33	Ord	15.0	-	30.000	500.00/500.00	44.400	25.000	125.00	165.00
34	Ramp	15.0	-	30.000	5000.0/5000.0	44.400	25.000	125.00	165.00
35	Ramp	120	-	720.00	5000.0/5000.0	44.400	25.000	125.00	165.00
36	Loop end	-	-	-	-	-	-	-	-
37	Ramp	60.0	-	770.00	5000.0/5000.0	44.400	25.000	125.00	165.00
38	Ord	30.0	-	770.00	500.00/500.00	44.400	25.000	125.00	165.00
39	End	-	-	-	-	-	-	-	-

Note: All gas flow rates are in sccm. Solid color indicates open bubbler valves. Nominal TEGa flow = 3.21e-5 mol/min, nominal TBAs flow = 7.66e-5 mol/min, nominal TMIn flow = 1.93e-5 mol/min, nominal CBr_4 flow = 2.20e-6 mol/min, and nominal V/III ratio = 1.49. Growth rate $\sim$ 0.8 Å/s

Unfortunate date of RG64RF-F regrowth

Year 2021	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Week 15 (April 11 - 17)	No Growth	Laser Growth	Laser Growth	Laser Growth	Laser Growth	Laser Growth	N_2 Shutdown
Week 16 (April 18 - 24)	N_2 Shutdown	N_2 Shutdown	Pump Failure	RG64RF-F Regrowth	H_2 Shutdown	H_2 Shutdown	H_2 Shutdown
Week 17 (April 25 - May 1)	H_2 Shutdown	H_2 Shutdown	Laser Growth	Laser Growth	Laser Growth	Laser Growth	No Growth

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