**Course Syllabus**

**ECE 156A  Digital Design with VHDL and Synthesis  (Elective)  4 units**

**Catalog Description:**
Introduction to VHDL basic elements. VHDL simulation concepts. VHDL concurrent statements with examples and applications. VHDL subprograms, packages, libraries and design units. Writing VHDL for synthesis. Writing VHDL for finite state machines. Design case study.

**Prerequisites:**
ECE 152A with a minimum grade of C-.

**Text, References, and Software:**

Text:

Advanced Digital Design with the Verilog(TM) HDL, by Michael D. Ciletti  
Publisher: Prentice Hall; Book and CD-ROM edition (August 13, 2002)  
ISBN: 0130891614


Software:

ModelSim, by Mentor Graphics Corporation  
Design Compiler, by Synopsys, Inc.

**Topics Covered and Course Goals:**

1. Modern Design Methodologies for Digital Systems  
   1. Understand basic design flow  
   2. Understand design issues and challenges  
   3. Able to use a logic simulator to verify a small design

2. Basic Synthesis Concepts and Logic Minimization  
   1. Understand synthesis flow  
   2. Comprehend the concepts in 2-level logic minimization

3. Using Verilog to Design Digital Systems  
   1. Understand Verilog features and constructs  
   2. Able to use structural and behavioral Verilog to model various designs

4. Verilog Synthesis  
   1. Understand basic synthesis process and related issues

**Class/Laboratory Hours:**
Lecture, 3 hours; laboratory, 3 hours.
Contribution to Criterion 5

Contributes to the one and one-half year of engineering topics, primarily engineering design.

Contribution to Program Outcomes:

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Prepared by: Li-C. Wang                         Date: Jan 8, 2008