Course Syllabus

ECE 156B  Computer-Aided Design of VLSI Circuits (Elective)  4 units

Catalog Description:
Introduction to computer-aided simulation and synthesis tools for VLSI. VLSI system design flow, role of CAD tools, layout synthesis, circuit simulation, logic simulation, logic synthesis, behavior synthesis and test synthesis.

Prerequisites:
ECE 156A with a minimum of C-

Text, References, and Software:

Text:
Advanced Digital Design with the Verilog(TM) HDL, by Michael D. Ciletti
Publisher: Prentice Hall; Book and CD-ROM edition (August 13, 2002)
ISBN: 0130891614


Software:
ModelSim, by Mentor Graphics Corporation
Design Compiler, by Synopsys, Inc.

Topics Covered and Course Goals:

1. Modern Design Automation Flow for Digital Systems
   1. Understand electronic design automation flow
   2. Understand design challenges
2. Synthesis and Verification
   1. Understand advanced concepts in functional and logic verification
   2. Comprehend the concepts in multi-level logic minimization
   3. Experience synthesis and verification in a design process
3. Fundamental synthesis and verification algorithms
   1. Understand fundamental algorithms used in synthesis and verification such as SAT and OBDD
   2. Experience state-of-the-art SAT and OBDD tools
4. Emerging design issues
   1. Understand emerging design issues in the industry

Class/Laboratory Hours:
Lecture 3 hours; Laboratory 3 hours.

Contribution to Criterion 5
Contributes to the one and one-half year of engineering topics, primarily engineering design.

Contribution to Program Outcomes:

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Prepared by: Li-C Wang                  Date: Feb 15, 2008