Errata for the Dally/Poulton "Digital Systems Engineering" Text.

This list compiled by Fred Rosenberger (fred@cse.wustl.edu, http://www.cse.wustl.edu/~fred) as an aid to anyone using the Dally/Poulton text. I expect some of the "errors" reported here are misunderstandings or misconceptions on the part of myself or the person reporting them so use with caution. Additions and corrections to this list welcomed.

First: This is a very good text/reference. Lots of higly relevant material, broad coverage, authoratative. I have used it in CoE464 because I believe it is the best available text.

PAGE	Cm from Page Top	Original Text		Reported By	Date (Warning, not Y2K compliant
52	Table 2-3		RG-178B/U and M17/133 have the same impedance and velocity but different pf/m. Not possible.	FUR	Jan-6-99
83	Eq 3-7	d	should be s to correspond to Figure 3-2(e)	E464 Class Spring 1999	Jan-30-99
84	Table 3-2		Values in this table differ from those on inside front cover by more than just rounding	FUR	Jan-6-99
93	Eq 3-32, 3-36, …	3-32 has I_r = V_r/Zo but later is I_r = - V_r/Zo	Either can be correct depending on the definition of I_r but it should be consistent. The first form goes with I_r being defined as positive for current from right to left.	FUR	Jan-23-99
95	Fig 3-8	Has V_i and I_f	Not consistent. Seems both subscripts should be i (incident) or f (forward) Same for other equations. Also seems that either i or f should be used throughout, not a mixture (unless there is hidden distinction that I miss).	FUR	Jan-23-99
104	last line	"a 5-mil copper stripguide"	Is this stripline or microstrip? 0.5oz or 1oz, width, spacing, …? Stripguide is not in the index and I am not sure what geometry is meant here	FUR	Mar-12-99
105	Fig 3-19	30 AWG Pair (two places)	24 AWG Pair	FUR	Jan-23-99
271		1. Wiring ground rules …	<- Wiring rules … ground rules in the original has two interesting meanings, ground as in 0 potential, and ground rules as in baseball. I spent time figuring out which was intended and the word ground really adds nothing here.	FUR	Mar-12-99
276	Tbl 6-3		Please give units (C, L, …) in table, not just in text. Also please give meaning of asterisk in table, not just text	FUR	Mar-12-99
276	3nd last line	"all dimensions are in mils"	This only matters if the conductors have specific thickness, otherwise only ratios matter and units could be anything. Line thickness is not given, is it 0.5 oz?	FUR	Mar-12-99
276	Tbl 6-3	C and Cm	On page 110 capacitance is specified in Cs and Cc	FUR	Mar-12-99
277	15.8	"are grounded at one end"	This depends on the type of coupling but I believe for high speed digital signals this should be "are grounded at both ends" assuming the shield has its ends close to the ends of the shielded wires.	FUR	Jan-30-99
279	Fig 6-15		R2 cannot change when A1 does, this would be 0 prop delay. Direction of change also is suspect. Finally, it's the voltage across the termination resistors that matters and this is not calculated or shown. This really should be analyzed from the viewpoint of coupled lines	FUR	Mar-12-99
298	3rd line before 6.7	"made on a statistically significant sample of channels …"	Seems covering the range of allowed fab parameters is more important than number of samples. Noise components such as offsets are not random, and there is no number of samples that is gaurenteed to reasonably cover the range without more info	FUR	Mar-12-99

308		Section 7.1.1: Calculation of PD for CMOS case may be misleading.	With 50% duty cycle, max PD with 200 Ohm output R is: 0.5*V^2/R = 0.5*3.3^2/200 = 27mW, much less than the 130mW given in 7.1.1. This is partially due to the fact that the circuit can't switch at 100MHz. Of course limitation to less than 100 MHz is a big disadvantage. Output R could be set to 50 Ohms with wider FETs, this would allow operation at 100MHz and would increase max PD to 108mW. This 108mW is still a little still less than the 130mW calculated in 7.1.1 because the round trip delay of the example is 12ns, longer than the period between data changes. Once the round trip delay is longer than the period between data changes, no additional power is required to increase the data rate. Note that if data value changes infrequently PD for the full-swing CMOS can actually be lower than LSC case. Random data would have a transition every other cycle on the average and PD of 54mW.	FUR	Jan-7-99
309	Tbl 7-3		From page 307, offset is +/-10mV and sensitivity is 10mV. This should give Vih and Vil of +/-15mV.	FUR	Mar-12-99
311	2nd line before 7.1.3	"because most CMOS drivers do not …"	But they could. Does not seem fair to give advantage to LSC here because CMOS could do this also.	FUR	Mar-12-99
312	2nd line 7.1.4	"Yet it is far from optimal in almost any application	It is optimal in number (or area) of components	FUR	Mar-12-99
318	Fig 7-7		Both parts of the Figure are labeled (a)	FUR	Mar-12-99
319	Fig 7-8		Ir could be reduced for unipolar signaling to improve its performance. The two schemes would then be about equal (with illustrated values).	FUR	Mar-12-99
323	Fig 7-13		This might be drawn closer to the form in Fig 7-4 to make correlation between the Figures easier.	FUR	Mar-12-99
329	4th line from bottom		In some ECL based CRAY computers, unused outputs (ECL has two complemtry outputs) were terminated just to keep the current approximately constant when switching	FUR	Mar-12-99
331	2nd line	"it is better to model …"	Seems its *easier* to model as lumped circuit, but more accurate to model as distributed.	FUR	Mar-12-99
349	Fig 7-41		Is Vrs consistently defined in the text. Seems somewhere its defined as half that in Fig 7-41?	FUR	Mar-12-99
510	19.8	Rosenburger	Rosenberger	FUR	Feb-15-99
648	15.7	Rosenburger	Rosenberger	FUR	Jan-6-99
659	21.1	Stackup, 44	Stackup, 41	FUR	Jan-6-99
Inside back cover			Equation for wire over ground plane capacitance needs 2 added in numerator. Equation for Zo needs 2 added in denominator.	FUR	Feb-06-99
388	Fig 8-32	Legend to right of middle plots refers to solid and dashed but both traces are solid		Dan Lenoski, Growthnetworks Inc.	Mar-26-99
437	Fig 9-38		Clock adjust block should show clock input	FUR	Apr-3-1999
440	Fig 9-42		Clock adjust block should show clock input	FUR	Apr-3-1999
469	2nd Par in 10.2.2.2		Dealing with noise its necessary to consider an ensemble of events, not a single isolated event. I don't understand the last sentence. It can be shown that including noise for ensemble of events gives approximately same result as noise free case	FUR	Apr-3-1999
469	3rd Par in 10.2.2.3	"The value of delV1 is uniformly distributed between 0 and 1"	This is a safe bound on the initial voltage (but should be -Vdd and Vdd, not 0 and 1) but is very conservative.	FUR	Apr-3-1999
470	Table 10-1		Does not give tau_s	FUR	Apr-3-1999

470	line 11	"one clock period less tdCQ, t_w approx 10ns	A Figure is needed for at latch (or flop) showing the definition of t_w. When does this period start? At clock edge, or t_dCQ after clock edge? Also, setup time should be subracted from clock period since valid value is required at second flop input a setup time before clock	FUR	Apr-3-1999
471	5th line from bottom	tau_r	should be tau_s	FUR	Apr-3-1999
472	2nd Par		Reference Flannagan (JSSC Aug 85, pp880-882, sc-20, no 4) which shows optimum tau_s is obtained with equal width N- and P-FETS.	FUR	Apr-3-1999
477	13th line from bottom	"places the keep-out region into the receiver's"	Sentence is garbled.	FUR	Apr-3-1999
104	last line	"5-mil copper stripguide"	w and h are given but not s. Is this 50 Ohm impedance? Configuration?	FUR	Apr-3-1999
226	first line		change "drops" to drop	FUR	Apr-16-1999
232	6th line		change "increase" to "decrease"	FUR	Apr-16-1999
405	line 2		Change "BC" to "AC"	EE464 De Alwis	Apr-16-1999
418	Sec 9.5.2, next to last line		"Two-Phase clocking is the most common ..." In what context? Not at PC board level. Not in edge-triggered ASIC design. Not in FPGAs. Unless we look inside flops at their internal structure.	EE464 De Alwis	Apr-16-1999
369	Fig 8.16, Eq 8-9		I_b is used twice, once for the bias current sources (in figure), once for the difference output current (delta-I_b in Eq 809)	EE464 De Alwis	Apr-16-1999
326	Eq 7-15 and 7-16		both lower case and upper case B is used in subscripts but it seems they should all be the same.	EE464 De Alwis	Apr-16-1999
329	13.2cm	"twice the noise margin"	Should be more than twice the noise margin if drive is doubled and receiver sensitivity stays the same.	EE464 De Alwis	Apr-19-1999
329	14.2cm	"rise- or fall-time affecting … half the transistion time"	This could be stated more clearly: dv/dt is twice …	EE464 De Alwis	Apr-19-1999
511	Prob 10-1		tau_r should be tau_s. Why is t_dCQ included (see comments about page 470)? t_a is not given (could be determined if rise time were given)	EE464 Hussain	Apr-19-1999
307	line 7		2x3.3mA/50Ohm should be 2X3.3mAx50Ohm	EE464 Hussain	Apr-19-1999
468	second line after Eq 10-1	K_s=I/C approx 1/t_a	Where does this come from? It at least needs a reference or an explanation. This is approximately the value for any delay (t_dCQ, t_s, t_h, …)	FUR	Apr-19-1999
469	Eq 10-3		log(del-V_1) does not have correct units. Should be log(del-V_1/1V). Although the actual value of voltage used (1V in this case) is not very important in overall reliability calculations, carrying it along in the calculations makes the understanding and checking much easier.	FUR	Apr-19-1999
Chapt 12			Chapter 12 on timing circuits could include a section on design of (and analysis of) flip-flop metastability parameters. How to design flops for good resolving time. Use Flanigan (sp?) ref and others.	FUR	Apr-19-1999
399	line 3		"loop has low bandwidth, it is unable to track and cancel the high-frequency jitter." If clock to clock jitter is independent then there is no loop bandwidth that would cancel jitter.	FUR	Apr-19-1999
399	Eq 9-1		This equation should include t_dCQ. Clearly t_dCQ has the same effect as wire delay in series with the transmit flop output so it must be part of the equation.	FUR	Apr-19-1999

363	line 7		Figure 8-8 should be Figure 8-7	EE464 Hussain	Apr-19-1999
460	Prob 9-7		"Table 9-7" should be Table 9-9. Table 9-9 at top of page should refer to problem 9-7, not Figure 9-7.	FUR	Apr-19-1999
back cover			k_r in reflection coefficient is lower case k, but in Eq 3-38 reflection coefficient is upper case K (but lower case in Eq 3-37)	FUR	Apr-19-1999
482	Fig 10-17		This seems to have a synchronization problem in the flops just after t_m. If the value of xp is changing from 010 to 001, then sdxp might be: 000, 010, 011, or 001. Two of these are ok, two are not and must be detected and dealt with.	FUR	Apr-19-1999
General			A glossary of terms, and more importantly symbols, would be a great help to the reader. Also it would help eliminate multiple symbols for the same parameter (k vs K for reflection coefficient, tau_r vs tau_s for metastability time constant, …)	FUR	Apr-19-1999
308	5th line from bottom	"noise immunity"	What is definition of noise immunity?	FUR	Apr-26-1999
398	Fig 9-2	"RxClk-to rest of receive chip'	Why take from indicated position? Phase is unknown with respect to data flop clock.	FUR	Apr-26-1999
407	Eq 9-13		Reverse -t_ao and +t_ao in first two lines	De Alwis	Apr-26-1999
95	below eq 3-36	"Telegrapher's equation"	Poon and others call eq 3-26 the telegrapher's equation. Matick does not refer to it. I think common usage is that eq 3-26 is the telegraphers equation, not 3-36	FUR	May-08-1999
364	8.2.2 caption	"Equalization … "	"equalization" is not in the index	FUR	May-08-1999
469	line 2	"to attain unit voltage"	I realize that it makes little (actually no) practical difference, but the use of unit voltage here causes the units to get lost (e.g. units in eq 10-3 don't balance as you can't take the log of Volts. It would become ln(delta_V1/Vdd)). Use of Vdd, rather than unit voltage has a lot of pedagogical advantages including units, scaling to different voltages, etc.	FUR	May-08-1999
469	eq 10-3		Use of log for log_base_e is mildly confusing sometimes (I think this happens other places in text also). Many texts use ln for log_base_e and log for log_base_10. Seems a little safer and conventional.	FUR	May-08-1999
319	Par. 2	"Bipolar signalling reduces power ..."	Peak current is 1/2, but current is required 100% of the time rather than 50% so total power is the same	FUR	Mar-01-2000
469	7th line from bottom	"uniformly distributed between 0 and 1"	This needs significantly more justification and rationalization.	FUR	Mar-14-2000
582	next to last par	"edge-triggered flip-flop"	latch	FUR	Mar-14-2000
122	Fig 3-32		Explicit representation for ground(s) would help here	FUR	Mar-14-2000
297	Line 123	"gross noise margin"	In text gross noise margin is delta-V/2 - V_N. In Lecture notes 6, slide 14, gross margin is delta-V/2, are these supposed to be the same or are we to have two gross margins (one with "noise" as part of name)?	De Alwis	April-26-2000
470	10.2.2.4, second last line	2.59*10^-17	2.59*10^17	Scott Moran	April-08-2001
407	line 4	t_dDQ	t_dCQ	Karen Ng	April-04-2002

437	Fig 9-38		I don't think this phase comparator works as shown. Would give 1/2 Vdd as filtered value. Text at end of paragraph says 9-38 is identical to 9-2, but 9-2 has two flops and an ex-or for the phase comparator.	FUR	April-09-2003
83	Eq 3-7	we/s	w eps/s (error created in fixing earlier error)	Teddy Lee	Feb-4-2003
Inside Back cover	microstrip formula		C should be: eps*w/s +2*pi*eps/(ln(2*s/*h/2))	FUR	Feb-4-2004
Inside Back cover	wire over ground plane		For Zo, the pi in the denominator should be 2*pi	FUR	Feb-4-2004
Inside Back cover			In equation for parallel plate characteristic impedance, the W should w (lower case) to correspond to the Figure	FUR	Feb-4-2004
106	Eq 3-56		epsilon_k <- epsilon_r	Joseph Lancaster	Mar-2-2004