On Chip Power Distribution

* CMOS Devices have very uneven power draw $\Rightarrow I_{peak} >> I_{avg}$ for typical design.

E.G. Consider a $0.35\mu M$ inverter driving 2 other inverters w. $200\mu M$ of wire:

$\omega_p = 4\mu m \quad \omega_n = 2\mu m$ Total load ~ 62fF

$V_{cc} = 2.0V \Rightarrow Q_{ch} = C_L \cdot V_{CL} = 124\,fC$

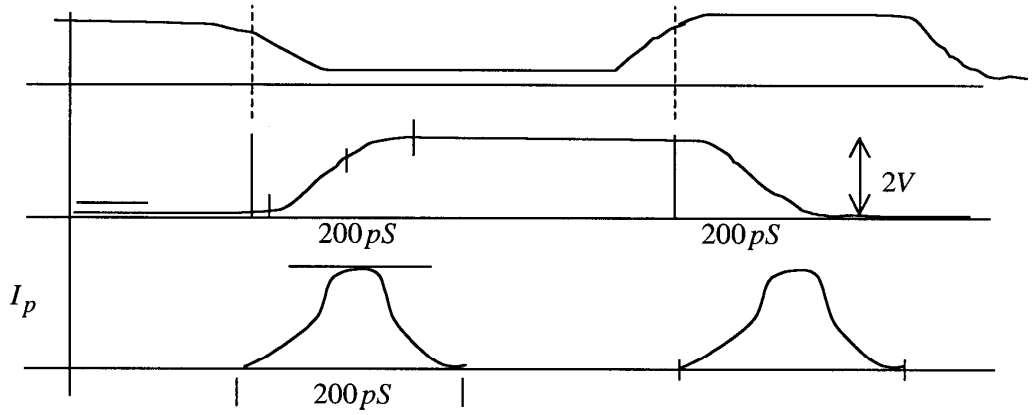
Given $R_{chN} \sim 10K\Omega /\ @\ 0.35\mu m = L$

we get: $1.14mA$ peak current (I_{dsat})

$$\Rightarrow T_R = 100pS$$

given input rise time of $200pS$ we expect ~ $200pS$ 0-90% rise as well, similar fall since 2x width. (Actual = $240pS$)

Wave forms:



On Chip Power Distribution

Typical current pulse is triangle with base $= 2T_R = 2T_F$.

peak current is convolution of input rise/fall and output rise fall:

$$I_{peak} = \begin{cases} 0.75 \; I_{dsat} & t_{in} \approx t_{out} \\ 1.0 \; I_{dsat} & t_{in} << t_{out} \\ 0.5 \; I_{dsat} & t_{in} >> t_{out} \end{cases}$$

- On the other hand $I_{avg} = \dfrac{K \cdot Q_{sw}}{t_{clk}} = K \cdot C_L \cdot V_{dd} \cdot f_{clk}$

  where K is the switching probability.

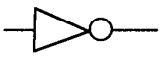
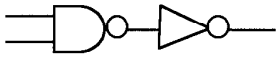
- Larger Logic blocks:

  For larger logice, the peak current depends on the gate topology. RAM's have 2 peaks, 1 for decode, 1 for read/1 write buffering decode.

Typically for multistage fast logic, each stage is equalized in delay so that we can often approximate the ensemble peak current by a triangle for each stage.

On Chip Power Distribution

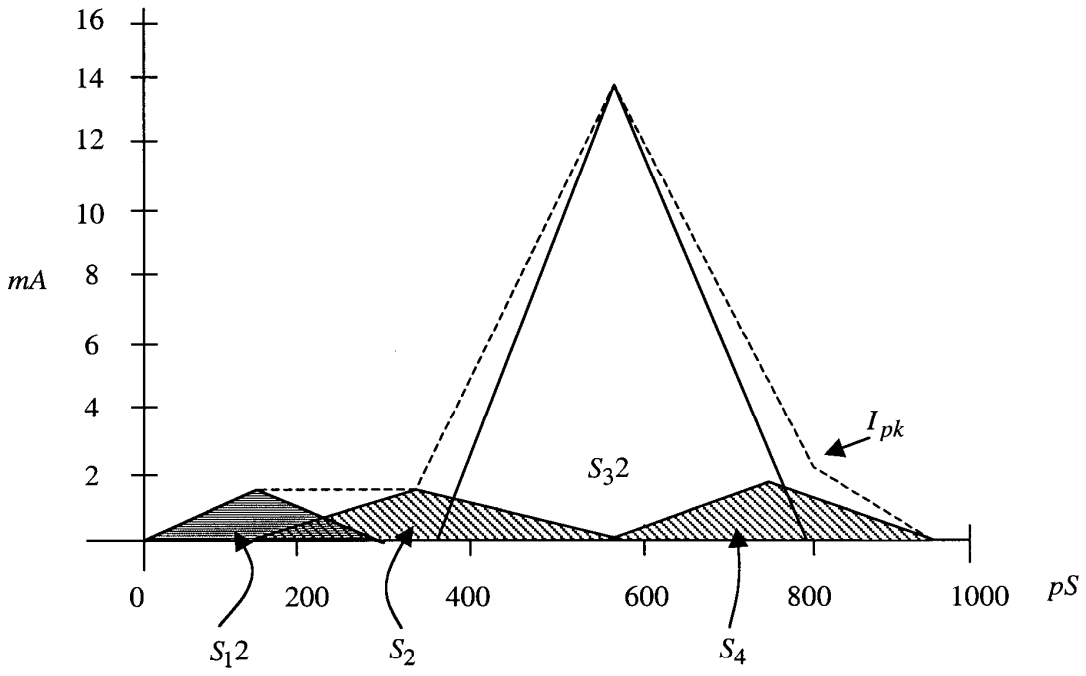
Eq: 1-64 decoder: $0.35\mu m$

Stage 1	Stage 2/3	Stage 4
6 inverters 1/0.5	2-4 decode 2/2 14/7	4/6 4/6
		
6x 6 switch	12x 3 switch	64x 1 switch

* note: only a small number of 2 & 3 will be active.

STG	*N*	*S*	L_L	C_T	C_Q	t_r	I_{pk}
1	6	6	18f	108f	0	153p	1.9
2	12	3	46f	138f	414	201p	1.9
3	12	3	350f	1050f	3150	218p	13.4
4	64	1	100f	100f	6300	217p	1.3

C_Q is "Quiest" load, those that didn't switch…



On Chip Power Distribution

* Random Logic Case

Eq: $N_a = 50{,}000$ gates $C_L = 100fF$ /gate (0.35m)

$d = 10$ levels, assume $2K_s$ switch each cycle

(K_s switch in each direction...)

$N_s = K_s \cdot N_G$ in one direction, equalize delay/stage

Triangular stage peak as before:

$$N_i = \text{number of switching in stage } i = \begin{cases} \dfrac{4N_{si}}{d(d+2)} & i \le d/2 \\ \dfrac{4N_s(d-i)}{d(d+2)} & i \ge d/2 \end{cases}$$

$$I_i = \text{current in stage } i = \frac{N_i C_L V_{cc}}{t_r}$$

So for our example: $K_s = 0.25$ $N_s = 12{,}500$

$$N_i = 2{,}083 \quad \Rightarrow \quad I_p \cong 2.9A$$

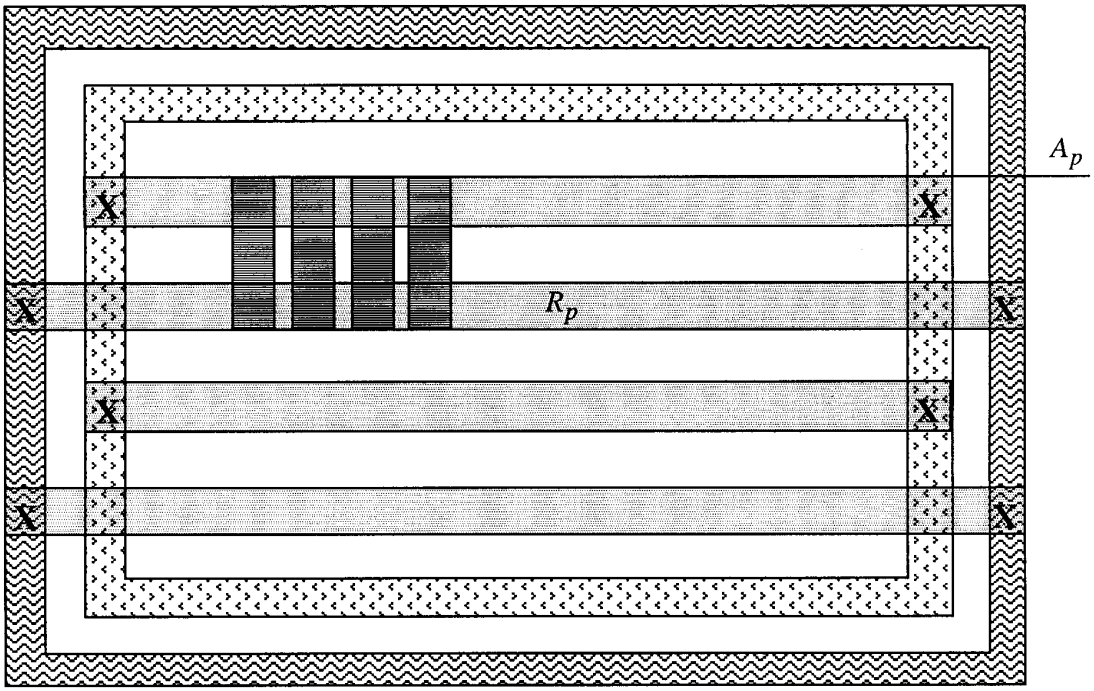
for $t_{ck} = S_n S$ $I_{Au} = 624mA$

* Note: we must assume worst case pattern in estimate of K_s for pour design! $\Rightarrow$ else will "work" sporadically!

On Chip IR Drop

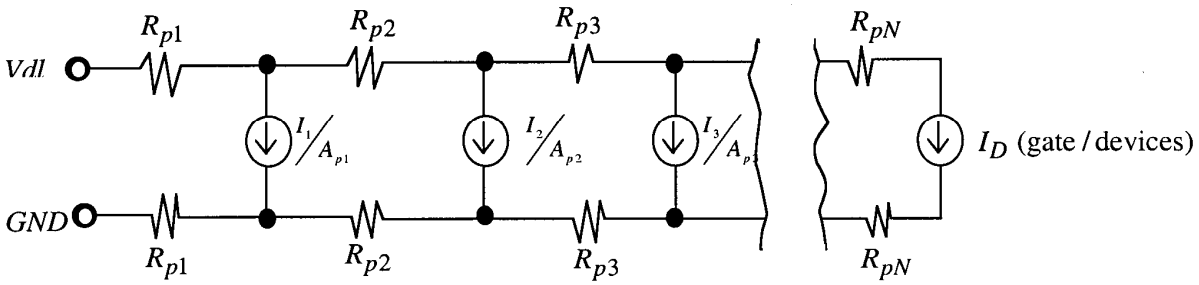
On Chip IR Drop

Assume that the power grid is a hierarchy of wires with essentially zero resistance at the periphery:

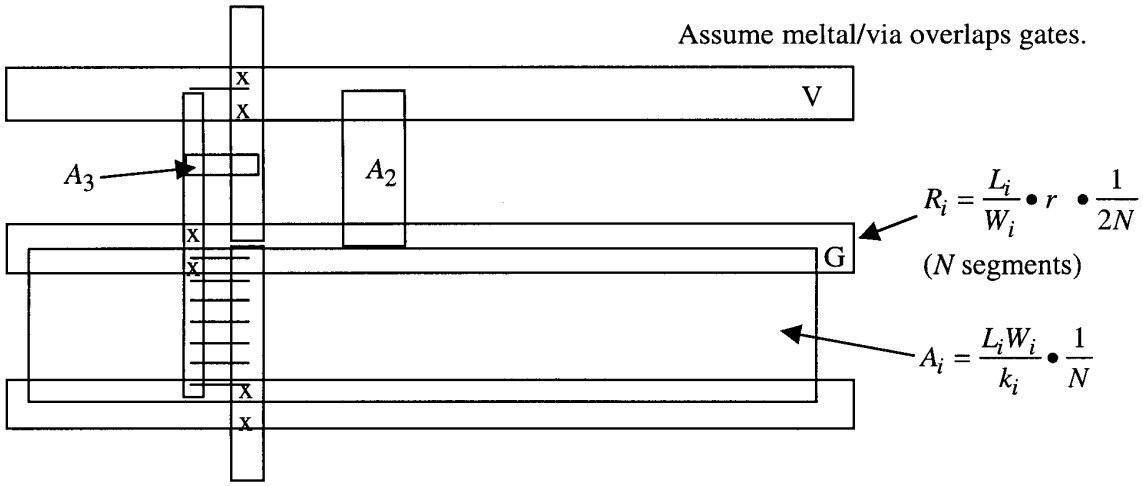


Assuming periphery has near zero resistance (pods)

Resisting of metal layer is constant: $R = 0.04\Omega$ / @ $1\mu m$ A
Via = 1Ω ($0.35\mu m$)

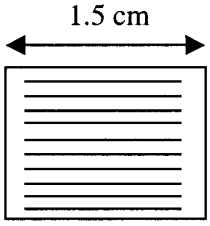


On Chip IR Drop



k_i=fraction of metal level devoted to power of 1 side:

Eg:



$L_p = 15mm$ $\quad K_p = 0.375 = \left(\frac{30}{80}\right)$

$W_p = 30\mu m \quad \Rightarrow \quad N = 187$

pitch $= 80mm$ $\quad A_p = 1.2mm^2$

(note: A_p counts area for N = # of pairs of N, P)

* Peak Current Drawn by a segment $\Rightarrow$ Peak current of supplied area.

@ $0.35\mu m$: 4 K gates/$(\mu m)^2$ $K_{sw} = 0.25$ we get ~ $0.26A/mm^2 = J_{pk}$ and

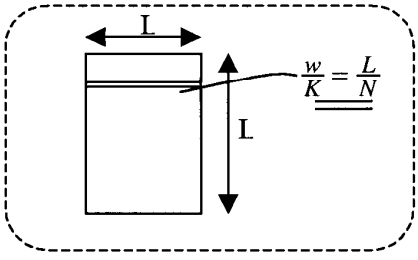
$J_{avg} = 56mA/mm^2$

$\Rightarrow$ Peak/segment = $J_{RR} \cdot A_1 = \frac{0.31A}{N}$

Each Segment has current = sum of all lower sources

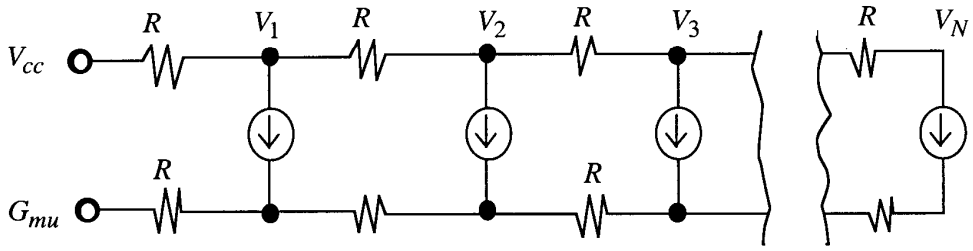
if we assume that K_p = width/pitch ration is constant for all levels hierarchy:

i.e., Aspect ratios of each segment is same $\Rightarrow$



$\Rightarrow$ all Resistors are equal.

On Chip IR Drop



$$V_1 = R \bullet J_{RK} \circ A_1 \qquad \text{(voltage drop)}$$

$$V_2 = V_1 + R \cdot J_{pk} \cdot A_2$$

$$V_i = \sum_{j=1}^{i} R \cdot J_{pk} \cdot A_j = \sum_{j=1}^{i} J_{pk} \cdot \frac{L_i}{W_i} \cdot \frac{r}{2N} \cdot \frac{L_i W_i}{K_i N}$$

$$= \sum_{j=1}^{i} J_{RR} \cdot \frac{L_i^2 r_{\square}}{2N^2 K} \qquad \text{as segments} \Rightarrow \infty$$

$$V_{drop} = \sum_{j=1}^{N|2} J_{pk} \cdot \frac{L_i^2 r_{\square}}{2N^2 K} \qquad V_{drop} = \int_{\circ}^{½} \frac{J_{pk} \cdot r\, x}{kp} d_x = \boxed{\frac{J_{pk} r_{\square} L^2}{8kp}}$$

So for $0.35\mu m \Rightarrow J_p = 0.31A / rm^2$ $r_D = 0.04$ $L = 15mm$ $k = 3/8$ $V_{drop} = 0.3V$

$\Rightarrow$ Total Drop = $\boxed{0.6V}$! **note:** only can reduce if use thicker wire or more of layer.

* Thicker top level wire $\Rightarrow R_j \rightarrow$ reduced.

* Chip pods across area of dil. $\Rightarrow$ use wire in p.c. board.

* On-Chip bypass

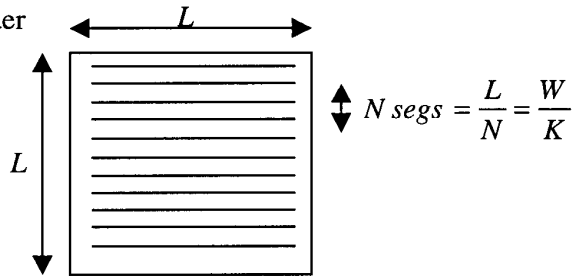
On Chip IR Drop

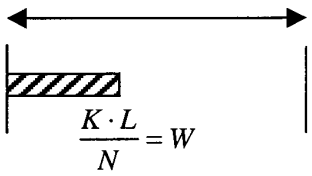
Metal Migration:

Worry sets in @ $1mA/mm^2 = (10^9 A/m^2)$

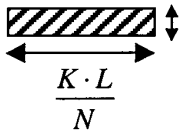
so average current must be distributed on sufficient metal

Consider





$$\text{Current/segment} = J_{AV} \bullet L \circ \frac{L}{N} = J_{avg} \bullet \frac{L^2}{N}$$

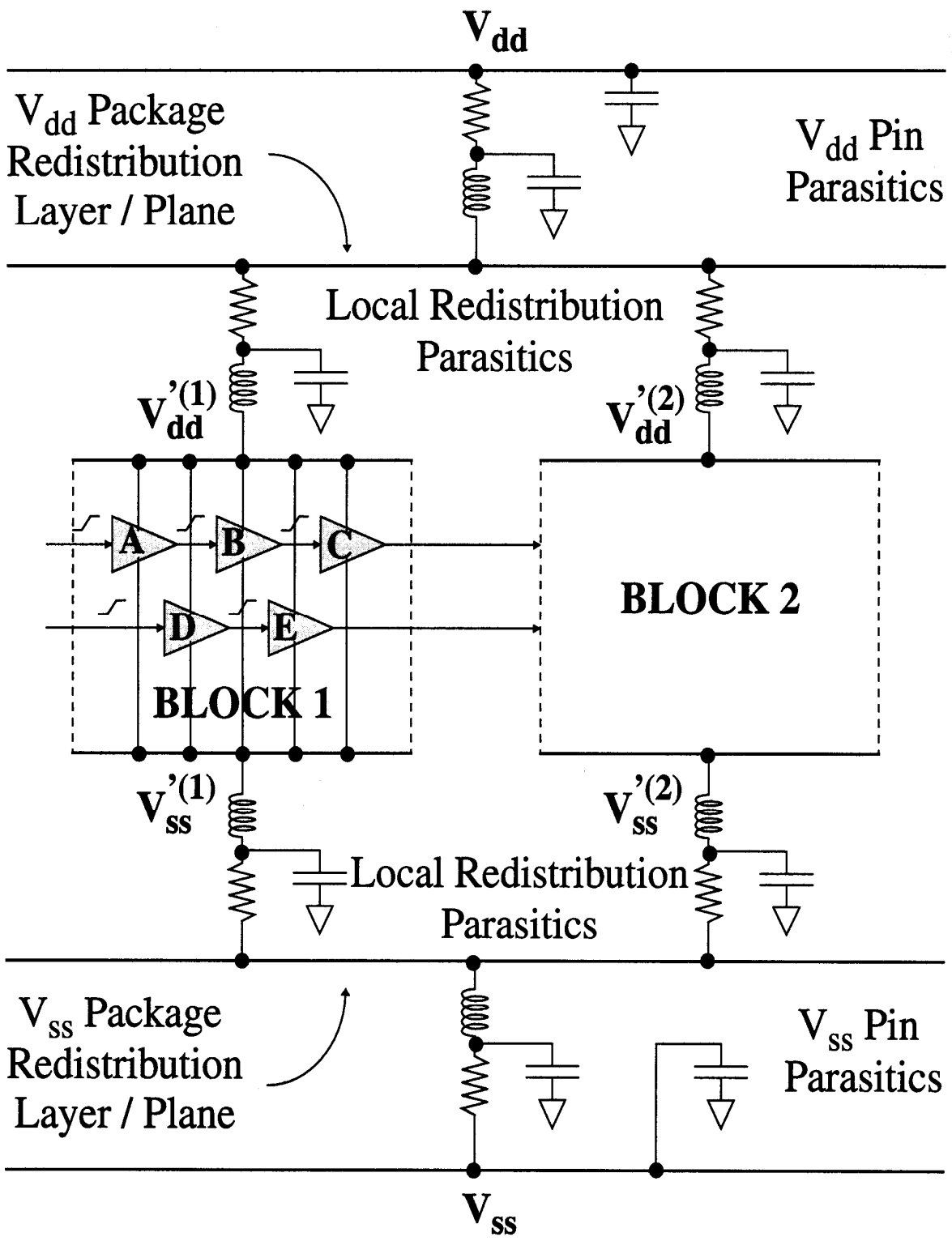
Area of wire $\Rightarrow$ 

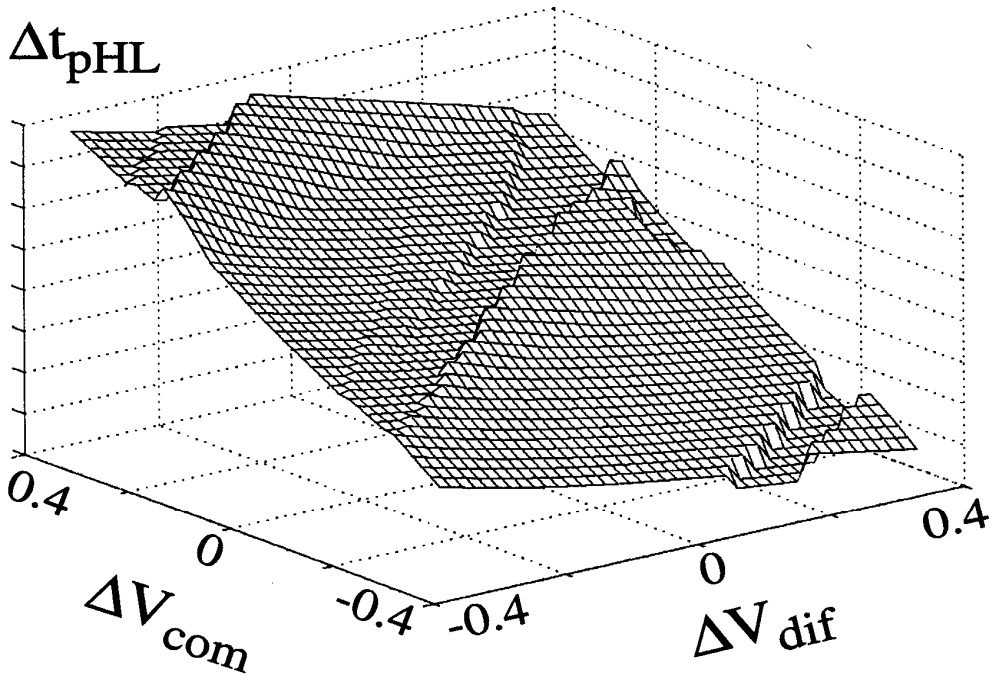
$$H = \frac{H \cdot K \cdot L}{N}$$

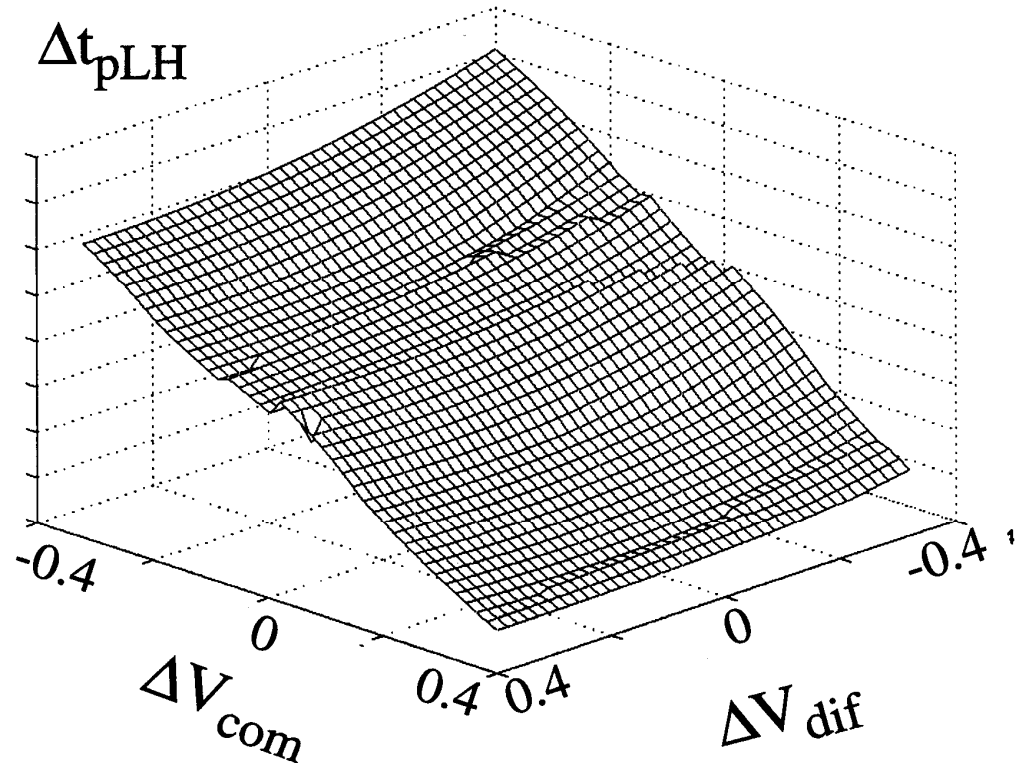
$\Rightarrow \frac{1}{2}$ current for each side $\Rightarrow$ current/area $= \frac{J_{AV} \cdot L^2}{2N} \bullet \frac{N}{HKL}$

$$\frac{10^3}{mm^3} \geq \frac{J_{AV} \cdot L}{2Hk} \qquad \Rightarrow \qquad K \geq \frac{J_{AV} \cdot L}{2H} \cdot 10^{-3}(mm)$$

Eq: $K \leq 0.45$ @ example.


V_{dd}
V_{dd} Package Redistribution Layer / Plane
V_{dd} Pin Parasitics
Local Redistribution Parasitics
$V'^{(1)}_{dd}$
$V'^{(2)}_{dd}$
A
B
C
D
E
BLOCK 1
BLOCK 2
$V'^{(1)}_{ss}$
$V'^{(2)}_{ss}$
Local Redistribution Parasitics
V_{ss} Package Redistribution Layer / Plane
V_{ss} Pin Parasitics
V_{ss}


Δt_{pHL}
0.4
0
-0.4
ΔV_{com}
-0.4
0
0.4
ΔV_{dif}


Δt_{pLH}
-0.4
0
0.4
ΔV_{com}
0.4
0
-0.4
ΔV_{dif}

Parameter					0.25μm						0.18μm					
					Simulation		Our Method				Simulation		Our Method			
W_p/W_n (μm)	C_L (ff)	t_r (ps)	ΔV_{dd} (volt)	ΔV_{ss} (volt)	Δt_{pHL} (ps)	Δt_{oT} (ps)	Δt_{pHL} (ps)		Δt_{oT} (ps)		Δt_{pHL} (ps)	Δt_{oT} (ps)	Δt_{pHL} (ps)		Δt_{oT} (ps)	
10/5	100	100	-0.250	-0.250	-21.93	-4.198	**-21.23**	**3.2%**	-4.849	15%	-24.94	-10.71	**-24.50**	**1.8%**	-12.87	20.1%
10/5	100	100	0.00	-0.100	-4.729	0.169	**-4.694**	**0.7%**	0.167	1.1%	-6.224	-2.943	**-5.970**	**4.0%**	-2.598	11.9%
10/5	100	100	0.025	0.100	5.402	0.421	**5.644**	**4.5%**	0.418	0.7%	6.950	2.955	**6.927**	**0.3%**	3.138	6.2%
10/5	100	100	0.100	0.00	3.760	2.043	**3.800**	**1.0%**	2.007	1.8%	3.708	2.680	**3.828**	**3.2%**	2.893	8.0%
10/5	20	50	-0.500	0.025	-6.045	-1.683	**-5.701**	**5.6%**	-1.768	5.1%	-8.085	-6.923	**-7.802**	**3.5%**	-6.238	9.9%
10/5	20	50	0.500	0.100	8.599	2.715	**8.195**	**4.7%**	2.525	7.0%	9.729	1.551	**10.22**	**5.0%**	1.472	5.1%
5/5	100	100	0.250	0.100	14.13	5.366	**14.35**	**1.6%**	4.926	8.2%	17.30	3.639	**16.46**	**4.9%**	3.139	13.7%
5/5	100	100	0.500	-0.025	16.47	10.15	**17.04**	**3.4%**	10.24	0.8%	19.15	7.701	**18.06**	**5.5%**	7.185	6.7%
5/5	100	50	0.025	-0.250	8.294	-4.856	**8.686**	**4.7%**	-5.137	5.8%	8.524	1.677	**8.945**	**4.9%**	1.467	12.5%
10/10	100	100	-0.250	0.050	-4.694	-10.08	**-4.644**	**1.1%**	-11.78	16.8%	-4.733	-2.203	**-4.491**	**5.1%**	-2.273	3.2%

Table 1: Validation of expressions for incremental buffer delay and slope changes

$$\Delta t_{phl} = K_1 \cdot \Delta V_{com} - K_2 \cdot \Delta V_{diff}$$

$$= K_1 (\Delta V_{dd} + \Delta V_{ss}) - K_2 \cdot (\Delta V_{dd} - \Delta V_{ss})$$

$$K_1 \cong \frac{t_r}{2V_{dd}(1+\alpha)} + \frac{C_L}{2I_{D0}}$$

$$K_2 \cong \frac{t_r}{2V_{dd}(1+\alpha)} - \frac{C_L}{2I_{D0}}$$

$K_1 > K_2$ for most tech nologies

I_{D0} = Sat current @ $U_{DS} = U_{GS} = V_{dd}$

α = velocity SAT index : $\alpha \sim (1 - 1.2)$ typical CMOS