Speed Optimization of Edge-Triggered Nine-Transistor D-Flip-Flops for Gigahertz Single-Phase Clocks

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Abstract - An analysis is performed on one of the recently published D-flip-flops to show the conflicting nature of the requirements for sizing each transistor in a digital circuit. The decision process is complex because the electrical parameters such as gate capacitance and drain current of a MOS transistor are functions of terminal waveforms which change rapidly with time, and are different from one state-transition to another. A better understanding of the operation of such digital circuits during each state-transition helps both the human designer and the computer tool to reach a better compromise in shorter design time. It may also lead to improvement in the circuit configuration, once the speed bottlenecks are identified.

A new D-flip-flop configuration is presented which enables gigahertz clock speeds to be easily achieved for 2-μm and 1.5-μm standard CMOS technologies.

Introduction

The clock speed of CMOS integrated circuits has been steadily increasing in the last decade, from the megahertz range in the early eighties to the hundred megahertz range today [1]. Continuing progress in fabrication technology has resulted in ever smaller feature sizes, which is one of the most important factors that affect the circuit speed. Improvement of clocking strategies and clock distribution also plays an important role in improving the overall speed of a digital system.

Recently, circuit techniques which dramatically improve clock speed have been the focus of many excellent studies [2,3]. Many digital circuit cells are designed to use a single-phase clock [4]. In designs aided by computer tools [5,6], clock speeds up to even 1GHz have been achieved for the type of D-flip-flop (DFF) shown in Fig.1a using 2-μm standard CMOS technologies. Such an achievement is a clear demonstration of the benefit of better understanding of circuit structures and that of computer aids in improving clock speed.

In the following, we shall further study the structure of the DFF in Fig.1a and illustrate the trade-offs in the design process. reconfiguring the transistors in Fig.1a results in a new DFF structure in which the conflicting requirements for sizing each transistor can be better reconciled and higher speed can be achieved.

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Sizing Transistors for Maximum Speed

Digital circuits such as the Toggle-flip-flop (T-FF) shown in Fig.1b typically consists of inverter-like structures chained in a feedback loop. Most transistors in such circuits are therefore drivers and loads at the same time. The loading a transistor presents and the drive current it delivers are rapidly changing functions of the transistor's terminal voltages. This makes it difficult for the designer to recognize the dimensions of each transistor that would result in the optimal performance (speed) of the overall circuit. Linearized transistor models, while useful for enabling a computerized optimization, usually do not reflect the dependence of electrical parameters on time. Computer aids can therefore be more effective when they are combined with at least some form of qualitative reasoning, so that the designer's insight into how the circuit can be improved is not lost as a result of over-reliance on computer aids.

Consider the sizing of the transistors in Fig.1b. In a toggle configuration, the D flip-flop output is periodic in two periods of the input (clock). There are thus four possible state-transitions, as shown in Fig.2, in which different transistors charge and discharge node capacitors to produce new node voltages. The best transistor dimensions are those which maximize the slowest state-transition, so that the clock (input) period can be minimized.

To appreciate the requirements of each state-transition of the transistors, arrows and crosses are used in Fig.2a - Fig.2d to indicate whether a driver transistor should be wider, a load transistor should be narrower, don't cares or indeed conflicting requirements because the transistor in that transition is both a driver and a load. An arrow or bar next to a node voltage, y_1 or y_2, indicates whether the voltage on that node should rise, fall or stay unchanged. Transistors that are turned off during a particular state-transition are removed from each circuit diagram to facilitate the analysis of the rest of the circuit, and their size in that phase is a don't care. The loading of the switch transistors to the clock driver is not considered, as the latter can always be made sufficiently powerful for the first stage of a frequency divider.

The arrows and crosses in all 4 state-transitions are then tallied for each transistor, as shown in Fig.1b. Since each transistor can only have one geometry, it must accommodate the requirements from all 4 state-transitions. The conflicting nature of such requirements is apparent. Whether the optimization of transistor

dimensions is performed by a human designer or a computer, the conflicting requirements both from within each state-transition and from different state-transitions must be compromised. In the case of the human designer, recognition of what the conflicts are may lead him to come up with a better circuit configuration that resolves some of the conflicts.

Considering the sizing requirements in detail, several points are worth noting. Firstly, if used as a frequency divider, the first T-FF in the divider chain is required to operate the fastest. The requirements for the following stages can be eased because of reduced clock frequency. The clock driver to the first T-FF, not being constrained by a feedback loop, can be designed to be extremely powerful. There is therefore no requirement to reduce the loading from the T-FF's switch transistors whose source terminals are connected to the power supplies. Those transistors can therefore be very wide. Secondly, although transistor MN2 is the only load transistor on node y_1, it doesn't have to be narrow. This is because when node y_1 is being charged up, either MNS1 or MN2 is turned off. For similar reasons, MPS1 and to a lesser extent MNS2 do not present much loading and can be wide transistors. The remaining four transistors all have seriously conflicting sizing requirements. They are therefore the most difficult ones to design.

A Modified Single-Phase Edge Triggered D-FF

A further observation can be made. Exchanging the locations of transistors MP1 and MPS1 and those of MN3 and MNS2, as shown in Fig.3, does not change the function of the circuit. It can be verified that the new circuit in Fig.3 is still a D-flip-flop. In Fig.3, however, it is transistors MP1 and MN3 that are now floating during most state-transitions. This can substantially reduce the load at node D and node y_2 and improve the circuit speed. Switch transistors MPS1 and MNS2, on the other hand, are no longer floating. However, as they are driven by a powerful clock driver, the loading they present is not important and the two transistors can be as wide as necessary.

A similar analysis of the sizing requirements to the one shown in Fig.2 can be performed for the new circuit in Fig.3, where the resulting arrows and crosses are indicated. Seven out of nine transistors now do not have conflicting requirements. This greatly simplifies the task of choosing the compromise dimensions for transistors MN1 and MP2, whether this is done by a computer or a human designer.

In exchanging the two pairs of transistors, what has been done is that all switch transistors have been directly connected to the power supplies. This increases the load to the clock driver, which is known to be very powerful because inverter chains in an open loop can be much faster than those in a closed feedback loop. Moving the switch transistors to the supplies enables the other transistors which are in a feedback loop to be more or less floating when they are being driven. This reduces the load and improves speed. For the T-FFs which are further down a frequency divider chain, their clock input is the output of the T-FF they follow. The configuration in Fig.1 is a better choice as its load to the previous stage is not as high. Thus a frequency dividing circuit should start with the new circuit presented in Fig.3, to be followed by the existing 9-transistor D-FF in Fig.1.

The dimensions of an example design for the new D-FF are also shown in Fig.3 with an inverter as load. Using parameters from the VLSI Technology 2-μm standard CMOS process, clock frequencies of 880MHz, 1.1GHz and 2GHz have been predicted by SPICE simulations for the worst-case, typical case and best case SPICE parameters, respectively. The input and output waveforms for the 1.1GHz and 2GHz cases are shown in Fig.4a and Fig.4b, respectively. Under similar conditions, the maximum clock speeds we managed to achieve for the configuration in Fig.1 are about 30% lower.

When connected in a multi-stage frequency divider configuration, the maximum clock speed becomes lower for the same process as substantial load is presented to the first T-FF by the following T-FFs. A test chip comprising 9 T-FFs in a frequency divider configuration has been designed using the ES2 1.5-μm process. SPICE simulations predict between 1GHz and 2GHz clock frequencies for typical and best case parameters.

Conclusions

The electrical parameters such as the gate capacitance and drain-source current of a MOS transistor are complex functions of the terminal waveforms which change rapidly in time. This makes the optimal sizing of these transistors difficult in a digital circuit, as whether a transistor should be scaled up or down depends on the particular state-transition, which often presents conflicting requirements.

A simple example, the design of a 9-transistor D-FF in a toggle configuration, is used to illustrate the compromise that has to be made. A state-transition per state-transition analysis reveals not only all the conflicting requirements, but also possible ways to improve the circuit configuration.

Such an analysis leads to the modification of the existing D-FF configuration. The resulting new circuit enables 30% faster clocks to be used, according to SPICE simulations.

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Figures

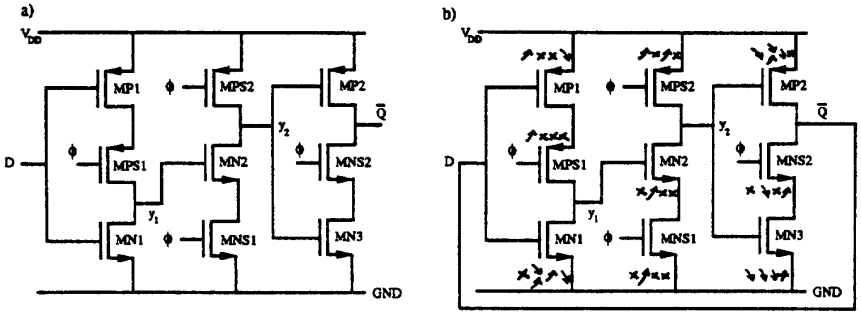

Fig.1 a) A D-FF from [2] b) T-FF with transistor sizing requirements marked

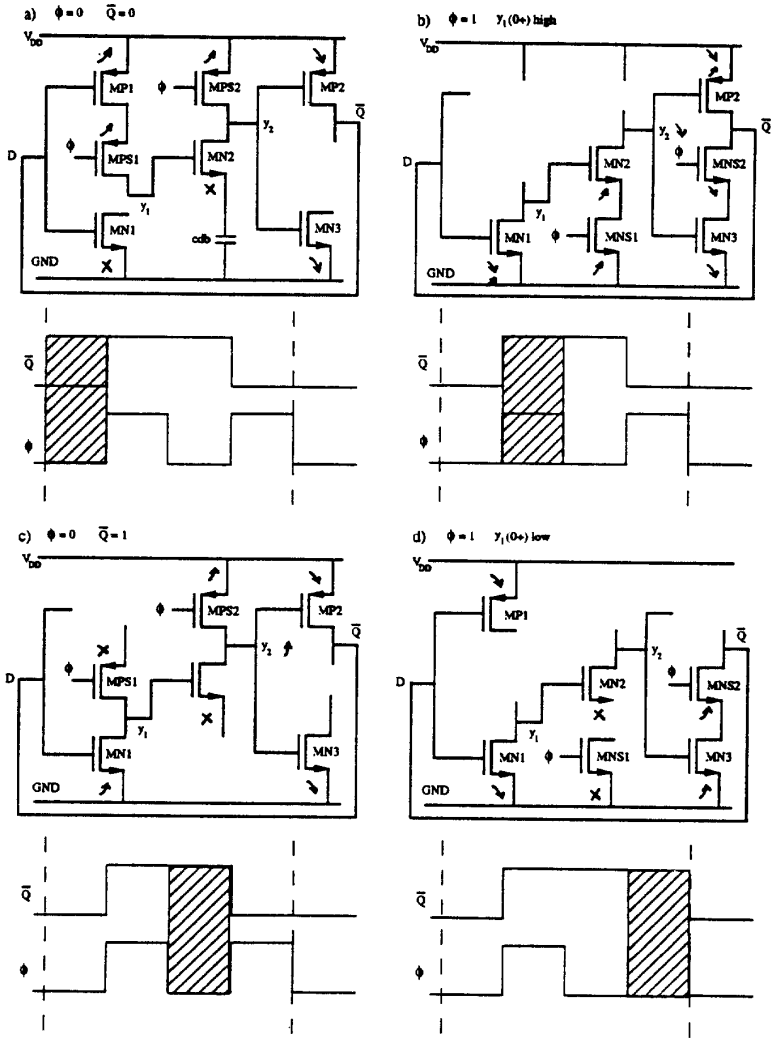

Fig.2 The Toggle Flip-Flop in Its Four State-Transitions

Fig.3

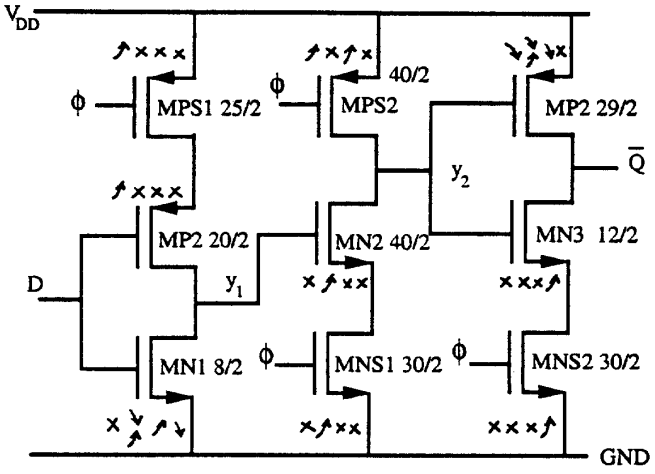

Fig.4a

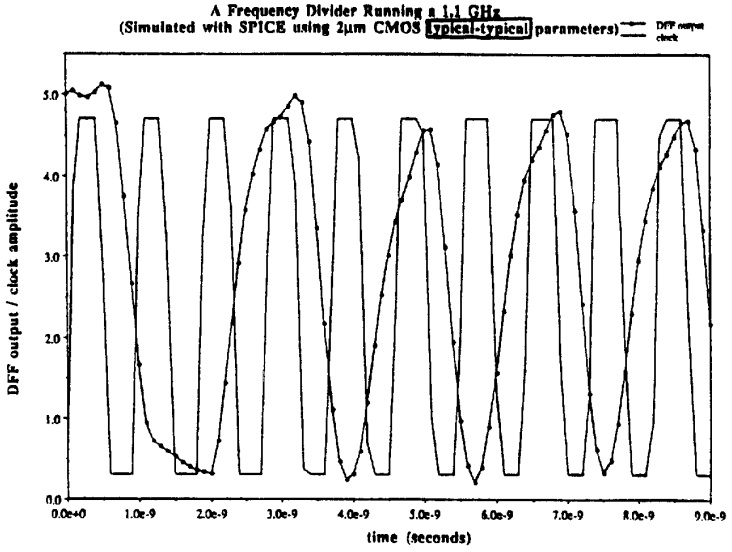

Fig.4b