ECE 124d/256c
Lab 3

In this lab you are to characterize the behavior of two cells: 1. a classical flip-flop design (the MMI_FFB.sp design from the /eci/tech/tsmc18/tech18/mmi18/stdcell/extract directory) and 2. a classical buffer -- specially wired allow you to determine its value as a parasitic bypass capacitor.

Part 1 FF:

Flip-flops are tricky circuits to fully characterize, in particular, you need to determine the setup and hold time (i.e. the timing aperture) the clock to q and clock to change times. All of these times are state dependent so need to be found separately for both rising and falling transitions. To make matters more complicated, you typically need to have some idea of the input slew rates to evaluate the jitter in these circuits.

a. In this part, use 3 'A' drive inverters to get fast but realistic drives and loads; One each on the d and clock inputs and one loading the q output. Drive the clock and D inputs with two periodic near-square logic signals at 500MHz and at 501 MHz respectively. Choose rise and fall times to approximate the loaded inverter times. Describe what you see at Q and determine setup, hold, clock to Q and clock to change times from this measurement. Hint: Reduce the difference in frequency to get higher resolution measurements, at the cost of longer simulations. Also look at the current usage and note if there are any discernible patterns (i.e. is there a maximum usage -- does it relate to the timing of the inputs? Repeat the experiment with a half rate clock on the d input. Does the result agree with your expectations? Finally, characterize the current usage of the flip-flop when the data does not change. Is it state dependent? In a large circuit, given the options of freezing the inputs or gating the clocks (i.e. freezing the clock) what is the relative power savings due to the flip-flops? (all of the above at 1.8 volts).

b. Vary the Vdd drive by +- 10% and find the sensitivity of the setup, hold and Clock-Q times to static voltage variation, for both rising and falling transitions. How does the power usage scale with voltage modulation? Does it agree with your expectations?

c. Introduce a pi-network representing a wire of 200um, 500um, 1mm and 2mm between the buffer and the d-input. Assume 2.9pF/cm and 5.4kΩ/cm wire characteristics. For these lengths, measure the slope at the d input, the signal arrival (i.e. 50% of Vdd time) and the setup time using a method similar to that above. Is the setup time affected by the change in slew rate? How? Lastly, shift the flip-flop power and ground supplies by 10% respectively for the 4 wire models. Does the behavior change as you expect?

Part 2 Buffer:

Design an experiment using spice to accurately measure the effective capacitance with respect to the power supply of an MMI_INVD inverter when its input is tied to Gnd and its output is tied to Vdd. Such a device is commonly used in designs to bypass the power supply for local current loads. (Read the Sani Paper) What is the value with input and output ties reversed? Why?