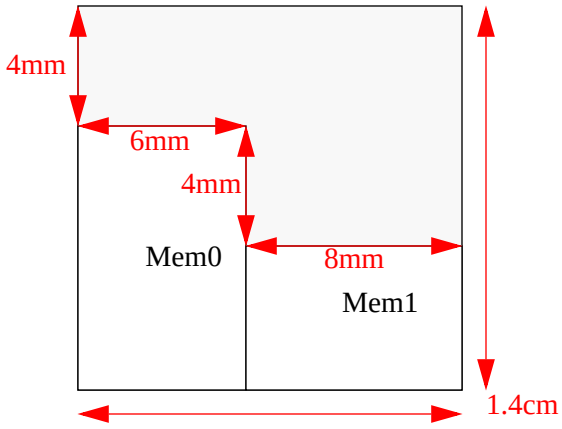
ECE 124d/256c
Final Lab: “Clock Distribution Network”

- Due: Wednesday March 16, 2011, noon via email to the TA, cc forrest@ece.ucsb.edu.

In this lab, your job is to design a single phase 400MHz clock tree suitable for driving 200,000 flip-flops which are uniformly distributed over a L-shaped region of a die as shown in the figure above. Each MMI_FFB flip-flop (clock network leaves) loads its clock input and your clock needs to have a single source which you can assume has zero jitter and is modeled by a single MMI_BUFE gate driven by your (perfect) clock (use a 60pS rise and fall voltage source for the input to this driver).



You are using metal interconnect with a resistance of 45mΩ/sq., 40 aF/μm^2 area capacitance and 65 aF/μm fringing capacitance on each side. The total cap = area component + 2 times the fringe component. (This specification is so you can make the wire wider and have a reasonable estimation of the capacitance and resistance. You may make the wires as long and wide as you desire with any topology you desire). In most cases, a 3 resistor+ 2 capacitor pi-model is sufficient to model the wire segments, however, if you use very wide wires with large currents, you should add appropriate inductors to your model. ***You need the delivered clock rise time to be less than 200pS at the flip-flops and the maximum skew+jitter must be less than 400pS for both rising and falling edges.*** Note that the clock delay could be larger than this value.

The circuit is subject to jitter because of power coupled noise which has a maximum droop of 150mV (1.8 V nominal, 1.65 V minimum), while the system ground has a bounce of 60mV max (0V to 60mV). These noise sources are not correlated in this area-bonded design so buffers separated by more than 0.5mm will be subject to different power and ground noise sources. Noise modeling is very important in this design. Set the wire model “substrate ground” to the spice ground node and model both power and ground supplies with voltage sources relative to this level. You will need to modify the MMI spice decks to support a “substrate ground” for parasitic capacitors and the n-channel substrate contacts in addition to power supply VDD and GND terminals). To validate your jitter modeling, you will need to run a few hundred Monte-Carlo test cases to plot a histogram of the simulated jitter at the leaves of your design.

Your buffers are selected from the MMI_BUF(B-E) buffers which can be used in any number (or in parallel) in your design. Your goal is to minimize the power dissipation of your clock network at 400MHz. Thus, wider wires (lowering the resistance), add capacitance and may cost you power as does adding more buffers or redundant signal paths in grid-like designs. On the other hand, small wires will require frequent rebuffering which adds jitter to the design. ***The design goal in this lab is to achieve the skew and jitter goals with the smallest power dissipation.***

Since you cannot build the entire circuit (it would simulate far too slowly), you need to exploit symmetry in the design so that the number of unique segments is minimized. Then you only need to simulate the uniquely different paths as long as you adequately add capacitive loading to the terminals to represent the segments you are not simulating. Design of this model is the primary effort in this lab -- please justify the assumptions you make and the sizes of parasitics and ensure that your network covers all of the needed flip-flop terminals. To find the total power, measure the current each buffer is using and multiply by the number of similar components in the network.

Please discuss the methods you use and results you obtain for your design clearly. Your lab report should contain the following parts:

1. A layout model describing accurately the physical design of the network, including placement, sizes of wires and buffer locations. The network may be a tree, grid, h-tree or hybrid design, but your model must have sufficient details to model the system.

2. A schematic of your electrical model from the source to sufficient leaves that the worst case behavior is modeled, showing the capacitive loads of your model. (In the case of a grid model, describe the simulation approach you chose).

3. A jitter/delay histogram model of the jitter at the leaf due to power coupled noise. Sufficient monte-carlo runs should be shown to validate your performance claims.

4. A power analysis for the design showing the assumed and simulated values and the overall power you achieved. Included in this analysis, please determine the total wire length and total area of metal, the total wire capacitance, total complement of buffers of different sizes, the equivalent total current drive in amps and total parasitic input and linearized output capacitance of the buffers.

5. Methods you used for optimization of the design or observations about your design and what your strategy was.

6. Sue, Spice and related model files as a compressed tarball.

Note -- Please organize your report to be as concise as possible, do not print out all of your spice decks or intermediate results into the report, but do substantiate your assumptions and models and show the overall design of your clock network. The game here is to model at a level which allows reasonably good ball-park bounds on the design. In practice, the detailed design would be the next step -- but you’d use this to knwo what to expect and where to push the design. Reports should be under 6 pages in length, inclusive of graphs and schematics.