SIGNAL DELAY IN RC TREE NETWORKS*

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Abstract

In MOS integrated circuits, signals may propagate between stages with fanout. The MOS interconnect may be modeled by an RC tree. Exact calculation of signal delay through such networks is difficult. However, upper and lower bounds for delay that are computationally simple are presented here. The results can be used (1) to bound the delay, given the signal threshold; or (2) to bound the signal voltage, given a delay time; or (3) to certify that a circuit is "fast enough", given both the maximum delay and the voltage threshold.

Introduction

In MOS integrated circuits, a given inverter or logic node may drive several gates, some of them through long wires whose distributed resistance and capacitance may not be negligible. There does not seem to be reported in the literature any simple method for estimating signal propagation delay in such circuits, nor is there any general theory of the properties of RC trees, as distinct from RC lines. The work reported here has led to a computationally simple technique for finding upper and lower bounds for the delay. The technique is of importance for VLSI designs in which the delay introduced by the interconnections may be comparable to or longer than active-device delay. This can be the case for polysilicon wires as short as 1 mm, with 4-micron devices. The importance of this technique grows as the wiring lengths increase or feature sizes decrease.

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Consider the circuit of Figure 1. The slowest transition (and therefore presumably the one of most interest) occurs when the driving inverter shuts off and its output voltage rises from a small value to V_{DD}. During this process the various parasitic capacitances on the output are charged through the pullup transistor. Figure 2 shows a simple model of this circuit for timing analysis. The pullup, which is nonlinear, is approximated by a linear resistor, and the transition is represented by a voltage source going from 0 to V_{DD} at time $t = 0$. (Later, for simplicity, a unit step will be considered instead.) The polysilicon lines are represented by uniform RC lines. The resistance of the metal line is neglected, but its parasitic capacitance remains. Capacitances associated with the pullup source diffusion, contact cuts, and the gates being driven are included. Any nonlinear capacitances are approximated by linear ones. The work reported here actually applies to voltage sources other than steps, and an example appears below with a saturated ramp input source.

In general, the circuit response cannot be found in closed form. The results of this paper can be used to calculate upper and lower bounds to the delay that are very tight in the case where most of the resistance is in the pullup. The theory as presented here does not explicitly deal with nonlinearities and therefore does not apply to signal propagation through pass transistors unless they are modelled as linear resistors. A more complete discussion of this theory will appear elsewhere [1], [2].

Analysis

An RC tree is defined as follows. Consider any resistor tree with no node at ground. From each node in this tree a capacitor to ground may be added, and any resistor may be replaced by a distributed RC line. Although nonuniform RC lines may appear in an RC tree, for simplicity the

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examples in this paper involve only lumped resistors and capacitors and uniform RC lines. An RC tree has one input and any number of outputs. Side branches may or may not end in a node that is considered as an output; in fact, outputs may be taken anywhere in the tree. Nonuniform RC lines are special cases of RC trees, without any side branches. An important property of RC trees is that there is a unique path from any point in the tree to the input.

The tree representing the signal path is driven at the input with a unit step voltage. (Below, this result is generalized to other driving voltages.) Gradually the voltages at all other nodes, and in particular at all the outputs, rise from 0 to 1 volt. It is assumed that the output voltages cannot be calculated easily. The problem is to find simple upper and lower bounds for the output voltages, or, equivalently, to find upper and lower bounds for the delay associated with each output.

Consider any output node e, and any lumped capacitor at node k with capacitance C_k. For the moment consider only lumped capacitors; the theory is similar if the distributed lines are considered also. One may think of many-stage approximations for the distributed lines, or one may convert some summations in the formulas below to a form including both summations over lumped capacitors and integrals over distributed ones.

The resistance R_{ke} is defined as the resistance of the portion of the (unique) path between the input and e, that is common with the (unique) path between the input and node k. In particular, R_{ee} is the resistance between input and output e and R_{kk} is the resistance between the input and node k. Thus $R_{ke} \le R_{kk}$ and $R_{ke} \le R_{ee}$. For an illustration, see Figure 3.

The sum (over all the capacitors in the network)

$$T_{De} = \sum_k R_{ke} C_k \tag{1}$$

has the dimensions of time, and is equal to the first-order moment of the impulse response, which has been called "delay" by Elmore [3]. Next, define for each output e two quantities that also have the dimensions of time,

$$T_P = \sum_k R_{kk} C_k \tag{2}$$

$$T_{Re} = \left(\sum_k R_{ke}^2 C_k\right)/R_{ee}. \tag{3}$$

All three summations extend over all the capacitors of the network. Each of these three quantities plays a role in the final delay formulas, but none of them is equal to the delay. Each can be computed easily, even in the presence of distributed lines, and while T_{Re} is in general different for different output nodes, T_P is the same for all outputs. It is easily seen that

$$T_{Re} \le T_{De} \le T_P. \tag{4}$$

For nonuniform RC lines (i.e., RC trees without side branches) $T_{De} = T_P$. For a single uniform RC line, $T_P = T_{De} = RC/2$, and $T_{Re} = RC/3$.

A detailed derivation [1] leads to the upper bounds for the unit step response $v_e(t)$

$$v_e(t) \le 1 - \frac{T_{De} - t}{T_P} \tag{5}$$

$$v_e(t) \le 1 - \frac{T_{De}}{T_P} e^{-t/T_{Re}} \tag{6}$$

and lower bounds for the unit step response $v_e(t)$

$$v_e(t) \ge 0 \tag{7}$$

$$v_e(t) \ge 1 - \frac{T_{De}}{t + T_{Re}} \tag{8}$$

$$v_e(t) \ge 1 - \frac{T_{De}}{T_P} e^{(T_P - T_{Re})/T_P} e^{-t/T_P} \tag{9}$$

where (9) applies if $t \ge T_P - T_{Re}$. The tightest upper bounds are (5) for small t and (6) for large t. The tightest lower bounds are (7) for $t \le T_{De} - T_{Re}$, (8) for $T_{De} - T_{Re} \le t \le T_P - T_{Re}$, and (9) for $T_P - T_{Re} \le t$.

Bounds for the time, given the unit step response voltage, are possible because the voltage is a monotonic function of time (a fact proven in [1]). Of course

$$t \ge 0 \tag{10}$$

and in addition, (5) and (6) can be inverted to yield

$$t \ge T_{De} - T_P[1 - v_e(t)] \tag{11}$$

$$t \ge T_{Re} \ln \frac{T_{De}}{T_P[1 - v_e(t)]} \tag{12}$$

and (8) and (9) yield

$$t \le \frac{T_{De}}{1 - v_e(t)} - T_{Re} \tag{13}$$

$$t \le T_P - T_{Re} + T_P \ln \frac{T_{De}}{T_P[1 - v_e(t)]} \tag{14}$$

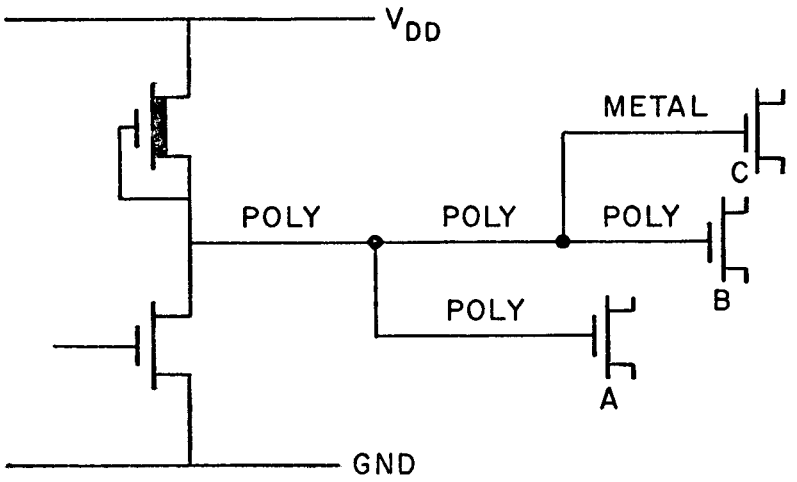

Figure 1. Typical MOS signal-distribution network. The inverter is shown driving three gates.

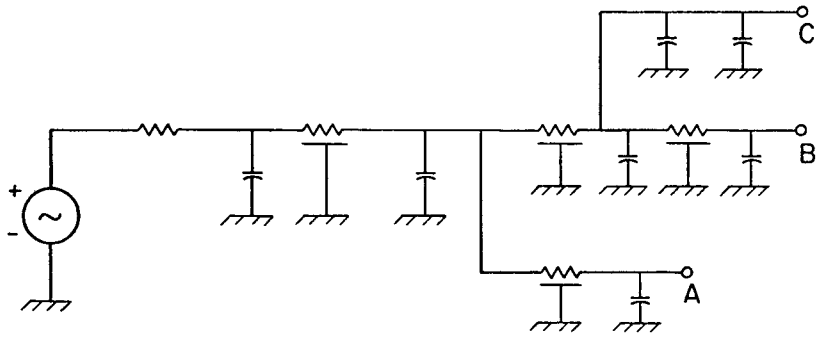

Figure 2. Linear-circuit model for the network of Figure 1. The voltage source is a step at time $t = 0$.

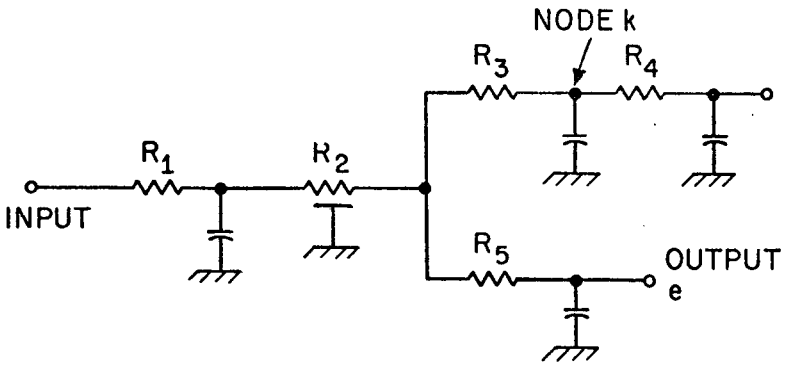

Figure 3. Illustration of resistance terms. For this network, $R_{ke} = R_1 + R_2$, $R_{kk} = R_1 + R_2 + R_3$, and $R_{ee} = R_1 + R_2 + R_5$.

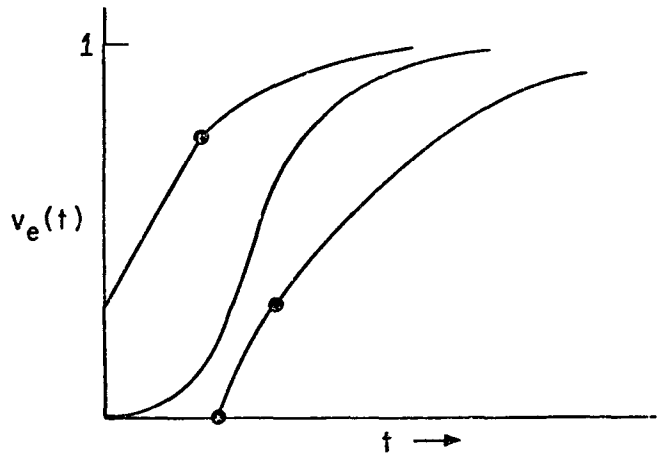

Figure 4. Form of the bounds, with the distances from the exact solution exaggerated for clarity.

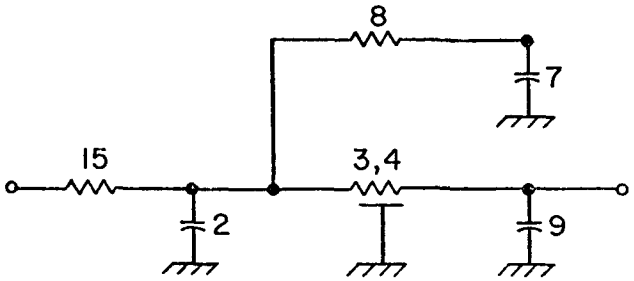

Figure 5. Example network. Parameter values are in ohms and farads.

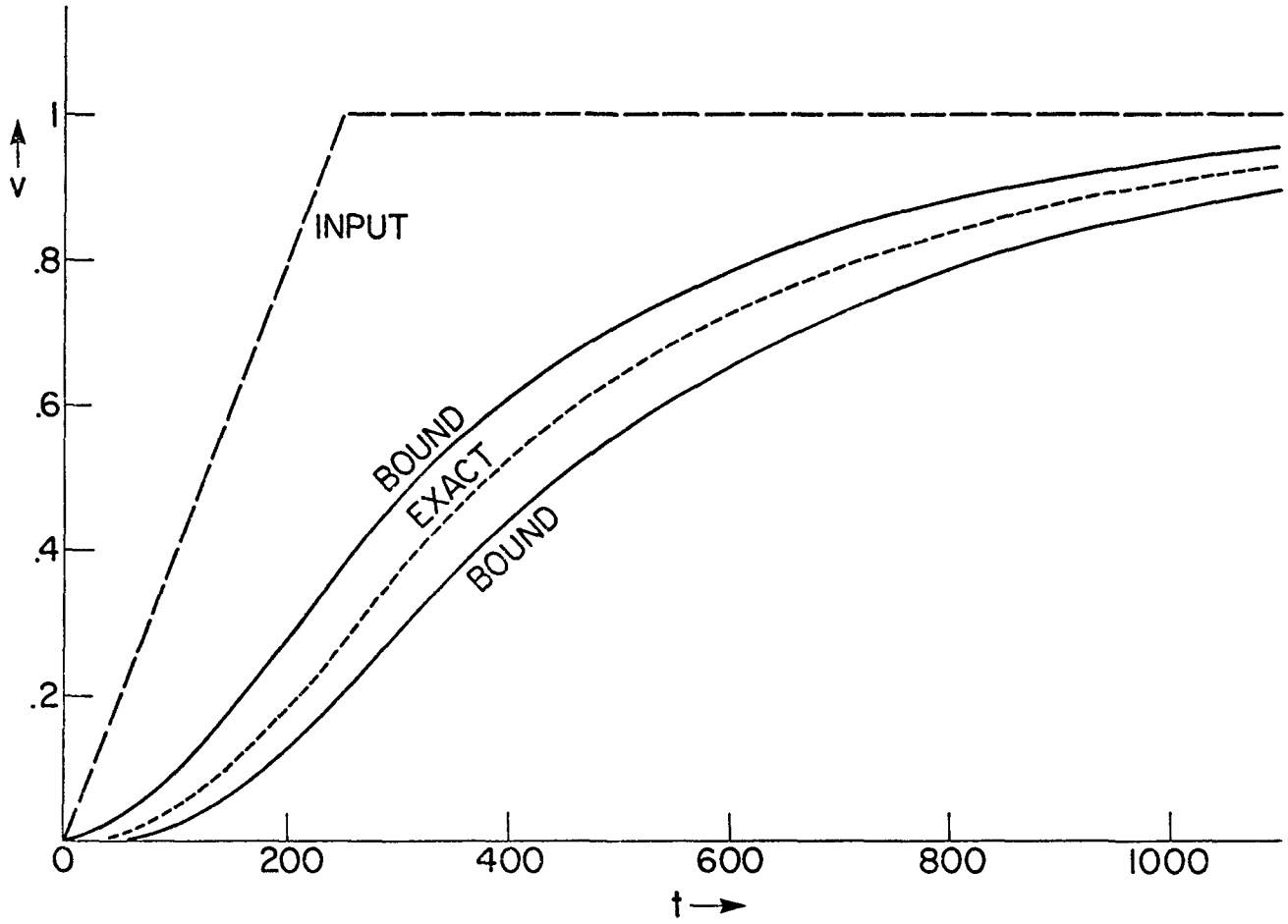

Figure 6. Upper and lower bounds for the network in Figure 5, with a saturated ramp input. The exact solution, found from circuit simulation, is shown also.

where (14) only applies if $v_e(t) \geq 1 - T_{De}/T_P$. The general form of all these bounds is illustrated in Figure 4.

Arbitrary Input Waveforms

Bounds for the response $y_e(t)$ of an RC tree to an arbitrary excitation $x(t)$ can be obtained from the bounds $v_{ue}(t)$ and $v_{le}(t)$ just derived for the unit step response $v_e(t)$.

First, the superposition integral can be used to obtain $y_e(t)$ as

$$y_e(t) = \int_0^t v_e(t - t') \frac{dx(t')}{dt'} dt'$$

$$= v_e(t) * dx/dt \qquad (15)$$

where $*$ denotes time convolution. From

$$v_{le}(t) \leq v_e(t) \leq v_{ue}(t) \qquad (16)$$

one obtains, if $dx/dt \geq 0$,

$$v_{le}(t) * dx/dt \leq y_e(t) \leq v_{ue}(t) * dx/dt \qquad (17)$$

or if $dx/dt \leq 0$,

$$v_{ue}(t) * dx/dt \leq y_e(t) \leq v_{le}(t) * dx/dt \qquad (18)$$

where $v_{ue}(t)$ and $v_{le}(t)$ are known analytically. From (17) it can be seen that bounds for the ramp response can be obtained simply by integrating the unit step bounds. Equations (17) and (18) apply for monotonic inputs.

The general case, where the excitation $x(t)$ has both positive and negative slopes, is treated elsewhere [1].

As an illustration of the use of these relations, consider the network of Figure 5, excited with a saturated ramp. The actual response (calculated from an expensive simulation) is shown along with the upper and lower bounds, from (17), in Figure 6.

Practical Algorithms

One way to use the inequalities of the previous sections is to consider the overall RC tree, and compute for each capacitor the appropriate R_{ke} and R_{kk} so that T_P, T_{De}, and T_{Re} for each output can be found. Of course for distributed lines the sums are replaced by appropriate integrals. In this approach, the calculations necessary for each output require time proportional to the square of the number of elements.

An alternate approach is to build up the network by construction, and calculate independently for each of the partially constructed networks enough information to permit the final calculation of T_P, T_{De}, and T_{Re}. The computation time for each output is then proportional to the number of elements, rather than the square of the number. Programs that implement this approach appear elsewhere, in both a restricted form [2] and a more general form [1].

Conclusions

A computationally efficient method for calculating the signal delay through MOS interconnect lines with fanout has been described. Tight upper and lower bounds for the step response of RC trees have been presented. Linear-time algorithms exist for calculating these bounds from an algebraic description of the tree. Substantial computational simplicity is achieved even in the presence of RC distributed lines by representing the RC tree by a small set of suitably defined characteristic times, which can be calculated by inspection and used to generate the bounds.

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