Buffer Delay Change in the Presence of Power and Ground Noise

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ABSTRACT

Variations of power and ground levels affect VLSI circuit performance. Trends in device technology and in packaging have necessitated a revision in conventional delay models. In particular, simple scalable models are needed to predict delays in the presence of uncorrelated power and ground noise. In this paper, we analyze the effect of such noise on signal propagation through a buffer and present simple, closed-form formulas to estimate the corresponding change of delay. The model captures both positive (slowdown) and negative (speedup) delay changes. It is consistent with short-channel MOSFET behavior, including carrier velocity saturation effects. An application shows that repeater chains using buffers instead of inherently faster inverters tend to have superior supply-level-induced jitter characteristics. The expressions can be used in any existing circuit performance optimization design flow or can be combined into any delay calculations as a correction factor.

Categories & Subject Descriptors: [Computer-Aided Engineering]: Computer-aided design (CAD).

General Terms: Algorithms.

Keywords: Power and ground noise, differential mode noise, common mode noise, incremental delay change.

1. INTRODUCTION

This paper describes a new model for the change in buffer delay caused by both power and ground supply level variations and level variations between stages in sequences of repeaters. These delay changes are a large component of the total timing jitter for a signal where the jitter accounts for all noise sources such as substrate noise and coupling noise as well as power level noise. There is a substantial amount of previous work in this area, notably papers: [4][6][13][14] [19]. However, for several reasons described below, we believe that the problem bears re-examination and a renewed effort to create a fast, simple model suitable for mass implementation in a modern design flow.

Growth in design sizes and scaling of interconnections have led to the requirement for insertion of very large numbers of buffer/repeaters in recent designs [1][7][9][15]. Among them, [9] proposes an optimum multistage buffer design to drive long uniform lines. [7] and [15] consider simultaneous buffer insertion and wire sizing for timing optimization. [1] presents comprehensive buffer insertion techniques for noise and delay optimization. Because of the buffer/repeaters' preponderance in number, use in heavily loaded nets, and use in clock and timing circuits, buffer delays account for a large percentage of all critical timing nets in a design. In some of these applications, total timing uncertainty (not just worst-case delay) is important. Disturbance of the buffer delay will affect the type, number and position of buffers that optimize the interconnect delay. Therefore, it is essential to take the change of delay into consideration in order to adjust the solution for timing optimization. At the same time, scaling of power supply levels and improving transconductance of devices have increased the sensitivity of buffers to supply-level-induced delays. Finally, increases in chip-level design scales and modern packaging strategies such as bump bonding have localized supply variations so that buffers in one set of supply levels are driving buffers in another zone with different supply levels. Since power loading is logic switching-dependent and supply sources are localized, power and ground levels need not be inversely correlated as is typical in a wire bonded die.

Under such conditions, power-level-induced delay changes may either increase or decrease the effective delay of a buffer, and successive stages may or may not accumulate incremental delays. One must consider both power and ground levels at the signal source and at the current buffer to derive an equivalent delay change. This value can be substantially smaller than that predicted by superposing ground-bounce and power level changes [3][5][10][20][21]. The superposition approximation works well only if the variations in the power distribution network are mirrored in the ground network. However, due to changes in packaging technology and the number of pins that can feasibly be devoted to power and ground connections, no single parasitic dominates the noise on the power and ground nets. Yet another trend in technology is the relative reduction of gate parasitics compared to those from the interconnection network. The net effect of this is de-correlation of the power and ground voltage variations which in turn make delay variations much more complex. In particular, the worst-case

delay caused by power noise may not occur simultaneously with the worst-case delay due to ground noise, and the superposition may cause a substantial overestimation. Second, the delay effects of *common mod*e voltage shifts will be shown to be larger in scale than equivalent differential mode changes. (Differential mode voltage shifts are the most commonly studied model). Lastly, changes in power distribution and clocking strategies, and the potential for future changes, create the need for a timing model which is independent of common assumptions about power level noise sources. We *do* assume that large scale power level changes result from an ensemble effect of many devices at a variety of differing slew rates. However, in a practical design there must always be some amount of local decoupling capacitance (both parasitic and added). This capacitance limits the magnitude of the highest speed noise excursions. (This cannot be done in later stages of the power network design because of inductance in both the physical network and the packaged capacitors). We therefore assume that the remaining large magnitude noise excursions occur at a somewhat slower time scale than the typical switching transitions in buffers meeting common design requirements.

In the following, we analyze the effect of P/G (power/ ground) noise on buffer delay, and present linear, closed-form formulas for the corresponding incremental changes in delay based on a short-channel transistor model. The expressions simultaneously model both the power supply and ground levels, resulting in positive (slowdown) or negative (speedup) delay changes. These expressions are intended for inclusion in timing analysis tools and statistical delay estimators as corrections to nominal delay models that account for other effects. The expressions make few assumptions about the specific shape of the P/G noise waveform. Furthermore, they are shown to be largely independent of the buffer load circuit structure, increasing their applicability.

The rest of the paper is organized as follows: sections 2-3 define P/G noise, buffer delay nomenclature, and illustrate the P/G-noise-induced buffer delay change. Section 4 presents our new model. Section 5 demonstrates the accuracy and fidelity of the model. Applications of the model and concluding remarks are presented in sections 6-7. Detailed derivations are given in Appendices A and B.

2. BUFFER DELAY CONVENTIONS

A *buffer* is a chain of tapered inverters. Here, we consider buffers consisting of one inverter or two inverters.

2.1 Variation of V_{dd} and V_{ss}

We use V_{dd}, V_{ss}, V_i (input), V_{in} (adjusted input), V_o (output), V_{out} (adjusted output), etc. to represent values related to the ideal power and ground levels, and we use V_{dd}', V_{ss}', V_i', V_{in}', V_o', V_{out}', etc. to represent the corresponding values in the presence of power and ground noise. ΔV_{dd} and ΔV_{ss} denote the variation of power supply and ground, respectively.

$$\Delta V_{dd} = V_{dd}' - V_{dd} \text{ (power noise)} \quad (1)$$

$$\Delta V_{ss} = V_{ss}' - V_{ss} = V_{ss}' \ (V_{ss} = 0) \text{ (ground noise)} \quad (2)$$

In small-scale wire-bond packaging styles, a dominant supply level noise source is bond wire inductance in the package. Neglecting I/O current drives, the power and ground noise of the chip due to simultaneous switching typically follows an inverse pattern, and ΔV_{dd} is often symmetric to $\Delta V_{ss.}$ However, in modern bump-bonded and low-inductance package styles, the package distributes power over the whole area of the chip (figure 1). Every bump connects to an underlying local power/ground network. To save chip metallization area and improve density, global power distribution metal is reduced in preference to thicker package distribution layers. Increasing design scales causes an increase in long wire loading, and in more wires connecting between different power domains. Logic-level-dependent currents flow between such blocks, causing asymmetric power and ground noise within a block. This noise is increased by the inclusion (within a bump block) of long wire repeater buffers which are often added in a post-placement timing optimization step.

Figure 1 shows a simple circuit which uses bump-bond packaging. Each block is defined by the subcircuit supplied by a pair of bumps (V_{dd}/V_{ss}). Suppose that the cells A to E have transitions. Switching of the buffers A, B and D has a symmetric effect on the power and ground noise ($\Delta V_{dd}^{'(1)}$ and $\Delta V_{ss}^{'(1)}$), because they drive loads (consisting largely of parasitic interconnect capacitance) within the same block. On the other hand, switching of the C and E buffers has a non-symmetric effect on $\Delta V_{dd}^{'(1)}$ and $\Delta V_{ss}^{'(1)}$, because they drive loads which are outside of block 1, causing different switching currents to flow through the power and ground ports of block 1. Since wires leaving a block are likely to be physically long, these currents are proportionally large. In general, there is little reason for the currents flowing out of the block via loads to cancel.

2.2 Incremental buffer delay change

To allow reference to previous work, it is necessary to formally define the model for buffer delay, as the measurement levels are subject to noise.

Without loss of generality, we define a buffer's *ideal* delay as the time interval between its input and output voltage reaching 50% of the power supply level. Figure 2 illustrates the definition for an inverter delay given ideal power supply and ground levels. t_{pHL} is the high-to-low delay when the input of the inverter has a rising transition. The input and output transition times are t_r and t_{oT}, respectively. Other time values are: t_{i5}, t_{o5}, t_{o1} and $t_{o9,}$ which are times when the

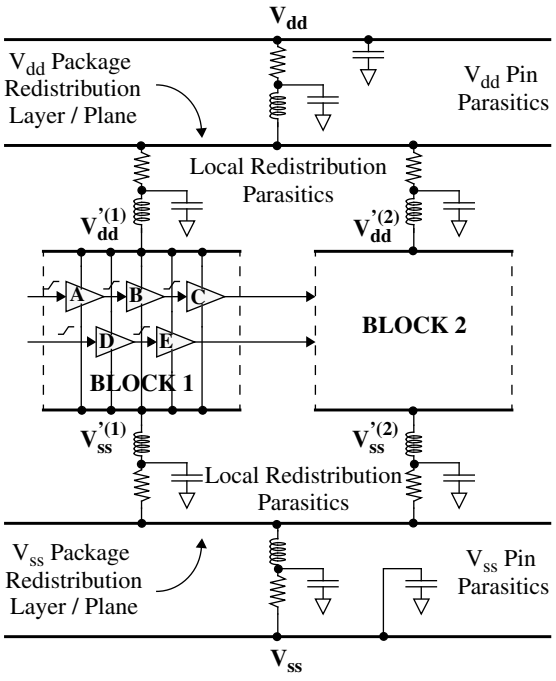


Figure 1. Power distribution in bump-bond packaging

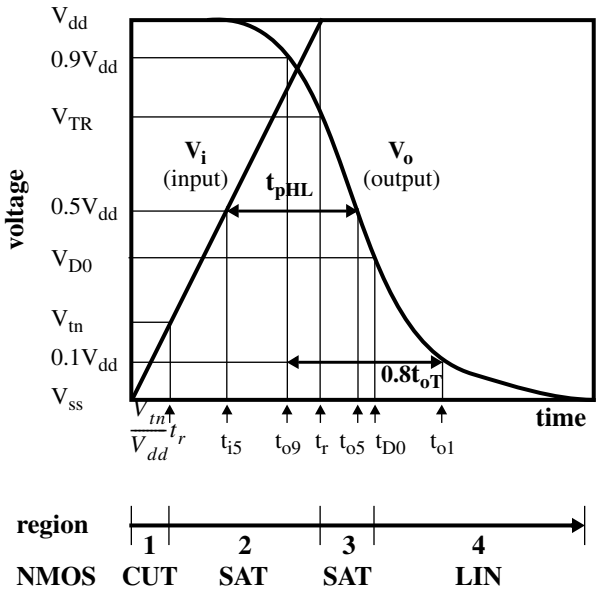


Figure 2. Ideal inverter transition and nomenclature

input or output voltage reaches 50%, 10%, and 90% of V_{dd}, respectively.

$$t_{pHL} = t_{o5} - t_{i5} \tag{3}$$

$$t_{oT} = \frac{t_{o1} - t_{o9}}{0.8} \tag{4}$$

Figure 3 (a) and (b) illustrate the delay and slope when there is a P/G noise. In figure 3(a), we assume a bump-bond packaging technique, in which every bump has a small power/ground network, relatively independent of the others. Therefore the low and high voltage levels of the input transition ($V_{ss} \rightarrow V_{dd}$) are independent of the change of power supply and ground level for the buffer. The corresponding buffer delays are $t_{pHL}^{(1)}$ and $t_{pHL}^{(2)}$. In figure 3(b), conventional wire-bond packaging technique is assumed. For such a technique, the dominant noise on the power supply and ground level is often due to the wiring inductance in the package, so the whole chip's power and ground noises are synchronized. Therefore, the voltage level of the input transition ($V_{ss}' \rightarrow V_{dd}'$) will be the same as that of the buffer. The corresponding buffer delays are $t_{pHL}^{(3)}$ and $t_{pHL}^{(4)}$. Because of power supply and ground level changes, we are interested in delay measured at different voltage levels: the 50% point between the ideal V_{dd} and V_{ss} ($t_{pHL}^{(1)}$ and $t_{pHL}^{(3)}$), and the 50% point between the disturbed V_{dd}' and V_{ss}' ($t_{pHL}^{(2)}$ and $t_{pHL}^{(4)}$). Hence we have four types of disturbed buffer delays, corresponding to four types of buffer delay changes.

The special output voltage points are defined as follows:

$$V_{o1}' = V_{ss}' + 0.1(V_{dd}' - V_{ss}')$$

$$V_{o5}' = V_{ss}' + 0.5(V_{dd}' - V_{ss}')$$

$$V_{o9}' = V_{ss}' + 0.9(V_{dd}' - V_{ss}')$$

The disturbed high-to-low delay and slope are given by:

$$t_{pHL}^{(j)} = t_{o5}^{(j)} - t_{i5}^{(j)}$$

$$t_{oT}^{(j)} = \frac{t_{o1}^{(j)} - t_{o9}^{(j)}}{0.8}$$

where $j = 1, 2, 3, 4$, indicating four different definitions of the disturbed buffer delay and output slope illustrated in figure 3 (a) & (b).

In figure 3(a) we have $t_{o1}^{(1)} = t_{o1}^{(2)}$ and $t_{o9}^{(1)} = t_{o9}^{(2)}$. In figure 3(b) we have $t_{o1}^{(3)} = t_{o1}^{(4)}$ and $t_{o9}^{(3)} = t_{o9}^{(4)}$. Therefore,

$$t_{oT}^{(1)} = t_{oT}^{(2)},\ t_{oT}^{(3)} = t_{oT}^{(4)}$$

With a rising transition at the input, the changes of delay and output transition time are defined as follows:

$$\Delta t_{pHL}^{(j)} = t_{pHL}^{(j)} - t_{pHL}$$

$$\Delta t_{oT}^{(j)} = t_{oT}^{(j)} - t_{oT}$$

The results shown in figure 5 are according to the first type of delay definition with *j = 1*.

3. P/G NOISE DELAY EFFECTS

The changes of power supply and ground level affect signal propagation through an inverter in several different ways, which will be discussed in this section.

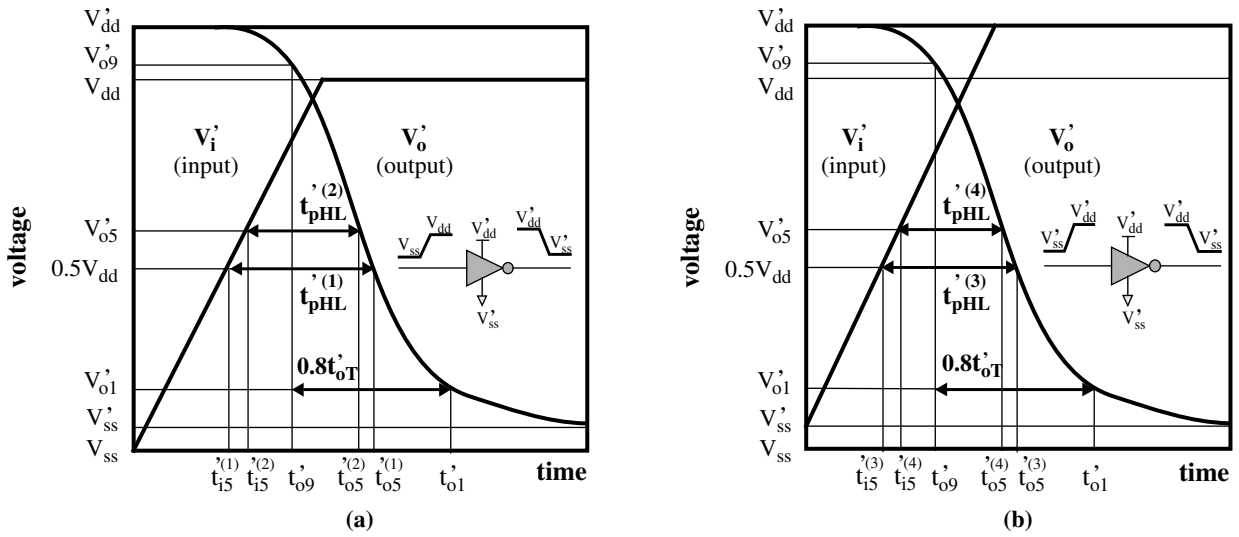


Figure 3. Notation for disturbed delay and slope

3.1 Differential mode noise

We define the *differential mode noise* (DMN) ΔV_{dif} as:

$$\Delta V_{dif} = V'_{dif} - V_{dif} = \Delta V_{dd} - \Delta V_{ss}$$

where

$$V'_{dif} = V'_{dd} - V'_{ss} \text{ and } V_{dif} = V_{dd} - V_{ss}$$

We have observed through HSpice simulations that the voltage difference (V_{dif}) between the power supply and ground level affects the inverter delay (t_{pHL}/t_{pLH}), which is the inverter's ability to propagate signals. Similarly, the change of the above difference (ΔV_{dif}) affects the change of delay ($\Delta t_{pHL}/\Delta t_{pLH}$).

The differential mode noise ΔV_{dif} may become positive or negative, depending on the directions and relative amplitudes of ΔV_{dd} and ΔV_{ss}. The voltage difference (V_{dif}) between power supply and ground level determines how fast the buffer charges/discharges its capacitive load, so it affects the delay and the transition time of the buffer output. The larger the difference ($V'_{dif} > V_{dif} \Rightarrow \Delta V_{dif} > 0$), the faster the output charging/discharging and the smaller the buffer delay ($t'_{pHL} < t_{pHL} \Rightarrow \Delta t_{pHL} < 0$), which is stated in observation 1.

Observation1: The buffer delay change is linearly dependent on the differential mode noise (DMN), as will be shown in section 4:

$$\Delta t_{pHL}\big|_{DMN} = -k_d \cdot \Delta V_{dif} = -k_d \cdot (\Delta V_{dd} - \Delta V_{ss}) \qquad (5)$$

where k_d is a positive constant dependent on the device and technology parameters, the input transition times, and the gate load. The expression of k_d can be found from equation (A5) in Appendix B. Similar effects hold for both high-to-low delay Δt_{pHL} and low-to-high delay Δt_{pLH}.

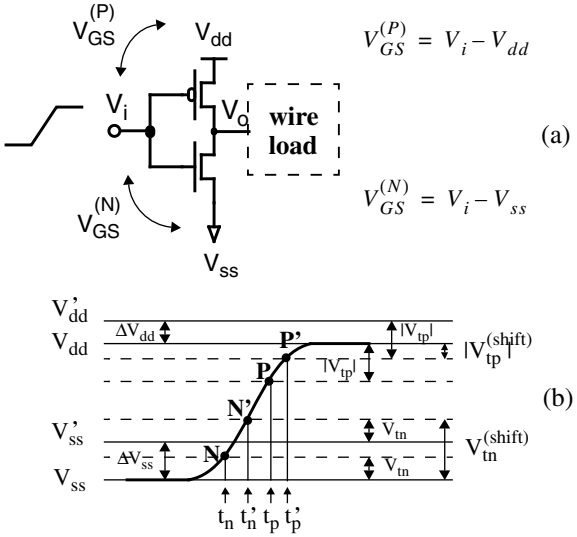


Figure 4. Threshold shift of an inverter

3.2 Common mode noise

We define the *common mode noise* (CMN) ΔV_{com} as:

$$\Delta V_{com} = \Delta V_{dd} + \Delta V_{ss}$$

CMN modifies the effective switching threshold of the gate. The threshold shift changes the gate delay as illustrated in figure 4. Figure 4(a) shows a rising transition arriving at the buffer. Figure 4(b) illustrates the gate threshold shift and the corresponding delay change caused by the power and ground variations.

In figure 4(b), N and P are the original points when the NFET switches from cutoff to saturation region and PFET switches from saturation to cutoff, respectively. The

corresponding switching times are indicated t_n and t_p. For noise of limited amplitude, the transistor thresholds (V_{tn} and V_{tp}) do not change significantly, namely,

$$V_{GS}^{'(N)}\Big|_{CUT} = V_i - V_{ss}^{'} = V_{tn} > 0$$

$$V_{GS}^{'(P)}\Big|_{CUT} = V_i - V_{dd}^{'} = V_{tp} < 0$$

This causes a shift of the NFET and PFET switching points from *N* and *P* to *N'* and *P'*. The corresponding switching time shifts to $t_n^{'}$ and $t_p^{'}$, respectively.

The points *N'* and *P'* can be mapped to shifted thresholds in figure 4(a) with ideal power supply and ground level:

$$V_{GS}^{(N)}\Big|_{CUT} = V_i - V_{ss} = V_{tn}^{(shift)}$$

$$V_{GS}^{(P)}\Big|_{CUT} = V_i - V_{dd} = V_{tp}^{(shift)}$$

We observe in figure 4(b) that:

$$\Delta V_{ss} > 0 \Rightarrow V_{tn}^{(shift)} > V_{tn} \Rightarrow t_n^{'} > t_n \Rightarrow \text{increasing delay}$$

$$\Delta V_{dd} > 0 \Rightarrow V_{tp}^{(shift)} > V_{tp} \Rightarrow t_p^{'} > t_p \Rightarrow \text{increasing delay}$$

Obviously, it takes more time for the NFET transistor to be turned on and PFET to be turned off when both power supply and ground level increase.

On the other hand, when power supply and ground level decrease, we have

$$\Delta V_{ss} < 0 \Rightarrow V_{tn}^{(shift)} < V_{tn} \Rightarrow t_n^{'} < t_n \Rightarrow \text{decreasing delay}$$

$$\Delta V_{dd} < 0 \Rightarrow V_{tp}^{(shift)} < V_{tp} \Rightarrow t_p^{'} < t_p \Rightarrow \text{decreasing delay}$$

Hence, it takes less time for the NFET transistor to be turned on and PFET to be turned off for decreased power and ground level.

Therefore, we make the following observation:

Observation 2: For an input with a rising transition, the dependency between the common mode noise (CMN) and the buffer delay change can be expressed by:

$$\Delta t_{pHL}\Big|_{CMN} = k_{cr} \cdot \Delta V_{com} = k_{cr} \cdot (\Delta V_{dd} + \Delta V_{ss}) \qquad (6)$$

where k_{cr} is a positive constant determined by the device and technology parameters, input transition time, and the gate load. The expression of k_{cr} can be found from equation (A5) in Appendix B.

Similarly, for an input with a falling transition, the dependency between the common mode noise (CMN) and the buffer delay change can be expressed by:

$$\Delta t_{pLH}\Big|_{CMN} = -k_{cf} \cdot \Delta V_{com} = -k_{cf} \cdot (\Delta V_{dd} + \Delta V_{ss}) \qquad (7)$$

where k_{cf} ia a positive constant determined by the device and technology parameters, input transition time, and the gate load.

For a rising transition, the effective switching threshold of an inverter is set by the current balance of the two active transistors. For positive common mode noise, this switching threshold is higher, and therefore it is reached later by the rising transition. Thus the delay is increased even though the voltage across the inverter, and hence the current drive, remains constant.

For a falling transition, the effective switching threshold of the gate rises, so that the threshold voltage level is reached earlier, and the effective gate delay decreases. This effect occurs even if the differential mode noise is zero, as it is the switching level - not the current drive - that is altered by the common mode noise.

We note an analogy here: a rising input transition with positive common mode noise can be thought of as climbing a rising mountain, which takes more time than climbing a mountain of initially the same, yet stationary, dimensions. A falling input transition with the same positive common mode noise is analogous to going downhill when the bottom of the mountain rises, which takes less time than descending a corresponding fixed dimensions mountain.

Therefore, common mode noise has a different effect on rising and falling transitions.

3.3 Loading effects

Both differential mode noise (DMN) and common mode noise (CMN) change buffer delays. Since the delay change can be of either sign, the noise sources need to be modeled together. Figure 5 shows alternative load configurations and the corresponding simulated delay change (both rising and falling transition) in 0.18µm technology. Note: $\Delta delay = 0$ when $\Delta V_{dd} = \Delta V_{ss} = 0$.

In figure 5 (a), the wire load of the inverter is a distributed RC tree network, including vias, extracted from the layout of a real circuit. In figure 5 (b), the wire load is simplified to an RC π-model. In figure 5 (c), the wire load is further simplified to a single resistor plus a single capacitor. In figure 5 (d), an effective loading capacitor is used to replace the inverter's output load. These simplified wire-load models in figures 5(b)-(d) can be obtained using the methods described in [16]. The delay is measured when its input (V_i) and output (V_o / V_o' / V_o" / V_o"') voltage reach 50% of the ideal power supply voltage, respectively. The range for the power and ground noise is from -20% (-0.36 volt) to 20% (0.36 volt) of the power supply voltage, which is set to 1.8 volt for the selected technology. The range for the change of delay is from -30ps to 30ps.

It is interesting to note that each of the four wire load models displays a linear relationship between the change of power/ground level and the change of inverter delay. Furthermore, the linearity improves when the change of power and ground level is smaller than 20%. In practical designs, the tolerable range for the power and ground levels

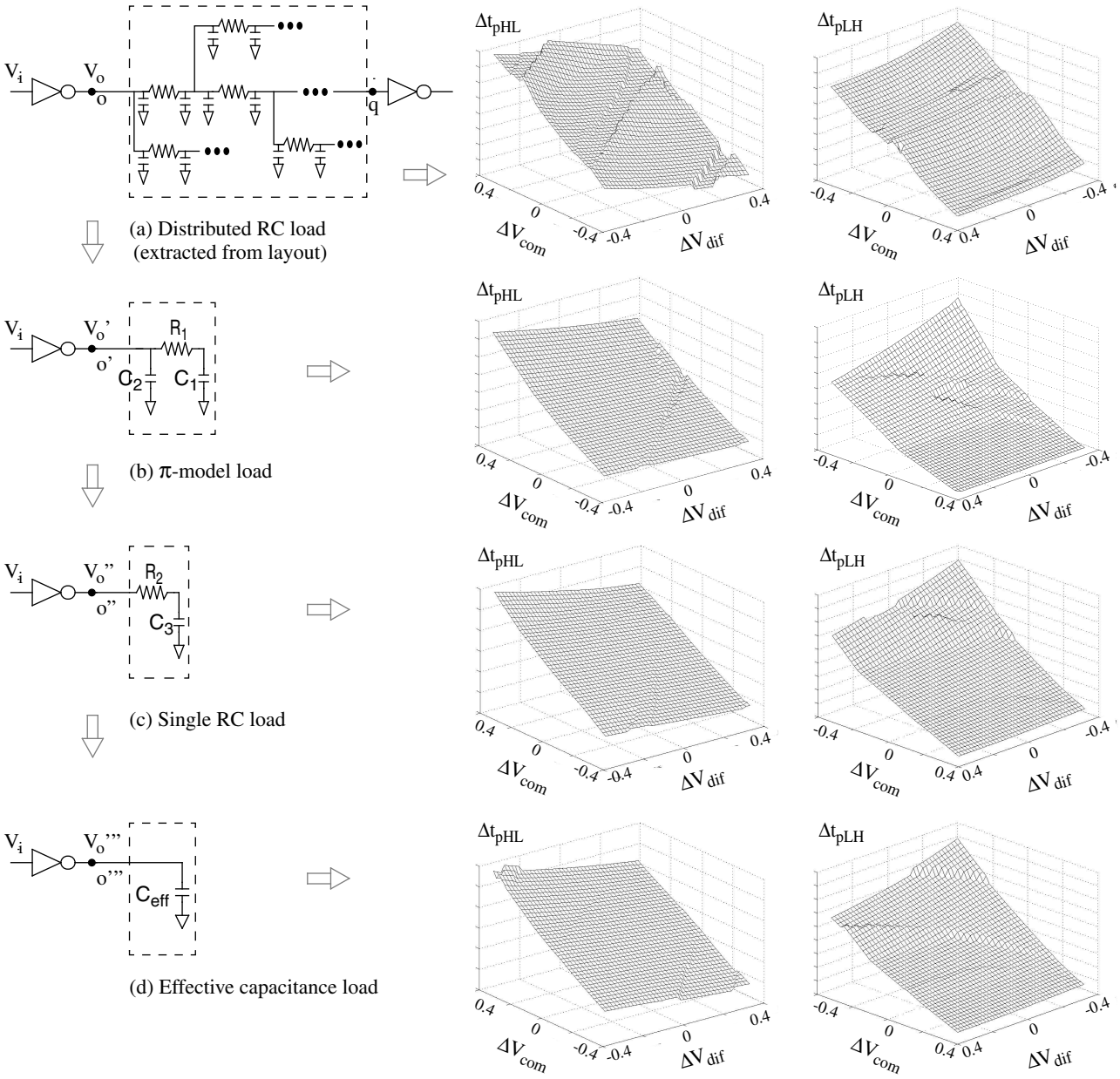


Figure 5. Buffer delay change induced by P/G noise

is usually less than ±10% .Thus, the CMN and DMN-induced delays can be superposed as noted below.

Observation 3: For a rising input transition and any of the wire load models described in figure 5, the incremental change of buffer delay due to P/G noise is expressed as:

$$\Delta t_{pHL} = k_{1r} \cdot (\Delta V_{dd} + \Delta V_{ss}) - k_{2r} \cdot (\Delta V_{dd} - \Delta V_{ss}) \quad (8)$$

A similar result applies to a falling input transition:

$$\Delta t_{pLH} = -k_{1f} \cdot (\Delta V_{dd} + \Delta V_{ss}) - k_{2f} \cdot (\Delta V_{dd} - \Delta V_{ss}) \quad (9)$$

where k_{1r}, k_{1f}, k_{2r} and k_{2f} are positive constants dependent only on input transition time, gate load, and the device and technology parameters. The actual expressions can be found from equations (11) and (14) in section 4.2, based on the theoretical model.

Observation 3 brings in two related observations.

Observation 4: Buffer delay change is more sensitive to common mode noise than to differential mode noise for deep submicron designs, and may be dominated by common mode noise in some instances. This is indicated by the fact that the slope along the ΔV_{com} direction is much steeper

than the slope along the ΔV_{dif} direction in figure 5. It also indicates $k_{1r} > k_{2r}$ and $k_{1f} > k_{2f}$ in equations (8) and (9). This will be further discussed in section 4.4.

Observation 5: Common mode noise has different effects on rising and falling transitions. As shown in figure 5, for a rising transition, with the *increase* of ΔV_{com} from -0.4 to 0.4 volt, delay change increases. However, for a falling transition, it is with the *decrease* of ΔV_{com} from 0.4 to -0.4 volt that the delay change increases. This is indicated by different signs associated with ($\Delta V_{dd} + \Delta V_{ss}$) in equations (8) and (9): positive for a rising and negative for a falling transition.

Observation 3 indicates that an appropriate simplified wire load model can be used for delay modeling of the buffer itself. With appropriate techniques [2][8][11][16], the distributed RC load of a gate can be simplified into the nearly equivalent π-model shown in figure 5(b). This π-model is further simplified into an effective capacitance load, shown in figure 5(d), by equating the average currents for the two load models. Such a capacitance model is inaccurate when the gate is behaving like a resistor [16]. This inaccuracy occurs primarily in the tail portion of the output waveform. However, for our purposes, the buffer delay is measured at the midpoint of the logic swing. Therefore, the inaccuracy in the gate delay (not the wire delay) caused by the effective capacitance model is relatively small, usually less than 5% for the technologies reported in the results.

The output voltage at node *o* in figure 5 (a) can be approximated by the voltage at node *o'* in figure 5 (b), *o"* in figure 5 (c) and *o"'* in figure 5 (d):

$$V_o \approx V_o' \approx V_o'' \approx V_o'''$$

However, the voltage at node *q* is different from that of node *o*:

$$V_q \neq V_o$$

The simplified wire load model is only used to characterize the interconnect's driving point (node *o*) delay, not the receiving node (node *q*) delay. A variety of techniques exist [5][11] in order to model the interconnect delay. In this paper, we focus only on the buffer delay characterization which is typically half of the total wire delay for optimized long wires.

Power and ground noise can either be correlated or largely independent depending on the relative magnitude of the power distribution parasitics and the relative number and activity of signals crossing between power distribution blocks. This noise contributes to the local buffer/inverter delay in a complex way which can either increase or decrease the signal delay. For application in performance estimation, optimization, or analysis, it is useful to develop simple models which can be quickly evaluated and which can be linked to theoretical device models.

4. THEORETICAL MODEL

4.1 Inverter model

In deep submicron circuits, carrier velocity saturation effects predominate. To capture these effects when deriving the signal transition delay and slope values in the presence of power and ground variations, we use the short channel alpha-power law MOSFET model [17].

From Figure 6, we have the following nodal equation:

$$I_n + I_p = I_c$$

where

$$I_c = -C_L \frac{d(V_o - V_{ss})}{dt}$$

In deep submicron circuits the signal transitions are fast, so we can ignore the short circuit current [17][18]. (For the technologies reported in the results, short circuit errors amounted to less than 5% for incremental delay and 20% for incremental transition time, over all simulated cases.) For a rising transition at the inverter input, short circuit current from the NFET is negligible.

The current flowing through NFET (I_n) is computed from the following equation [17]:

$$I_n = \begin{cases} 0 & (V_{GS} \le V_{tn})(CUT) \\ I_{D1} & (V_{DS} \ge V_{D1})(SAT) \\ (I_{D1}/V_{D1}) \cdot V_{DS} & (V_{DS} < V_{D1})(LIN) \end{cases} \quad (10)$$

where

$$I_{D1} = I_{D0}\left(\frac{V_{GS} - V_{tn}}{V_{dd} - V_{tn}}\right)^{\alpha} = I_{D0}\left(\frac{V_{in} - V_{tn}}{V_{dd} - V_{tn}}\right)^{\alpha}$$

$$V_{D1} = V_{D0}\left(\frac{V_{GS} - V_{tn}}{V_{dd} - V_{tn}}\right)^{\alpha/2} = V_{D0}\left(\frac{V_{in} - V_{tn}}{V_{dd} - V_{tn}}\right)^{\alpha/2}$$

CUT, *SAT*, and *LIN* represent *cutoff*, *saturation*, and *linear* modes of operation, respectively. And:

$$V_{in} = V_i - V_{ss} = V_{GS}$$

$$V_{out} = V_o - V_{ss} = V_{DS}$$

The above alpha-power law model is based on four parameters: α (velocity saturation index), V_{tn} (threshold

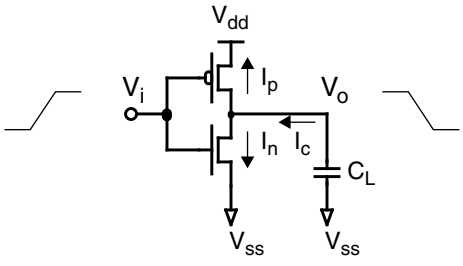


Figure 6. Propagation of a transition

voltage), I_{D0} (drain current at $V_{GS} = V_{DS} = V_{dd}$), V_{DO} (drain saturation voltage at $V_{GS} = V_{dd}$). For MOSFET in current technology, typical values for these parameters are: $\alpha = 1 \sim 1.2$, $V_{tn}/V_{dd} \approx 0.2$, and $V_{D0} \le 0.6 V_{dd}$. We assume that for a given transistor with a given loading capacitance, the above four values remain unchanged with a small disturbance of power supply and ground levels.

Figure 2 shows a typical traversal path for an inverter's operation mode when the input is a rising transition [17]. It is divided into four regions.

In the following two subsections, referring to figures 2~3, we will derive the output waveform and simple formulas to estimate the change of delay and slope induced by the change of V_{dd} and V_{ss}.

4.2 Change of buffer delay

The derivation of output waveform can be found in appendix A. According to the results in appendix A, we obtain t_{i5}', t_{o5}', t_{o1}', and t_{o9}'. By setting ΔV_{dd} and ΔV_{ss} to 0, we can obtain the corresponding t_{i5}, t_{o5}, t_{o1}, and t_{o9}. In order to differentiate between NFET and PFET, we use subscripts n and p to represent parameters related to NFET and PFET, respectively. According to equations (A5) and (A6) in appendix B, we have:

$$\begin{aligned} \Delta t_{pHL}^{(j)} &= k_{1n}^{(j)} \cdot \Delta V_{com} - k_{2n}^{(j)} \cdot \Delta V_{dif} \\ &= k_{1n}^{(j)} \cdot (\Delta V_{dd} + \Delta V_{ss}) - k_{2n}^{(j)} \cdot (\Delta V_{dd} - \Delta V_{ss}) \end{aligned} \tag{11}$$

The change of delay can also be expressed as:

$$\Delta t_{pHL}^{(j)} = k_{3n}^{(j)} \cdot \Delta V_{dd} + k_{4n}^{(j)} \cdot \Delta V_{ss} \tag{12}$$

where

$$k_{3n}^{(j)} = k_{1n}^{(j)} - k_{2n}^{(j)},\ k_{4n}^{(j)} = k_{1n}^{(j)} + k_{2n}^{(j)} \tag{13}$$

For the four types of delays defined in figure 3, we obtained the following coefficients:

$$k_{1n}^{(1)} = \frac{t_r}{2V_{dd}(1+\alpha)} + \frac{C_L}{2I_{D0}},\ k_{2n}^{(1)} = \frac{t_r}{2V_{dd}(1+\alpha)} - \frac{C_L}{2I_{D0}}$$

$$k_{1n}^{(2)} = -\frac{t_r}{2V_{dd}} \cdot \frac{\alpha}{1+\alpha},\ k_{2n}^{(2)} = \frac{t_r}{2V_{dd}(1+\alpha)} - \frac{C_L}{2I_{D0}}$$

$$k_{1n}^{(3)} = \frac{C_L}{2I_{D0}},\ k_{2n}^{(3)} = \frac{v_T \cdot t_r}{(1+\alpha)V_{dd}} - \frac{C_L}{2I_{D0}}$$

$$k_{1n}^{(4)} = 0,\ k_{2n}^{(4)} = \frac{C_L}{2I_{D0}} - \frac{v_T \cdot t_r}{(1+\alpha)V_{dd}}$$

Similar equations have been derived for $\Delta t_{pLH}^{(j)}$. The main difference is that the four parameters (α, V_{tp}, I_{D0}, V_{D0}) are obtained from the corresponding PMOS, and the polarity of k_{1p} is reversed compared to that of k_{1n}:

$$\begin{aligned} \Delta t_{pLH}^{(j)} &= -k_{1p}^{(j)} \cdot \Delta V_{com} - k_{2p}^{(j)} \cdot \Delta V_{dif} \\ &= k_{3p}^{(j)} \cdot \Delta V_{dd} + k_{4p}^{(j)} \cdot \Delta V_{ss} \end{aligned} \tag{14}$$

where

$$k_{3p}^{(j)} = -k_{1p}^{(j)} - k_{2p}^{(j)},\ k_{4n}^{(j)} = -k_{1p}^{(j)} + k_{2p}^{(j)} \tag{15}$$

Equations (11) and (14) match the results in observations 3, 4 and 5.

Theorem 1: Equations (11) to (15) demonstrate that the incremental change of buffer delay is linear with respect to the power and ground variations.

The coefficient k_1 quantifies the effect of the common mode noise while k_2 characterizes the effect of the differential mode noise on buffer delay. This theorem shows why the observations in sections 3.1 through 3.3 hold. k_{1n}, k_{2n}, k_{1p} and k_{2p} are equivalent to k_{1r}, k_{2r}, k_{1f} and k_{2f} defined in observation 3.

Under certain circumstances, the input transition time can be changed by the P/G noise. In other words, $\Delta t_r \neq 0$, and $t_r' = t_r + \Delta t_r$. The delay change will be slightly different:

$$\Delta t_{pHL}^{(j)} = k_{1n}^{(j)} \cdot (\Delta V_{dd} + \Delta V_{ss}) - k_{2n}^{(j)} \cdot (\Delta V_{dd} - \Delta V_{ss}) + \Delta t_r \cdot f_{ds}^{(j)}$$

where $f_{ds}^{(j)}$ is a function of P/G noise. For example, for the first type of delay change, we have:

$$f_{ds}^{(1)} = \frac{1}{2} - \frac{1}{1+\alpha} \cdot \left(1 - \frac{\Delta V_{ss}}{V_{dd}} - v_T\right)$$

which can be further simplified to:

$$\Delta t_{pHL}^{'(1)} = k_{1n}^{'(1)} \cdot (\Delta V_{dd} + \Delta V_{ss}) - k_{2n}^{'(1)} \cdot (\Delta V_{dd} - \Delta V_{ss}) + k_{5n}^{'(1)} \tag{16}$$

where

$$k_{1n}^{'(1)} = \frac{t_r + \Delta t_r}{2V_{dd}(1+\alpha)} + \frac{C_L}{2I_{D0}},$$

$$k_{2n}^{'(1)} = \frac{t_r + \Delta t_r}{2V_{dd}(1+\alpha)} - \frac{C_L}{2I_{D0}}$$

$$k_{5n}^{'(1)} = \Delta t_r \cdot \left(\frac{1}{2} - \frac{1 - v_T}{1+\alpha}\right)$$

Equation (16) can be transformed into a form similar to that of equation (12):

$$\Delta t_{pHL}^{'(1)} = k_{3n}^{'(1)} \cdot \Delta V_{dd} + k_{4n}^{'(1)} \cdot \Delta V_{ss} + k_{5n}^{'(1)} \tag{17}$$

where

$$k_{3n}^{'(1)} = \frac{C_L}{I_{D0}},\ k_{4n}^{'(1)} = \frac{t_r + \Delta t_r}{V_{dd}(1+\alpha)}$$

Similarly, for the other three types of buffer delay changes, we have:

$$k_{3n}^{'(2)} = \frac{C_L}{2I_{D0}} - \frac{t_r + \Delta t_r}{2V_{dd}}$$

$$k_{4n}^{'(2)} = -\frac{C_L}{2I_{D0}} + \frac{t_r + \Delta t_r}{2V_{dd}} \cdot \frac{1-\alpha}{1+\alpha}$$

$$k_{3n}^{'(3)} = \frac{C_L}{I_{D0}} + \frac{t_r + \Delta t_r}{V_{dd}} \cdot \left(\frac{1}{2} - \frac{v_T}{1+\alpha}\right)$$

$$k_{4n}^{'(3)} = \frac{t_r + \Delta t_r}{V_{dd}} \cdot \left(\frac{1}{2} + \frac{v_T}{1+\alpha}\right)$$

$$k_{3n}^{'(4)} = \frac{C_L}{2I_{D0}} - \frac{t_r + \Delta t_r}{V_{dd}} \cdot \frac{v_T}{1+\alpha}$$

$$k_{4n}^{'(4)} = -\frac{C_L}{2I_{D0}} + \frac{t_r + \Delta t_r}{V_{dd}} \cdot \frac{v_T}{1+\alpha}$$

$$k_{5n}^{'(j)} = \Delta t_r \cdot \left(\frac{1}{2} - \frac{1-v_T}{1+\alpha}\right) \quad (j = 2, 3, 4)$$

Lemma 1: Using equation (16), we can easily see that the buffer delay change is linearly related to the power and ground noise regardless of the change of input transition time.

4.3 The change of slope

According to equation (A9) in appendix B, we have the change of slope:

$$\Delta t_{oT} = h_3 \cdot \Delta V_{dd} + h_4 \cdot \Delta V_{ss} \qquad (18)$$

where h_3 and h_4 are determined by the device and technology parameters, input transition time, and the gate load.

4.4 Discussion

In this section, based on the derived equations, we discuss related issues and special cases.

4.4.1 The trend with technological scaling

With shrinking feature sizes, future deep submicron circuits have decreased power supply value V_{dd} and decreased velocity saturation index α, leading to increased values for the coefficients in equation (11). As a consequence, the buffer delay will become more sensitive to the same power and ground variations despite better packaging.

In classic wire-bond packaging, the power and ground noise were closely correlated for the whole chip. Hence it was appropriate to measure the delay at the 50% point of the changed power supply and ground level. We considered $\Delta t_{pHL}^{(4)}$ as the default value for the high-to-low delay change. It is dominated by the differential mode noise induced effect, because $k_{1n}^{(4)} = 0$.

However, in modern packaging, bump-bond techniques are used. The power and ground noise of each block/cell can be relatively independent of all others. Bump bonding has significantly lower parasitics overall - this means that the on-chip distribution network is more important, but only because the sensitivity has increased and the slew rates have increased. It is then appropriate to measure the delay at the 50% point of the ideal power supply and ground level. We consider $\Delta t_{pHL}^{(1)}$ as the default value for high-to-low delay change. It is more sensitive to the common-mode-noise induced delays, because $k_{1n}^{(1)} > k_{2n}^{(1)}$. This matches the simulation results shown in figure 5 and observation 4.

4.4.2 Power v.s. ground variation

As we mentioned in section 2.1, power and ground variations are related, but not necessarily correlated. Different combinations of variations exist. Usually IR-drop is discussed when assuming $\Delta V_{dd} < 0$ and $\Delta V_{ss} = 0$. Ground-bounce is another special case when $\Delta V_{ss} > 0$ and $\Delta V_{dd} = 0$. We list more special cases below.

1. Buffer delay change can be positive (slowdown) or negative (speedup), depending on the polarity of P/G noise, the relative amplitude between ΔV_{dd} and ΔV_{ss}, and the coefficients in equation (11).
2. When the changes of power and ground are in the same direction and have similar amplitudes, we have $|\Delta V_{ss} - \Delta V_{dd}| \ll |\Delta V_{ss} + \Delta V_{dd}|$. According to equation (11), the buffer delay change will be dominated by the effect induced by common mode noise for $\Delta delay = \Delta t_{pHL}^{(1)}$. However for the fourth type of delay change, we will have $\Delta delay = \Delta t_{pHL}^{(4)} \approx 0$.

   On the other hand, when ΔV_{dd} and ΔV_{ss} change in the opposite directions and have similar amplitudes, we have $|\Delta V_{ss} + \Delta V_{dd}| \ll |\Delta V_{ss} - \Delta V_{dd}|$. In such a case, if $k_{3n}^{(1)} \ll k_{4n}^{(1)}$, then $k_{1n}^{(1)} \approx k_{2n}^{(1)}$, and the buffer delay change will be dominated by the effect induced by the differential mode noise for $\Delta delay = \Delta t_{pHL}^{(1)}$. $\Delta t_{pHL}^{(4)}$ is always dominated by the effect of differential mode noise because $k_{1n}^{(4)} = 0$.
3. Suppose that, at a certain time period, only power variation exists, i.e. $\Delta V_{ss} = 0$. This degrades to a special case described in [19]. For such a case, buffer delay change is linearly proportional to ΔV_{dd}. In fact in [19] it has been experimentally verified that "a given percentage of V_{dd} variation translates directly to the same percentage of delay variation.
4. Similarly, when there is only a ground variation, buffer delay change is proportional to the ΔV_{ss}.

4.4.3 Definitions of delay

The expressions for delay and slope depend on how we define Δt_{pHL} and Δt_{OT}. We obtained our formulas in appendix A and B based on typical cases. Comparing these four different delay definitions, we can see that the same P/G noise has different effects on different $\Delta delay$. Even though different coefficients have been obtained, they all follow theorem 1.

Parameter					0.25μm						0.18μm					
					Simulation		Our Method				Simulation		Our Method			
W_p/W_n (μm)	C_L (ff)	t_r (ps)	ΔV_{dd} (volt)	ΔV_{ss} (volt)	Δt_{pHL} (ps)	Δt_{oT} (ps)	Δt_{pHL} (ps)		Δt_{oT} (ps)		Δt_{pHL} (ps)	Δt_{oT} (ps)	Δt_{pHL} (ps)		Δt_{oT} (ps)	
10/5	100	100	-0.250	-0.250	-21.93	-4.198	**-21.23**	**3.2%**	-4.849	15%	-24.94	-10.71	**-24.50**	**1.8%**	-12.87	20.1%
10/5	100	100	0.00	-0.100	-4.729	0.169	**-4.694**	**0.7%**	0.167	1.1%	-6.224	-2.943	**-5.970**	**4.0%**	-2.598	11.9%
10/5	100	100	0.025	0.100	5.402	0.421	**5.644**	**4.5%**	0.418	0.7%	6.950	2.955	**6.927**	**0.3%**	3.138	6.2%
10/5	100	100	0.100	0.00	3.760	2.043	**3.800**	**1.0%**	2.007	1.8%	3.708	2.680	**3.828**	**3.2%**	2.893	8.0%
10/5	20	50	-0.500	0.025	-6.045	-1.683	**-5.701**	**5.6%**	-1.768	5.1%	-8.085	-6.923	**-7.802**	**3.5%**	-6.238	9.9%
10/5	20	50	0.500	0.100	8.599	2.715	**8.195**	**4.7%**	2.525	7.0%	9.729	1.551	**10.22**	**5.0%**	1.472	5.1%
5/5	100	100	0.250	0.100	14.13	5.366	**14.35**	**1.6%**	4.926	8.2%	17.30	3.639	**16.46**	**4.9%**	3.139	13.7%
5/5	100	100	0.500	-0.025	16.47	10.15	**17.04**	**3.4%**	10.24	0.8%	19.15	7.701	**18.06**	**5.5%**	7.185	6.7%
5/5	100	50	0.025	-0.250	8.294	-4.856	**8.686**	**4.7%**	-5.137	5.8%	8.524	1.677	**8.945**	**4.9%**	1.467	12.5%
10/10	100	100	-0.250	0.050	-4.694	-10.08	**-4.644**	**1.1%**	-11.78	16.8%	-4.733	-2.203	**-4.491**	**5.1%**	-2.273	3.2%

Table 1: Validation of expressions for incremental buffer delay and slope changes

4.4.4 Change of waveform

Delay expressions will be different when the input/output waveforms differ from the ones shown in figure 2-3. Through HSPICE simulations, we have observed that the cases shown in figure 2-3 are typical for deep submicron circuits. When t_{o5} and t_{o5}' fall in region 2 or region 4, the expression for Δt_{pHL} becomes a little more complicated, but is still closed form. We don't list all corner cases here.

5. MODEL VALIDATION

We validated our model in both 0.25μm and 0.18μm technologies. As mentioned in section 4.1, the alpha-power law MOSFET model relies on four parameters: α, V_{tn}, I_{D0} (drain current at $V_{GS} = V_{DS} = V_{dd}$), V_{DO} (drain saturation voltage at $V_{GS} = V_{dd}$). These four parameters are not listed in the technology files. We determined these values for each transistor through HSPICE simulation. The extraction of I_{D0} and V_{DO} are straightforward. We follow the method in [17] to extract α and V_{tn}.

Table 1 shows our calculated variations in delay and slope compared to HSpice simulation, for a single inverter with different parameters, in different technologies. 10 sets of data are shown. Incremental delays for very fast (<50pS) rise times are not shown, for they are more accurately modeled than the presented data are. To achieve very high slew rates, wire parasitics are necessarily low so that conventional gate-to-gate nominal delay characterization works well. The approximations made in the incremental delay change model work better for fast slew rates since the short circuit current is reduced, and feed-forward capacitive coupling is modeled in the nominal delay.

In the results, we can see that the model provides accurate estimation for delay variations (Δt_{pHL}), with less than 5% error relative to HSPICE over a ±20% supply variation range. The model is not as accurate in estimating the change of transition time (Δt_{oT}). For delay estimation, this is acceptable because Δt_{oT} has only a second order effect on the delay of the next stage. Note that this modeling technique applies to arbitrary size inverters, loading capacitance, and input transition times. Comparison of the technologies shows the trend of increasing sensitivity to supply-level noise with scaling.

6. APPLICATIONS

An important feature of the model is its relative lack of dependence on the circuit loading structure. This simplifies inclusion in a design flow as a modification to the existing delay calculation. Iterations may result, because the updated delay will further affect the power and ground level. Since our formulas are very simple, an iterative process may be affordable. This section will show some applications of our modeling technique.

6.1 Delay change for special buffer design

To preserve duty cycle, clock buffer chain designs often presume equal input and output transition times. Thus:

$$t_r = \frac{0.9C_L}{0.8I_{D0}}V_{dd} + \frac{C_L V_{D0}}{0.8I_{D0}} \cdot \ln\left(\frac{10V_{D0}}{eV_{dd}}\right)$$

$$\Delta t_r = \frac{0.9C_L}{0.8I_{D0}}(\Delta V_{dd} - \Delta V_{ss}) + \frac{C_L V_{D0}}{0.8I_{D0}} \cdot \ln\left(\frac{V_{dd}}{V_{dd} + \Delta V_{dd} - \Delta V_{ss}}\right)$$

Substituting t_r and Δt_r into equation (11), we have:

$$\Delta t_{pHL}^{(j)} = \frac{C_L}{I_{D0}} \cdot (f_{1n}^{(j)} \cdot \Delta V_{com} - f_{2n}^{(j)} \cdot \Delta V_{dif}) \quad (j = 1 \sim 4) \quad (19)$$
$$= \frac{C_L}{I_{D0}} \cdot (f_{3n}^{(j)} \cdot \Delta V_{dd} + f_{4n}^{(j)} \cdot \Delta V_{ss})$$

where

$$f_{1n}^{(j)} = (f_{3n}^{(j)} + f_{4n}^{(j)})/2\,,\ f_{2n}^{(j)} = (f_{4n}^{(j)} - f_{3n}^{(j)})/2 \qquad (20)$$

When Δt_r is ignored, we have:

$$f_{3n}^{(1)} = 1\,,\ f_{4n}^{(1)} = \frac{1}{1+\alpha}\cdot f_{01}$$

$$f_{3n}^{(2)} = \frac{1}{2} - \frac{1}{2}\cdot f_{01}\,,\ f_{4n}^{(2)} = -\frac{1}{2} + \frac{1}{2}\cdot\frac{1-\alpha}{1+\alpha}\cdot f_{01}$$

$$f_{3n}^{(3)} = 1 + \left(\frac{1}{2} - \frac{v_T}{1+\alpha}\right)\cdot f_{01}\,,\ f_{4n}^{(3)} = \left(\frac{1}{2} + \frac{v_T}{1+\alpha}\right)\cdot f_{01}$$

$$f_{3n}^{(4)} = \frac{1}{2} - \frac{v_T}{1+\alpha}\cdot f_{01}\,,\ f_{4n}^{(4)} = -\frac{1}{2} + \frac{v_T}{1+\alpha}\cdot f_{01}$$

If Δt_r is not negligible, we have:

$$\Delta t_{pHL}^{(j)} = \frac{C_L}{I_{D0}}\cdot(f_{3n}^{(j)'}\cdot\Delta V_{dd} + f_{4n}^{(j)'}\cdot\Delta V_{ss})\ (j = 1 \sim 4) \qquad (21)$$

where

$$f_{3n}^{(j)'} = f_{3n}^{(j)} + f_{03}\,,\ f_{4n}^{(j)'} = f_{4n}^{(j)} - f_{03}$$

where

$$f_{01} = \frac{0.9}{0.8} + \frac{V_{D0}}{0.8V_{dd}}\cdot\ln\left(\frac{10V_{D0}}{eV_{dd}}\right)$$

$$f_{02} = \frac{0.9}{0.8} - \frac{V_{D0}}{0.8V_{dd}}$$

$$f_{03} = \left(\frac{1}{2} - \frac{1-v_T}{1+\alpha}\right)\cdot f_{02}$$

For a falling transition, we have:

$$\Delta t_{pLH}^{(j)} = \frac{C_L}{I_{D0}}\cdot(-f_{1p}^{(j)}\cdot\Delta V_{com} - f_{2p}^{(j)}\cdot\Delta V_{dif}) \qquad (22)$$

Note that equations (19) ~ (22) are independent of input slope. This result is used below to determine the cumulative jitter in a buffer chain.

6.2 Different buffer chains

The linear relationship between the P/G noise and delay change can be used to analyze the delivered jitter for a chain of single-inverter-buffers and a chain of double-inverter-buffers, as shown in figure 7.

Assume the input is a rising transition. For one stage of a single-inverter-buffer, we have from equation (19):

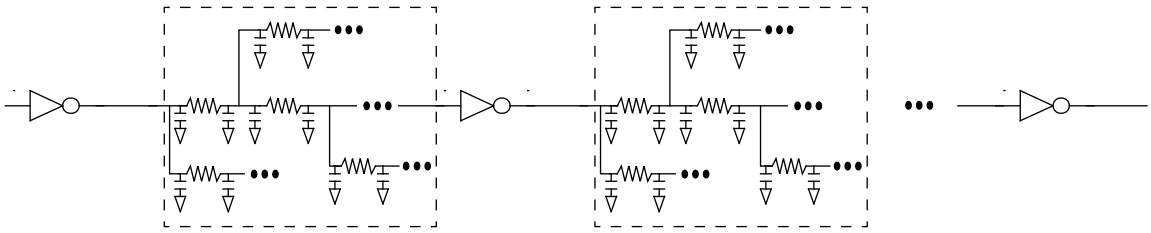
$$\Delta delay^{(s)} = \Delta t_{pHL}^{(s)} = \frac{C_L}{I_{D0}^{(s)}}\cdot(f_{1n}^{(s)}\cdot\Delta V_{com} - f_{2n}^{(s)}\cdot\Delta V_{dif}) \qquad (23)$$

For one stage of a double-inverter-buffer, we assume a tapered buffer design. According to equations (19) and (22), we have,

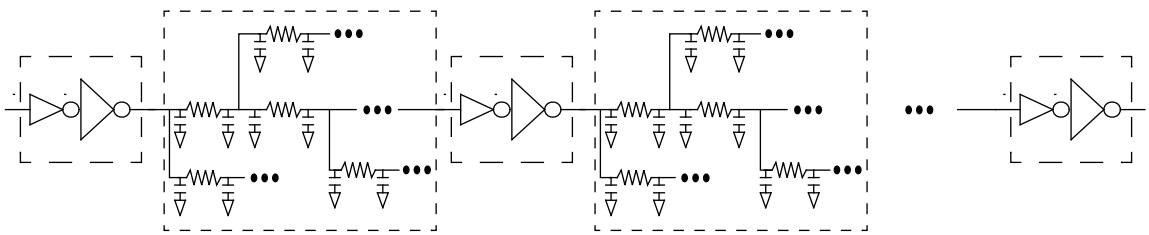
$$\Delta delay^{(d)} = \Delta t_{pHL}^{(d)} + \Delta t_{pLH}^{(d)} = \frac{C_L}{I_{D0}^{(d)}}\cdot[(f_{1n}^{(d)} - f_{1p}^{(d)})\cdot\Delta V_{com} - (f_{2n}^{(d)} + f_{2p}^{(d)})\cdot\Delta V_{dif}] \qquad (24)$$

where the superscripts (s) and (d) denote the corresponding parameters for single-inverter-buffer and double-inverter-buffer, respectively. And we assume the parameters for both buffer designs are comparable.

In deep submicron technologies, the buffer delay change is more sensitive to the common mode noise than to the differential mode noise. This has been experimentally demonstrated by our simulation results in figure 5, and theoretically proved by our equation (11) which indicates $k_{1n}^{(1)} > k_{2n}^{(1)}$. In other words, we have:



(a) Single-inverter-buffer chain



(b) Double-inverter-buffer chain

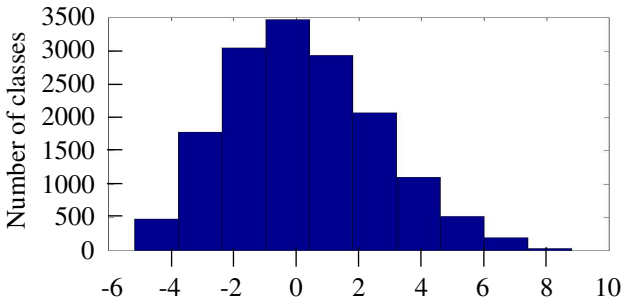
Figure 7. Delay change for single-inverter chain v.s. double-inverter chain

$f_{1n}^{(s)} > f_{2n}^{(s)}$, $f_{1n}^{(d)} > f_{2n}^{(d)}$, $f_{1p}^{(d)} > f_{2p}^{(d)}$

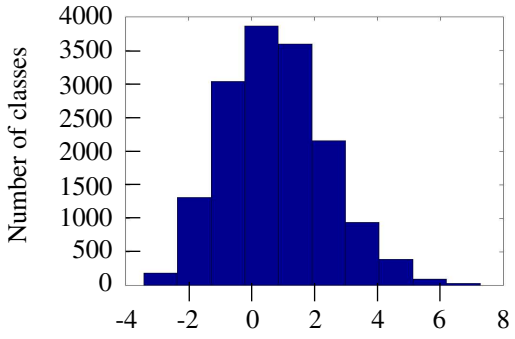
When the amplitude of the common mode noise is at least as large as that of the differential mode noise, the delay change of both buffer designs will be dominated by common mode noise. However, when $f_{1n}^{(d)}$ and $f_{1p}^{(d)}$ are comparable, the delay change induced by common mode noise from equation (24) will cancel while the delay change given by the equation (23) will dominate. Hence, we make the following observation:

Observation 6: The delay of a double-inverter-buffer chain is less sensitive to the power/ground noise variations than that of a single-inverter-buffer chain.

Figure 8 shows simulation results of buffer delay change for the buffer chains shown in figure 7. The power/ground noise of each buffer in the chain is independent of the others and ranges over ±10% of V_{dd}. Inverter sizes are determined such that both buffer chains in figure 7 have a similar nominal delay (around 280ps). This is done to simplify comparison of the delay changes, because buffer chains with un-correlated delay would be difficult to compare. We choose similar wire loads for each stage. We randomly simulate 20000 combinations of P/G noise induced jitter. The statistics in figure 8 clearly show that the overall delivered jitter (total delay change of the buffer chain) for the double-inverter buffers is smaller than that of a single-inverter buffer chain. In other words, a single-inverter buffer chain has larger delay uncertainty than the double-inverter buffer chain. This provides us a new guideline for design: in terms of power/ground noise avoidance, the double-inverter buffer chain is a better choice. Double-inverter buffers have slightly larger current requirements than inverters due both to tapering and to the domination of load capacitance by the interconnect, so the effect of additional current is minor. This result is affected by rapidly changing power levels primarily in the slow rise-time (RC dominated) extents of the interconnect. However, such effects should be similar for both styles of repeater.



(a) Delay change for a single-inverter-buffer chain (multiply by 10ps)



(b) Delay change for a double-inverter-buffer chain (multiply by 10ps)

Figure 8. Comparison of buffer delay change (histogram)

7. CONCLUSION

Maintaining signal integrity in deep submicron circuits is a difficult problem. Variations of power and ground levels play an important role because this type of noise significantly degrades circuit performance. Deep submicron circuits have decreased power supply level V_{dd} and decreased velocity saturation index α, leading to increased sensitivity of delay to P/G noise. Thus, despite the reduction of noise from lower-inductance packaging, the relative magnitude of the delay changes is still a serious potential problem.

We studied the effects of differential and common mode power/ground noise on buffer delay. Using the α-power law MOSFET model, we derived general formulas to estimate the influence of power and ground noise on delay and slope. As our model does not rely on the circuit structure, it can be incorporated into any existing gate delay calculation techniques. It is simple and accurate. An application in clock buffer chain design shows that repeater chains, using buffers instead of inherently faster inverters, tend to have superior level - induced delay characteristics.

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APPENDIX A: DERIVING THE OUTPUT WAVEFORM IN THE PRESENCE OF POWER AND GROUND NOISE

We first derive the output waveform for figure 3(a). The derivation is based on the definitions from figures 2 and 3(a).

$$V_{in}^{'} = V_{i}^{'} - \Delta V_{ss} = \frac{t}{t_r} \cdot V_{dd} - \Delta V_{ss}$$

In region 1, NMOS is in cutoff. So we have:

$$V_{out}^{'} = V_{dd} + \Delta V_{dd} - \Delta V_{ss} \left(0 \le t \le \frac{\Delta V_{ss} + V_{tn}}{V_{dd}} \cdot t_r \right) \quad \text{(A1)}$$

In region 2, NMOS is in saturation mode, and the input is defined by equation (10). The output waveform satisfies the following differential equation:

$$C_L \frac{dV_{out}^{'}}{dt} = -I_{D0} \left(\frac{V_{in}^{'} - V_{tn}}{V_{dd} + \Delta V_{dd} - V_{tn}} \right)^{\alpha}$$

Let $v_T = V_{tn}/V_{dd}$. With initial condition $V_{in}^{'} = V_{tn}$, $V_{out}^{'} = V_{dd} + \Delta V_{dd} - \Delta V_{ss}$, we get:

$$V_{out}^{'} = (V_{dd} + \Delta V_{dd} - \Delta V_{ss}) - \frac{I_{D0} \cdot t_r}{C_L} \cdot g(t) \quad \text{(A2)}$$

$$\left(\text{region 2: } \frac{(\Delta V_{ss} + V_{tn}) \cdot t_r}{V_{dd}} \le t \le t_r \right)$$

where

$$g(t) = \frac{\left(\frac{t}{t_r} - \frac{\Delta V_{ss}}{V_{dd}} - v_T \right)^{1+\alpha}}{(1+\alpha) \left(1 + \frac{\Delta V_{dd}}{V_{dd}} - v_T \right)^{\alpha}}$$

Referring to figure 3, we have:

$$V_{TR}^{'} = V_{out}^{'}(t = t_r)$$

In region 3, NMOS is still in saturation mode. But the input is fixed at:

$$V_{in}^{'} = V_{dd} - \Delta V_{ss}$$

Substituting the above equation into region 2's differential equation, with initial condition (t_r, $V_{TR}^{'}$), we get:

$$V_{out}^{'} = (V_{dd} + \Delta V_{dd} - \Delta V_{ss}) - \frac{I_{D0} \cdot k_v}{C_L} \cdot [t - t_{\alpha}^{'}] \qquad \text{(A3)}$$

$$\text{(region 3: } t_r \le t \le t_{D0}^{'}\text{)}$$

where

$$t_{\alpha}^{'} = t_r \cdot \left(1 - \frac{1 - \frac{\Delta V_{ss}}{V_{dd}} - v_T}{1 + \alpha} \right)$$

and $t_{D0}^{'}$ is the time when $V_{out}^{'} = V_{D0}$, expressed as follows:

$$t_{D0}^{'} = \frac{C_L}{I_{D0} \cdot k_{v1}} \cdot (V_{dd} + \Delta V_{dd} - \Delta V_{ss} - V_{D0}) + t_{\alpha}^{'}$$

where

$$k_{v1} = \left(\frac{V_{dd} - \Delta V_{ss} - V_{tn}}{V_{dd} + \Delta V_{dd} - V_{tn}} \right)^{\alpha} \approx 1$$

In region 4, the input is the same as in region 3, but NMOS goes into linear operation mode. The discharging process is described by the following differential equation:

$$C_L \frac{dV_{out}^{'}}{dt} = -\frac{I_{D0}}{V_{D0}} \left(\frac{V_{dd} - \Delta V_{ss} - V_{tn}}{V_{dd} + \Delta V_{dd} - V_{tn}} \right)^{\alpha/2} V_{out}^{'}$$

Substituting the initial condition (t_{D0}', V_{D0}), we get:

$$V_{out}^{'} = V_{D0} e^{-(t - t_{D0}^{'})/(C_L R_3^{'})} \quad \text{(region 4: } t \ge t_{D0}\text{)} \qquad \text{(A4)}$$

where

$$R_3^{'} = \frac{V_{D0}}{I_{D0} k_{v2}}, \; k_{v2} = \sqrt{k_{v1}} \approx 1$$

When $\Delta V_{dd} = \Delta V_{ss} = 0$, equations (A1), (A2), (A3) and (A4) describe the output waveform with ideal V_{dd} and V_{ss}.

Similar results were obtained when the inverter has a falling transition at its input. In such a case, we consider PMOS to be on, and NMOS to be off. PMOS will start from its cutoff region, traverse the saturation region and finally settle in its linear region.

A similar procedure can be applied to obtain the output waveform for figure 3(b).

APPENDIX B: DERIVING THE BUFFER DELAY CHANGE

We use the derivation of $\Delta t_{pHL}^{(1)}$ as an example. Derivation and the results for the other three types are similar.

According to the results in appendix A, we obtain t_{i5}', t_{o5}', t_{o1}', t_{o9}' and t_{D0}'. By setting ΔV_{dd} and ΔV_{ss} to 0, we can obtain the corresponding t_{i5}, t_{o5}, t_{o1}, t_{o9} and t_{D0}. Therefore, we have:

$$t_{i5} = \frac{t_r}{2}$$

$$t_{o5} = \frac{C_L V_{dd}}{2 I_{D0}} + \frac{v_T + \alpha}{1 + \alpha} \cdot t_r$$

$$t_{o1} = t_{D0} + C_L R_3 \cdot \ln\left(\frac{10 V_{D0}}{V_{dd}} \right)$$

$$t_{o9} = t_r v_T + t_r \left[\frac{V_{dd} C_L}{10 I_{D0} t_r} \cdot (1 + \alpha)(1 - v_T)^{\alpha} \right]^{1/(1+\alpha)}$$

According to figure 3, for the signal transition with disturbed V_{dd} and V_{ss}, we have:

$$t_{i5}^{'(1)} = \frac{t_r}{2}$$

$$t_{o5}^{'(1)} = \frac{C_L}{I_{D0} k_{v1}} \cdot \left(\frac{V_{dd}}{2} + \Delta V_{dd} \right) + t_{\alpha}^{'}$$

where $t_{\alpha}^{'}$ is defined in appendix A.

$$t_{o1}^{'(1)} = t_{D0}^{'} + C_L R_3^{'} \cdot \ln\left(\frac{10 V_{D0}}{V_{dd} + \Delta V_{dd} - \Delta V_{ss}} \right)$$

where t_{D0}' and R_3' are defined in appendix A.

$$t_{o9}^{'(1)} = t_r \cdot \left[\frac{\Delta V_{ss}}{V_{dd}} + v_T + (q)^{1/(1+\alpha)} \right]$$

where

$$q = \frac{C_L V_{dd}}{10 I_{D0} t_r} \cdot (1 + \alpha) \left(1 + \frac{\Delta V_{dd} - \Delta V_{ss}}{V_{dd}} \right) \left(1 + \frac{\Delta V_{dd}}{V_{dd}} - v_T \right)^{\alpha}$$

According to the definitions in section 3.2, we obtain:

$$\Delta t_{pHL}^{(1)} = k_1^{(1)} \cdot (\Delta V_{dd} + \Delta V_{ss}) - k_2^{(1)} \cdot (\Delta V_{dd} - \Delta V_{ss}) \qquad \text{(A5)}$$

where

$$k_1^{(1)} = \frac{t_r}{2 V_{dd}(1 + \alpha)} + \frac{C_L}{2 I_{D0}}, \; k_2^{(1)} = \frac{t_r}{2 V_{dd}(1 + \alpha)} - \frac{C_L}{2 I_{D0}}$$

The change of delay can also be expressed as:

$$\Delta t_{pHL}^{(1)} = k_3^{(1)} \cdot \Delta V_{dd} + k_4^{(1)} \cdot \Delta V_{ss} \qquad \text{(A6)}$$

where

$$k_3^{(1)} = k_1^{(1)} - k_2^{(1)}, \; k_4^{(1)} = k_1^{(1)} + k_2^{(1)}$$

We also obtain the change of slope as follows:

$$\Delta t_{oT}^{(1)} = (\Delta t_{oT1} + \Delta t_{oT2} + \Delta t_{oT3} + \Delta t_{oT4})/0.8 \quad \text{(A7)}$$

where

$$\Delta t_{oT1} = \frac{C_L}{I_{D0}} \cdot (\Delta V_{dd} - \Delta V_{ss})$$

$$\Delta t_{oT2} = \frac{C_L}{I_{D0}} \cdot V_{D0} \cdot \ln\left(\frac{V_{dd}}{V_{dd} + \Delta V_{dd} - \Delta V_{ss}}\right)$$

$$\Delta t_{oT3} = t_r \cdot \frac{\alpha}{1+\alpha} \cdot \frac{-\Delta V_{ss}}{V_{dd}}$$

$$\Delta t_{oT4} = t_r \cdot p_0 \cdot [(1 - v_T)^{\alpha/(1+\alpha)} - p_1]$$

$$p_0 = \left[\frac{C_L V_{dd}(1+\alpha)}{10 I_{D0} t_r}\right]^{1/(1+\alpha)}$$

$$p_1 = \left(1 + \frac{\Delta V_{dd} - \Delta V_{ss}}{V_{dd}}\right) \cdot \left(1 + \frac{\Delta V_{dd}}{V_{dd}} - v_T\right)^{\alpha/(1+\alpha)}$$

By applying a Taylor expansion, we obtain:

$$\Delta t_{oT2} = -\frac{C_L \cdot V_{D0}}{I_{D0} \cdot V_{dd}} \cdot (\Delta V_{dd} - \Delta V_{ss})$$

$$\Delta t_{oT4} = t_r \cdot p_0 \cdot \left(-\frac{1 + 2\alpha - \alpha v_T}{1+\alpha} \cdot \frac{\Delta V_{dd}}{V_{dd}} + \frac{1 + \alpha - \alpha v_T}{1+\alpha} \cdot \frac{\Delta V_{ss}}{V_{dd}}\right)$$

Therefore the change of output slope can be simplified as follows:

$$\Delta t_{oT}^{(1)} = h_1^{(1)} \cdot (\Delta V_{dd} + \Delta V_{ss}) - h_2^{(1)} \cdot (\Delta V_{dd} - \Delta V_{ss}) \quad \text{(A8)}$$

or,

$$\Delta t_{oT}^{(1)} = h_3^{(1)} \cdot \Delta V_{dd} + h_4^{(1)} \cdot \Delta V_{ss} \quad \text{(A9)}$$

where

$$h_1^{(1)} = \frac{h_3^{(1)} + h_4^{(1)}}{2}, \; h_2^{(1)} = \frac{h_4^{(1)} - h_3^{(1)}}{2}$$

$$h_3^{(1)} = \frac{1}{0.8}\left[\frac{C_L}{I_{D0}} \cdot \left(1 - \frac{V_{D0}}{V_{dd}}\right) - \frac{(1 + 2\alpha - \alpha v_T) \cdot p_0 \cdot t_r}{(1+\alpha) \cdot V_{dd}}\right]$$

$$h_4^{(1)} = \frac{1}{0.8}\left[-\frac{C_L}{I_{D0}} \cdot \left(1 - \frac{V_{D0}}{V_{dd}}\right) + \frac{[(1 + \alpha - \alpha v_T) p_0 - \alpha] \cdot t_r}{(1+\alpha) \cdot V_{dd}}\right]$$