3

Transistors at DC

In this lab you will experiment with the three types of transistors: JFETs, BJTs, and MOSFETs. Later coursework (ECE132) will teach you about the physics of how these devices work. Our goal in ECE2 is more practical and focused on *using* the devices: understanding their current-voltage characteristics, and learning how to configure the circuit environment for the transistor to set the appropriate biasing conditions.

In this lab we will not build any clever functional circuits; the goal is simply to learn how to bias transistors correctly. This is always the first step in transistor circuit design, and is **crucial** to determining the success or failure of the circuit. In fact, most of the mistakes made by beginning students with transistor circuits can usually be traced to incorrect DC biasing.

Pre-lab Preparation

Before Coming to the Lab

- □ Read through the lab experiment to familiarize yourself with the components and assembly sequence.
- □ Calculate the bias resistor values that are required in each of the steps. This will save you time during the lab experiment
- □ Each group should obtain a parts kit from the ECE Shop.

Parts List

Use stocked cabinet in lab and the bench decade box for any required resistors

Laboratory #3	
Intro to Transistors	
Qty	**Description**
2	2N5485 n-ch JFET
2	2N7000 NMOS
2	2N3904 NPN BJT
2	2N3906 PNP BJT
1	CD4007 CMOS pair/inverter
1	1uF capacitor (electrolytic, 25V, radial)
2	Red LED (20mA)

Background information

Suggested background reading:

- Sedra & Smith: Sections 4.2-4.5, 5.2-5.5 (excellent stuff on MOS and BJTs, although somewhat more rigorous in detail than we need here).

Transistor Basics

Familiar two-terminal components such as resistors, capacitors, and diodes, are defined electrically by the current-voltage characteristic, $I(V)$, as in Figure 3-1a. Transistors differ in that they have a third terminal, shown conceptually in Figure 3-1b, which serves as a control point to manipulate the current flow through the device. The ability to control the current flow through one part of the device using a separate electrical signal is what makes transistors useful.

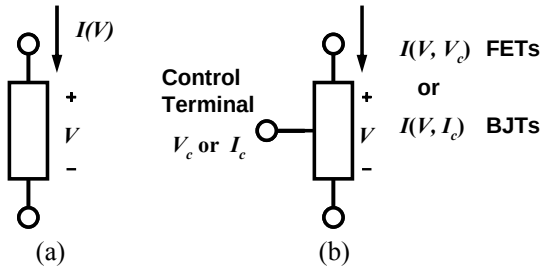

Figure 3-1 – (a) Two-terminal device (resistors, diodes, etc). (b) A three-terminal device (transistors fall in this category, but there are others as well!).

There are two main types of transistors that are grouped according to whether the I-V characteristics depend on the voltage or current at the control terminal. In "Field-Effect Transistors", or FETs, the I-V curve is a function of the *voltage* (electric field) at the control terminal. In "Bipolar Junction Transistors", or BJTs, the I-V curve depends on the *current* flowing into the control terminal. We say that *FETs are voltage-controlled devices*, and *BJTs are current-controlled devices*.

The detailed physics of how transistors work internally is somewhat complicated, but from a circuit standpoint, *using* the devices isn't all that hard: we just need to understand the general features of the I-V relationship and its dependence on the control terminal voltage or current. We will investigate the I-V characteristics of both FETS and BJTs in this lab, and start to learn how to use them in applications.

Before going on, we should also note that transistors aren't the only type of three-terminal electronic device. An electromechanical relay, which is a current-controlled switch, can be thought of in similar terms. Vacuum-tube triodes, early predecessors of the modern transistor, are close cousins of FETs; in fact an early name for the transistor was the "solid-state triode". There are also other semiconductor devices that have a third control terminal but differ from the transistor in some important ways: the silicon-controlled rectifier and thyristor are examples, used in power control applications.

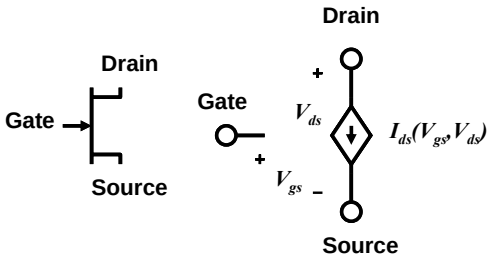

Figure 3-2 – Symbol for an n-channel JFET, and conceptual equivalent circuit for DC biasing.

Junction Field-Effect Transistors

Figure 3-2 shows the symbol for a type of FET called a Junction FET, or JFET. The three terminals are called the drain, source, and gate. In any FET, a conducting pathway (the "channel") connects the drain and source terminals, and the number of charge carriers in that channel can be manipulated by the

voltage on the gate. The "source" is the place where the charge carriers enter the channel, and after passing through the "gate" region they exit at the "drain". In an "n-channel" FET like the one shown in Figure 3-2, the charge carriers are electrons (the "n" is for "negative charge"), and so the current flow is opposite to the flow of electrons. We'll discuss the opposite device, the "positive"-channel FET later.

A nice feature of FETs is that the DC gate current is negligibly small, so the gate terminal is essentially an open circuit at DC. That makes them very easy to use. So, with reference to Figure 3-2, the important thing left to understand is how the drain-source current I_d varies with the gate voltage. Figure 3-3 shows some idealized current-voltage characteristics for the case where the drain-source voltage V_{ds} is varied while the gate-source voltage V_{gs} is held constant at several different values. This is called a common-source configuration because the source terminal is the common reference potential for the gate and drain voltages.

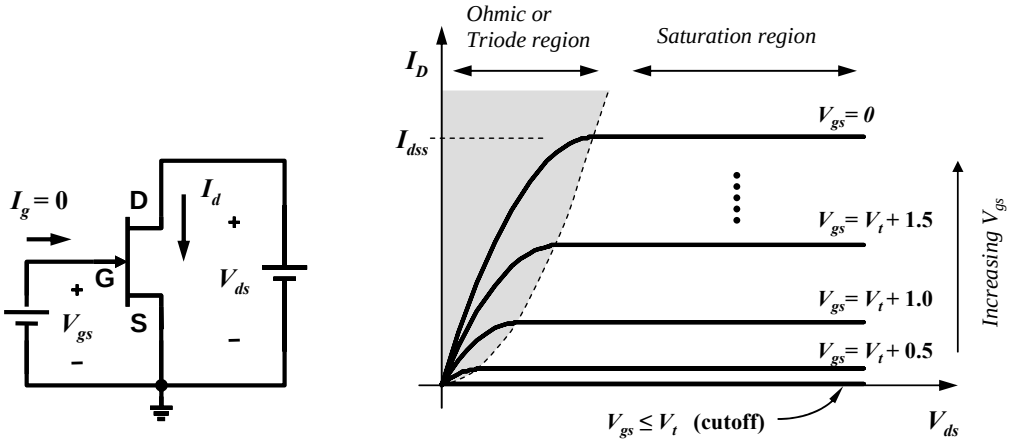

Figure 3-3 – Simple common-source bias configuration and resulting current-voltage characteristics for an n-channel JFET.

The first important feature of the I-V curves is that they all level out at sufficiently high V_{ds}; this is called the "saturation region", because the drain current has reached a saturation point where it can't increase any further (contrast this with a resistor, where the current just keeps increasing linearly with voltage). It's not obvious yet, but we will find that this is the most important region for FET operation in practice.

The second key feature is that there is a critical gate voltage that makes the drain current go to zero; this is called the threshold voltage V_t, also called the "pinch-off" voltage because charges are prevented from entering the channel, much like a plastic tube that has been pinched closed. In n-channel JFETs the pinch-off voltage is *negative*, usually on the order of a few volts. For $V_{gs} < V_t$ the drain current is zero, $I_d = 0$; we could say that the device is in its "off" state. When $V_{gs} > V_t$, the channel conducts and the device is "on". In a simple sense the device acts like a voltage-controlled switch, and many applications use FETs in this way.

In the saturation region, the drain current is a constant that only depends on the gate voltage, so a good model is the voltage-controlled current source as suggested in Figure 3-2. The I_d vs. V_{gs} relationship is given by

$$\text{Saturation:}\quad I_D \approx I_{dss}\left(1-\frac{V_{gs}}{V_t}\right)^2 \quad \text{when}\quad V_{gs} \ge V_t,\ V_{ds} > V_{gs} - V_t \tag{3.1}$$

In a JFET the maximum gate bias than can be applied is typically $V_{gs(\max)} = 0\,\text{V}$, and the drain current at this maximum bias is labeled I_{dss}. So clearly there are two critical parameters of interest for the JFET: I_{dss} and V_t. Once we know those two things, (3.1) allow us to predict the drain current at any other gate voltage. A caution: state-of-the-art short-channel FETs do not always obey (3.1)! Bt that is a topic for 137AB (and beyond…).

For small drain-source voltages the channel current does not reach saturation and instead varies almost linearly with V_{ds}, much as it would in an ordinary resistor, so this region is called the "Ohmic" region. In this case it can be shown that the drain current is given by

$$\text{Ohmic:}\quad I_D = I_{dss}\left[2\left(\frac{V_{gs}}{V_t}-1\right)\frac{V_{ds}}{V_t}-\left(\frac{V_{ds}}{V_t}\right)^2\right] \qquad 0 < V_{ds} \le V_{gs} - V_t \tag{3.2}$$

Note that when V_{ds} is small, this equation reduces to

$$I_D = \underbrace{\frac{2I_{dss}}{V_t}\left(\frac{V_{gs}}{V_t}-1\right)}_{1/R_{ds}} V_{ds} \qquad 0 < V_{ds} \ll V_{gs} - V_t \tag{3.3}$$

This is interesting because it shows that for small V_{ds} the device can be used as a voltage-controlled resistance, potentially useful in some applications. In most cases we will be trying to operate the device in the saturation region, but when used as a switching device, the voltage across the device in the "on" state is often small to minimize power dissipation, and (3.3) tells us that the minimum resistance in this on state occurs for $V_{gs} = 0$ and is given by

$$r_{DS(on)} = \frac{|V_t|}{2I_{dss}} \tag{3.4}$$

This is often a key figure of merit for a switching device.

We mentioned the fact that FETs can be n-channel or p-channel devices. What's the difference? Basically the current flow is in the opposite direction in p-channel devices; it flows from source to drain instead, and the polarity of the gate bias is reversed. Consequently the I-V characteristics are essentially the same as long as we replace V_{gs} by V_{sg}, and V_{ds} by V_{sd}. For a given device size, p-channel devices tend to have smaller I_{dss}, a larger on-state resistance, and poorer high-frequency performance when compared with n-channel devices. So in most cases it is preferable to use n-channel FETs, but we will see that p-channel FETs can be useful in combination with some n-channel devices.

Metal-Oxide-Semiconductor (MOS) Devices

The JFET is an example of a so-called *depletion-mode* device because with no gate bias, the channel normally has an abundance of charge carriers, and a negative applied voltage is required to deplete the channel of charges and pinch-off the device. Remember that we said the device is considered "on" when conducting, and "off" when the drain current is zero. For this reason, depletion-mode FETs like the JFET are called "normally on" devices; if you take away the gate bias they will always be "on" (conducting). In some applications it is desirable to have a normally-off device instead. The need for a negative gate bias also complicates the gate bias circuit, and sometimes makes it necessary to use a bipolar power supply (one with both positive and negative outputs) to power the circuit.

There is a different type of FET that removes these limitations, the enhancement-mode MOSFET. MOS is short for metal-oxide-semiconductor, which simply describes how the device is made; it is similar to a JFET but with an insulating oxide layer sandwiched between

the gate metal and the semiconductor channel. The most important difference from a practical standpoint is that the gate threshold voltage can be made *positive*, so for zero gate bias ($V_{gs} = 0\,\text{V}$) the device is then below threshold and is "off". A positive applied bias $V_{gs} > V_t$ is required to bring charges into the channel and allow current to flow. So enhancement-mode devices are normally "off", and the application of a positive gate bias turns them "on".

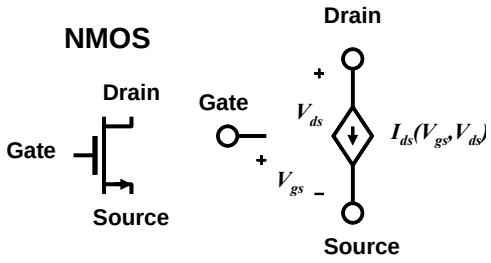

Figure 3-4 – N-channel enhancement-mode MOSFET and equivalent circuit for DC calculations

In most other respects enhancement-mode MOSFETs are similar to JFETs. The symbol and equivalent DC circuit for an n-channel enhancement-mode MOSFET is shown in Figure 3-4; the separation of the gate from the channel in the symbol indicates the presence of the insulating oxide layer that is characteristic of MOS devices. The current-voltage characteristics are shown in Figure 3-5. The only really significant differences are that the threshold voltage is positive, and so I_{dss} (the drain current at zero gate bias) is now a small number associated with a pinched-off channel.

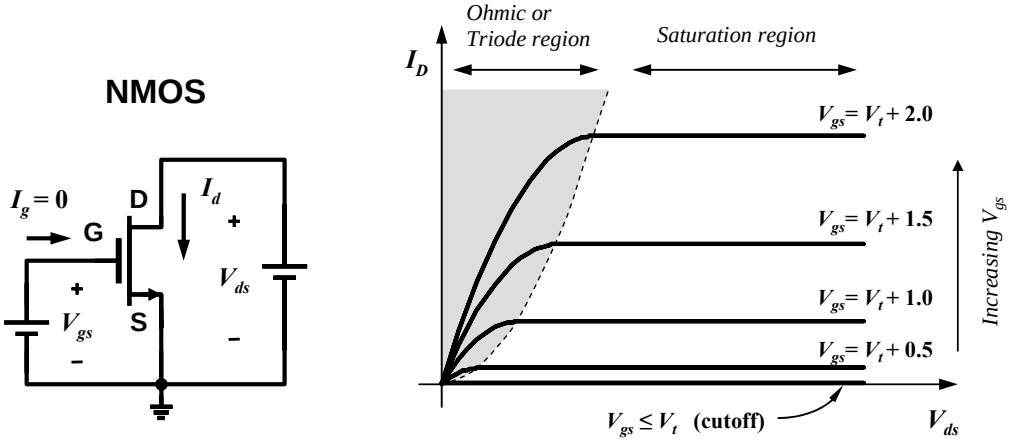

Figure 3-5 – Common-source bias configuration and resulting current-voltage characteristics for an n-channel enhancement-mode MOSFET. The curves are similar to a JFET but the threshold voltage is positive, so all the gate-source voltage in saturation are positive.

The I-V curves for the MOSFET are still reasonably well described by equations of the form (3.1) and (3.2), but it is more common to write them like this

$$I_D = \begin{cases} K_n\left(V_{gs} - V_t\right)^2 & \text{Saturation } (V_{gs} \ge V_t,\ V_{ds} > V_{gs} - V_t) \\ K_n\left[2\left(V_{gs} - V_t\right)V_{ds} - V_{ds}^2\right] & \text{Ohmic } (0 < V_{ds} \le V_{gs} - V_t) \end{cases} \tag{3.5}$$

where K_n is now a technology parameter that has the units of [A/V^2]. We will talk about this parameter and how it relates to the device design in later coursework. The relationship between K_n and I_{dss} is simply

$$I_{dss} = K_n V_t^2 \tag{3.6}$$

As with JFETs, the enhancement-mode MOSFET can be made with both n-type and p-type channels. N-channel MOSFETs are usually abbreviated as NMOS, and p-channel

similarly labeled PMOS. Integrated circuits that employ both types of transistors on the same chip are called CMOS (Complementary MOS) circuits. CMOS technology is by far the most dominant integrated-circuit technology.

It is also possible to create MOS devices that have a negative threshold voltage and hence devices that operate in a depletion mode. These differ from JFETs in that we can apply gate voltages greater than zero volts, so depletion-type MOSFETs are really kind of a hybrid device that combines elements of depletion and enhancement characteristics. So, there are basically six types of FETs that we can group into a family tree as shown in Figure 3-6.

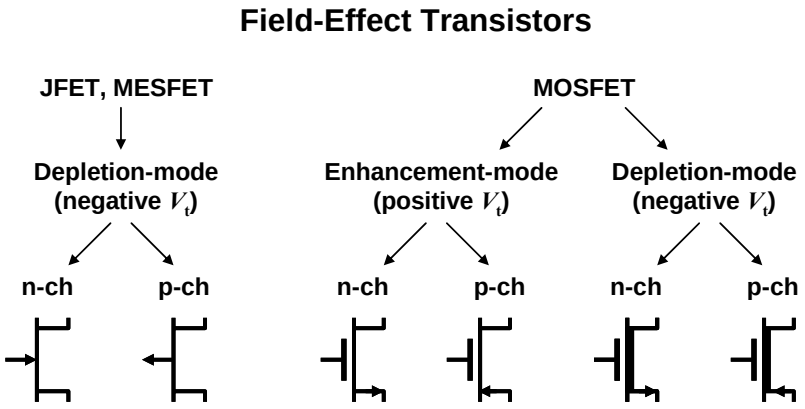

Figure 3-6 – Simple family tree for Field-Effect Transistors.

In this lab we will experiment with an n-channel JFET, an n-channel enhancement-mode MOSFET, and a simple CMOS circuit. In the process we will cover the essential features of many devices in this family tree.

Bipolar Junction Transistors

The BJT (Bipolar Junction Transistor) is both physically and operationally distinct from FETs. Whereas FETs are voltage-controlled devices, BJTS are current-controlled devices. BJTs were in fact the first type of transistor to be widely commercialized, and still play an important role in certain analog circuits and other applications.

Figure 3-7a shows the symbol for an NPN BJT. The primary current path is between the "collector" and "emitter", and this current is modulated or controlled by the current in the "base" terminal. The arrow in the BJT symbol indicates the direction of current flow in a device that is biased in the forward active region.

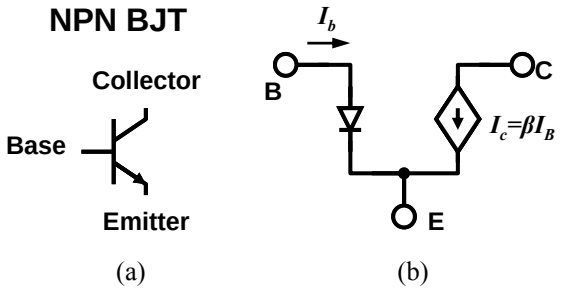

Figure 3-7 – (a) BJT symbol, (b) Simplified equivalent circuit in the forward active region for DC calculations.

Figure 3-7b shows an equivalent circuit for the NPN BJT. The base-emitter junction is modeled by a diode, so immediately we can see that current will only flow if the diode is "on"; that is, if the base is positively biased with respect to the emitter by the diode turn-on voltage (~0.7V for Silicon devices).

When the base-emitter junction is forward biased, the action of the transistor causes a current flow in the collector that is proportional to the base current; the proportionality factor β is appropriately called the current gain of the device.

One nice feature of the BJT is immediately apparent: the relationship between collector current and base (control) current is a simple, linear function. No nasty equations here! Typical I-V characteristics are shown in Figure 3-8. The device is turned "off" when the base-current is zero, and turned on when a base-current is allowed to flow (base-emitter diode is forward biased). Clearly there are qualitative similarities between all the transistors in terms of their I-V curves, but the terminology used in BJTs is a little different. For example, the shaded region in the I-V curve is called "saturation" here, and the region where the collector current is relatively constant is called the *forward active region*. The boundary between the two occurs when $v_{ce,sat} \approx 0.3\,\text{V}$. One feature we are showing in Figure 3-8 is a positive slope on the curves in the forward active region. This is present to some degree in most transistors (FETs too). We typically ignore this effect for DC calculations, but it can be an important effect in some circuits. We will learn how to model such non-idealities later.

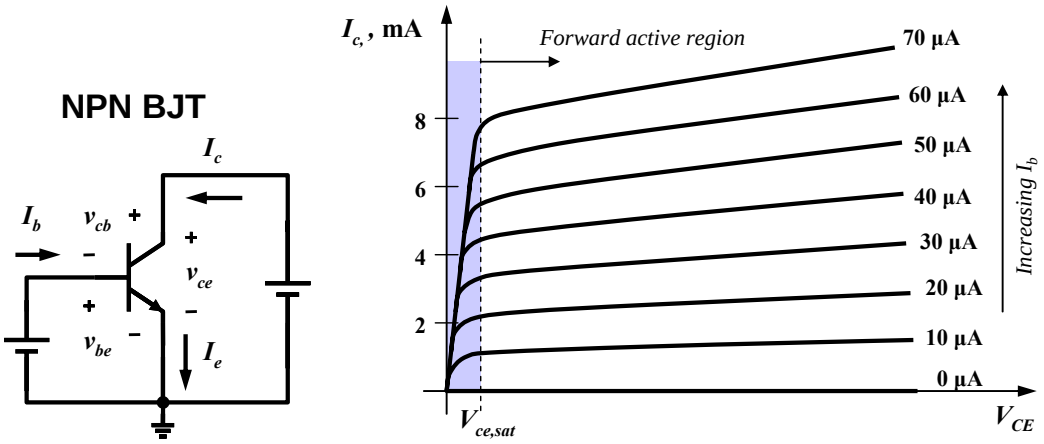

Figure 3-8 – Common-emitter bias configuration and I-V characteristics for the NPN BJT.

Biasing the BJT typically involves choosing the desired collector current and collector-emitter voltage (usually somewhere in the forward active region), determining what base-current is required to achieve this current, and then building a circuit around the device that is consistent with these parameters. With reference to Figure 3-7b, we can see that establishing a desired base current is just a simple diode biasing problem. Once thebase current is established, the collector and emitter currents are given by

$$I_c = \beta I_b \qquad I_e = I_c + I_b = (\beta + 1) I_b \tag{3.7}$$

The ratio of collector current to emitter current is characterized by α_F,

$$\alpha_F = \frac{I_c}{I_e} = \frac{\beta}{\beta + 1} \tag{3.8}$$

In many modern BJTs the current gain β is large enough (100-200) that we can usually take $\alpha_F \approx 1$ and hence $I_e \approx I_c$.

Like FETs, BJTs come in two flavors, NPN and PNP, which are complementary devices in the same sense as n-channel and p-channel FETs.

In-Lab Procedure

3.1 Depletion-mode FETs (JFET)

Measuring I-V characteristics

The JFET we are using in this lab is a 2N5485, an n-channel depletion-mode device. It is a small-signal device that is suitable for controlling currents on the order of <10 mA, at drain voltages <20V.

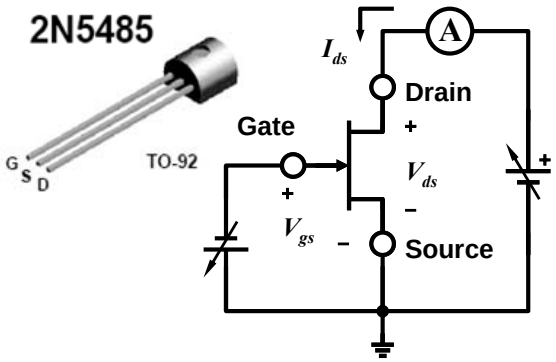

Figure 3-9 – JFET device and circuit for I-V characterization.

□ Find the 2N5485 device in your kit, and construct the simple biasing circuit shown in Figure 3-9. You will use separate power supplies to vary the drain and gate voltages (make sure they are turned down to zero volts before you start, to prevent any damage to the device). In a JFET the gate voltage will be *negative* with respect to the source ($V_{gs} < 0$), so be sure to hook up the gate-source supply correctly! Use your bench DMM to monitor the drain-source current; your hand-held DMM will be helpful later for monitoring some of the voltages.

□ Set $V_{gs} = 0$ and then increase the drain voltage to $V_{ds} = 10\,\text{V}$. The current eventually saturates to a nearly constant value, I_{dss}. This is the maximum current that can flow in the device under normal conditions. Record I_{dss} for your device.

□ Now, with $V_{ds} = 10\,\text{V}$, slowly decrease the gate-source voltage V_{gs} (that is, make it more negative, which means increasing the supply voltage if you hooked up the circuit correctly!). You should see the drain-source current start to decrease. Find the gate-source voltage that reduces the output current to nearly zero (say, <0.01mA); this is approximately the *pinch-off* voltage, or *threshold* voltage for the device, V_t (Note that different people label this in different ways; the data sheet calls it $V_{gs(off)}$).

Note: In the manufacture of FETs it is difficult to precisely control the threshold voltage and I_{dss}, so you will find that the data sheet just specifies upper and lower bounds for the device. In your lab writeup, compare your measurements with the values in the data sheet.

□ Now, lets measure the I-V curves. We "could" use a curve tracer, but that would be too easy! Fortunately we do not need many points to make a nice plot; the table below can serve as a guide. Record I_{ds} vs. V_{ds} in the range $0 < V_{ds} < 15\,\text{V}$ for four different values of V_{gs}, starting at $V_{gs} = 0$. Try to pick a range of gate-source voltages so that the last data set is near pinch-off; I've suggested increments of 0.5V since most 2N5485s pinch off around -2V, but you may need to choose differently depending on your device.

	I_{ds} [mA] (record for each gate voltage below)				
V_{ds} [V]	V_{gs}=0 V	V_{gs} = -0.5V	V_{gs} = -1.0V	V_{gs} = -1.5V	
0					
0.5					
1					
2					
5					
10					
15					

Looking at the data above, you should clearly see the general features that we expect for FETs: at the higher drain-source voltages (V_{ds}>5V) the current is nearly constant and depends only on V_{gs}. It is this ability to control the current using a separate signal on the gate that makes FETs so useful.

In your lab report, generate a set of I-V curves from your data. Compare the I_d-vs-V_{gs} data against the theoretical square-law relation. Do not do this during the lab period!

JFET Biasing Circuit

When we say "transistor bias", what we mean is configuring the circuit so that the transistor operates with a specified DC output current and voltage. Usually the electronic system will have some specified power-supply voltage (*e.g.* ±12 V), and it is our job to design the circuit to set the correct current and voltage levels on the transistor using the available voltages.

Consider the simple JFET circuit shown in Figure 3-10, powered from a 12V supply. To bias the transistor correctly in this case, we need to establish the correct gate voltage (which governs the drain current that can flow in saturation) and then we must choose the drain resistor to set the desired output voltage.

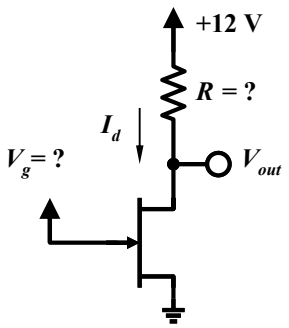

Figure 3-10 – A simple JFET biasing challenge

- □ Using the I-V data you took earlier, determine what gate voltage and resistor value is needed to make $V_{out} = +7\,\text{V}$ and $I_d = 5\,\text{mA}$ using a 2N5485 in the circuit of Figure 3-10.
- □ Now build the circuit and measure the output voltage (choose the nearest stock resistor value for your design). Use the bench supply for the gate bias. How close did you come? In such situations engineers will usually declare victory if they are within ±10% of the design goal! There are ***always*** uncertainties in device parameters and resistor values that make higher levels of precision a difficult challenge.

Note that if the gate voltage were suddenly disconnected for some reason, then the maximum drain current will flow. For this reason we say that depletion-mode devices are "normally on" devices; we have to apply a negative bias to shut them "off".

The negative gate bias that is required for depletion-mode devices is a slight annoyance, but there is a simple trick that we can use to "self-bias" the gate: this is shown in Figure 3-11. Can you see how this works? Since the gate is grounded, the voltage drop across the source resistance R_s puts the source at a higher potential than the gate, thus making V_{gs} negative.

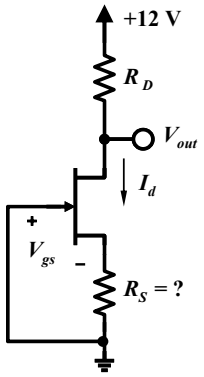

Figure 3-11 – Self-biasing JFET circuit.

□ Choose the source resistance R_s to establish the bias conditions that you had in the previous step. Choose the nearest stock resistor value and build the circuit. How close did you come this time?

JFETs have been largely displaced by MOS technology, but they share many common features with depletion-mode MOSFETs. There are also other depletion-mode devices (Gallium-Arsenide-based MESFETs and HEMTs) with characteristics somewhat similar to JFETs that are widely used in high-frequency applications such as radar and satellite communications. So a study of JFETs is worthwhile.

3.2 Enhancement-mode MOSFETs

Most transistor electronics today are based on a different type of device, the enhancement-mode MOSFET. Enhancement devices have some attractive features that make them more desirable and/or easier to use than JFETs and other depletion-mode devices. Two important advantages are: 1) they have a positive gate threshold voltage (i.e. they do not require negative gate bias); and consequently 2) they "normally off" devices.

Gate-Drain I_D-V_{gs} Characteristics

The MOSFET we are using in this lab is a 2N7000, an n-channel enhancement-mode device. It is a small-signal device that is suitable for controlling DC currents on the order of <200 mA, at drain voltages <60V. Since we already know what to expect for the I-V characteristics (the data-sheet also includes some representative curves), lets just measure the I_d-V_{gs} curve to find the important design parameters:

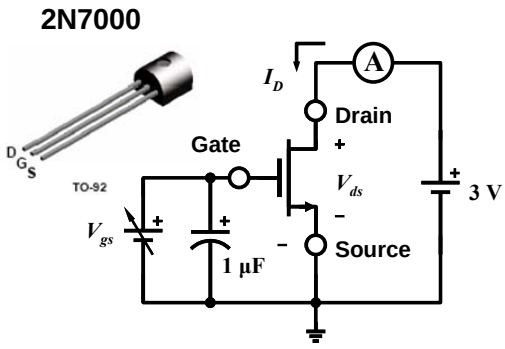

Figure 3-12 – N-channel enhancement MOSFET device and common-source circuit for Id-Vgs characterization.

□ Find the 2N7000 device in your kit, and construct the simple biasing circuit shown in Figure 3-12. **Note the pin assignments have changed!** Here the gate voltage will be *positive* with respect to the source ($V_{gs} > 0$). Note also the addition of a 1uF capacitor on the gate (needed for stability reasons).

□ Set $V_{gs} = 0$ and then increase the drain voltage to $V_{ds} = 3\,\text{V}$. The device should be off (no current flowing). Now increase V_{gs} slowly until the current reaches about 100mA (this should typically happen around 3V). We don't want to exceed this current level, in order

- □ to keep the power dissipation in the device within its specified range (<400mW max). Record the gate voltage and drain current.
- □ Now decrease the gate voltage in increments of 0.1V, and record the drain current at each voltage.
- □ Using your data, estimate the parameters K_n and V_t. Compare your threshold voltage against the data-sheet typical value of 2.1V.

V_{gs} [V]	I_D [mA]

In your lab report, plot the I_d-vs-V_{gs} data, and compare against the theoretical square-law relation in (3.5) to more accurately determine the parameters K_n and V_t. How well does this device obey the theoretical model? There is in fact a good reason why the model should *not* work well for small currents, but we'll save that topic for ECE 2C and ECE132!

Four-Resistor Bias Circuit

From your data you will notice that small changes in gate voltage lead to rather large changes in current with this device. This is generally a desirable property for reasons we will see shortly, but it has a drawback: it means that in order to set the DC drain current accurately, we must be fairly precise in how we set the gate voltage. Compounding this problem is the fact that the threshold voltage varies between devices.

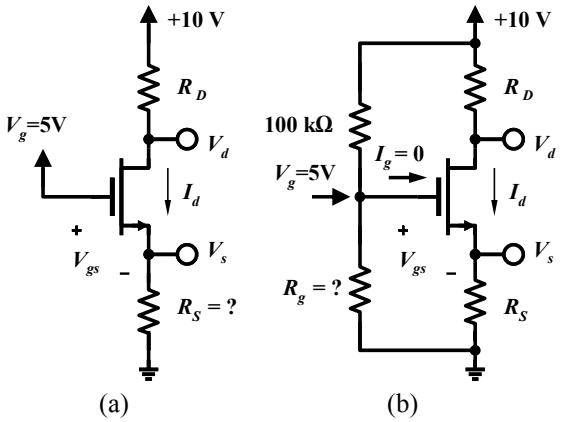

Figure 3-13 – Biasing circuit for MOSFET

Adding a source resistance is a partial solution to these problems. Figure 3-13a shows a simple bias scheme for a MOSFET, assuming a constant voltage is applied at the gate. If the drain current I_d is specified, then the gate voltage would be

$$V_{gs} = 5\,\text{V} - I_d R_s \tag{3.9}$$

We then choose R_s to give us the correct gate voltage, *i.e.* the V_{gs} that is appropriate to that drain current, which we can get from our measured data or the theoretical model.

To see why this is a good solution for biasing, consider what happens if the resistor is too small: then V_{gs} would increase, causing the drain current to increase, but then this would increase the voltage drop across R_s, causing V_{gs} to decrease. The source resistance thus has a stabilizing effect on the drain current, minimizing errors due to component tolerances and threshold voltage variations.

- □ Build the circuit in Figure 3-13a using your 2N7000. Choose a source resistance R_s so that $I_d \approx 20\,\text{mA}$, and then choose a drain resistance R_D so that $V_d \approx 8\,\text{V}$. Measure V_d and V_s. How close were you able to come to the design goal?

□ Since the FET draws negligible current at the gate terminal, we can make a simple voltage divider to derive the +5V gate bias from the +10V supply, as shown in Figure 3-13b. Do this for your design from the previous step, choosing the gate resistance R_g appropriately, and re-measure V_d and V_s.

The circuit you just made is one of the most common biasing networks for MOSFET amplifiers, often simply called a *four-resistor bias network*. A similar scheme works for BJTs too. This network gives us a lot of flexibility in choosing the bias conditions, and has the advantage of requiring only a single supply voltage.

Incidentally, you may wonder why a 100kΩ resistor was chosen for the voltage divider on the gate. Why not 1kΩ, for example? One reason is simply to minimize the current draw from the power supply; if this circuit were powered from a battery, any current through this resistor divider is really wasted current, and would reduce the battery life. In later coursework we will learn other considerations that impact the choice of this resistance.

Simple LED Blinker

In the bias circuit you just made, you chose resistors to set a current level of around 20mA, with a voltage drop of around 2V across the drain resistor. Those are also the terminal conditions that describe the on-state of a red LED, so we can swap out R_d and replace it with a red LED without changing the operation of the circuit.

Now, if we ground the gate terminal the device would then be off, and no current would flow in the LED. Thus we should be able to turn the LED on and off by varying the gate voltage between zero and 5V.

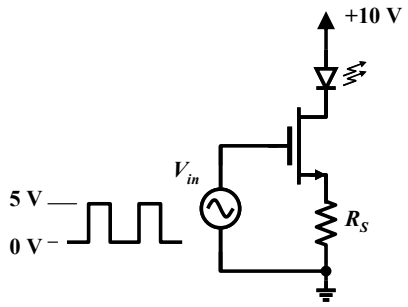

Figure 3-14 – Simple LED Blinker

□ Build the circuit in Figure 3-14 using your source-resistance from the previous step. Use the function generator to apply a 0-5V square wave to the gate terminal of the device. Adjust the frequency to a low enough value (on the order of 1 Hz) so that you can see the LED turn on and off. At what frequency can you no longer discern the flickering of the light? This question is relevant to our future discussion of LED displays.

This is our first example of using the transistor as a kind of electronic "switch" to turn something on or off. Note that the function generator is basically supplying no current (and hence no power) to the circuit; all the current for the LED comes from the +10V supply. This ability to control a large current with a separate and smaller signal is a central concept in the application of transistors.

More on Switching

Now, if we really wanted to operate the FET as a more ideal switch, we would try to make the device look like an open-circuit in the off state, and a short-circuit in the on-state. How can we do this?

The off-state is easy, just bias the gate below pinch-off so that no current flows. In fact we already did this in the LED blinker. To make it look like a short-circuit in the on-state we must configure the circuit so that the output voltage is very small when the device is

conducting; that is, we need to make the on-state resistance small in comparison to all the other resistances in the circuit.

Consider the circuit shown in Figure 3-15. When the input voltage is 0V, the device is off and no current flows through R_d. This means that the output voltage is just $V_{out} = 10\,\text{V}$. When the input voltage is +5V, however, then a very large drain current can flow. In this case, the drain current will then be limited by the drain resistor. That is, we can make $V_{out} \approx 0$ by simply choosing $R_d \geq 10 / I_d$; a large drain resistor effectively makes the device look like a short-circuit in comparison, and it consequently determines the amount of current that will flow when the transistor is "on". So here it is not important to control the gate voltage accurately. We just choose gate bias points that are well above and well below the threshold, and let the resistor do the work of setting the current!

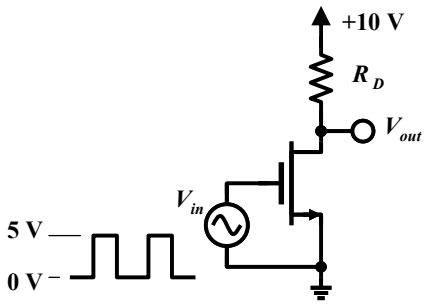

Figure 3-15 – A simple switching circuit (inverter).

□ Build the circuit in Figure 3-15 with a drain resistance of $R_d = 10\,\text{k}\Omega$. Set the function generator to create a 5V square wave at a frequency of 1 kHz. Configure the oscilloscope to monitor V_{in} on CH1, and V_{out} on CH2. Record your observations.

If you did this correctly, you will note the following:

- The device is indeed operating as a nearly ideal switch
- The circuit acts like an inverter: when the input is high, the output is low, and vice versa. You may recall from lab 1 that this inverting operation was impossible with diode logic, but it is easy with transistors.
- The circuit has effectively *amplified* the input signal by a factor of two. That is, the output waveform is like the input waveform but with twice the voltage!

As simple as this circuit is, it captures many of the essential aspects of more complicated transistor circuits that we will be learning about in subsequent labs and coursework. Please pay close attention to *why* the output waveform appears amplified: the choice of drain resistor accomplishes this trick. When the drain resistor is large enough so that the voltage drop across it is greater than the input voltage, then we will have a voltage "gain". As a simple thought experiment, what would the output voltage become if the supply voltage were reduced to +5V?

3.3 CMOS Circuits

The simple inverter circuit in Figure 3-15 has a problem: it doesn't work as well for some loads! So see why, consider Figure 3-16a. In the on-state when the FET acts like a short there is no problem: the output voltage will always be close to zero volts as long as R_d is reasonably large. But in the off-state the FET acts like an open circuit, so the load resistance R_L and drain resistance make a voltage divider. The output voltage in the off state then depends critically on the load resistance, an undesirable situation. We'd like the circuit to behave the same way no matter what it is hooked up to (within reason of course; few circuits work well when driving a short).

This is where p-channel devices and CMOS comes in, and shown in Figure 3-15b. The idea is to replace the drain resistor by a p-channel FET that switches in the opposite way as the n-channel device. When the input is high, the NMOS device is a short and the PMOS device is open, so the load is effectively shorted to ground. When the input is low the NMOS device is off and the PMOS device is ON, so the load is connected to the supply voltage.

This is a nearly ideal inverter circuit from an applications standpoint. It takes very little current to drive it, and can source or sink relatively large load currents while maintaining the output voltage limits close to 0 and V_{DD}. Unlike the resistor-based inverter, the CMOS version dissipates very little power because whenever a device is on, the voltage across it is small, so the current-voltage product is always small.

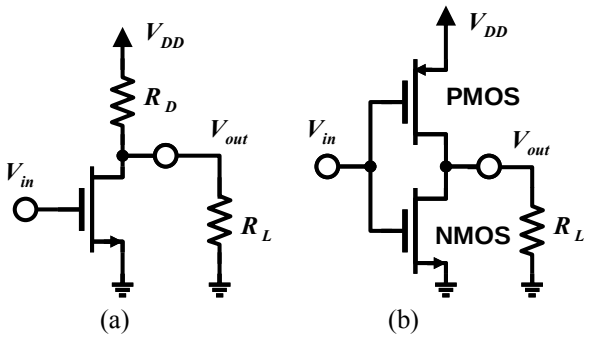

Figure 3-16 – Simple inverter with load, and (b) improved CMOS version

An additional advantage is that transistors occupy *much* smaller areas on an integrated circuit than a resistor, so we can fit lots more CMOS inverters on an integrated circuit than resistor-based inverters. The inverter is a fundamental building block of many logic functions, so you can start to appreciate why CMOS ICs are the logic family of choice for digital electronics.

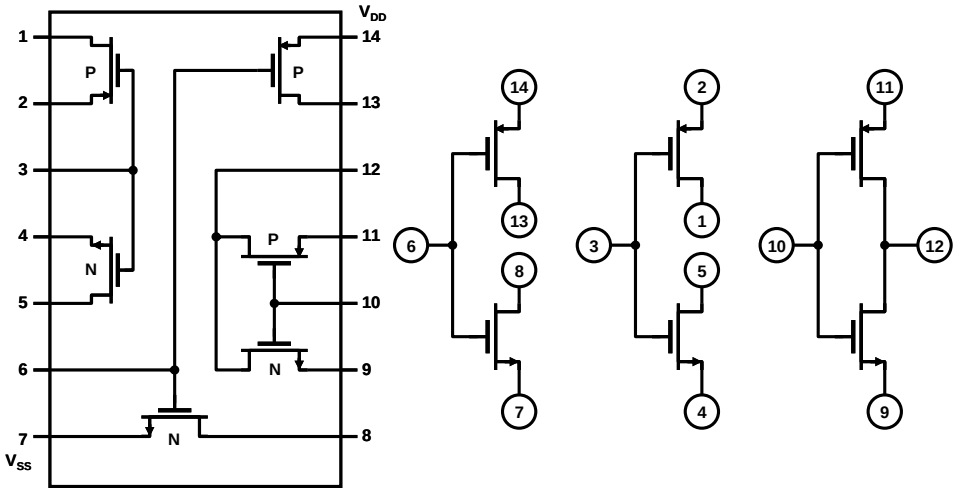

Figure 3-17 – Pinout for the CD4007 CMOS pair/inverter chip. **Note: Pins 7 and 14 must be hooked up to the supply rails for proper operation of the devices**.

In this lab we have provided a very simple CMOS integrated circuit that includes both PMOS and NMOS devices, the CD4007 shown in Figure 3-17.

□ Build the circuit in Figure 3-16b using one of the inverter pairs on the CD4007 (the 9-10-11-12 pair is obviously the easiest one here). Use a supply voltage of +5V and a load resistance of $R_L = 1\text{k}\Omega$. Remember to connect pin 14 to +5V and pin 7 to ground. Set the function generator to create a 0-5V square wave at a frequency of 1 kHz and use this

to drive the inverter. Monitor the input and output waveforms on the oscilloscope and record your observations.

Note: In CMOS IC's the transistors have a "body" or "substrate" terminal that is internally connected to one of the power-supply pins, thus it is important to hook up the V_{DD} and V_{SS} pins to their respective supply rails, even if the diagram does not show an explicit connection.

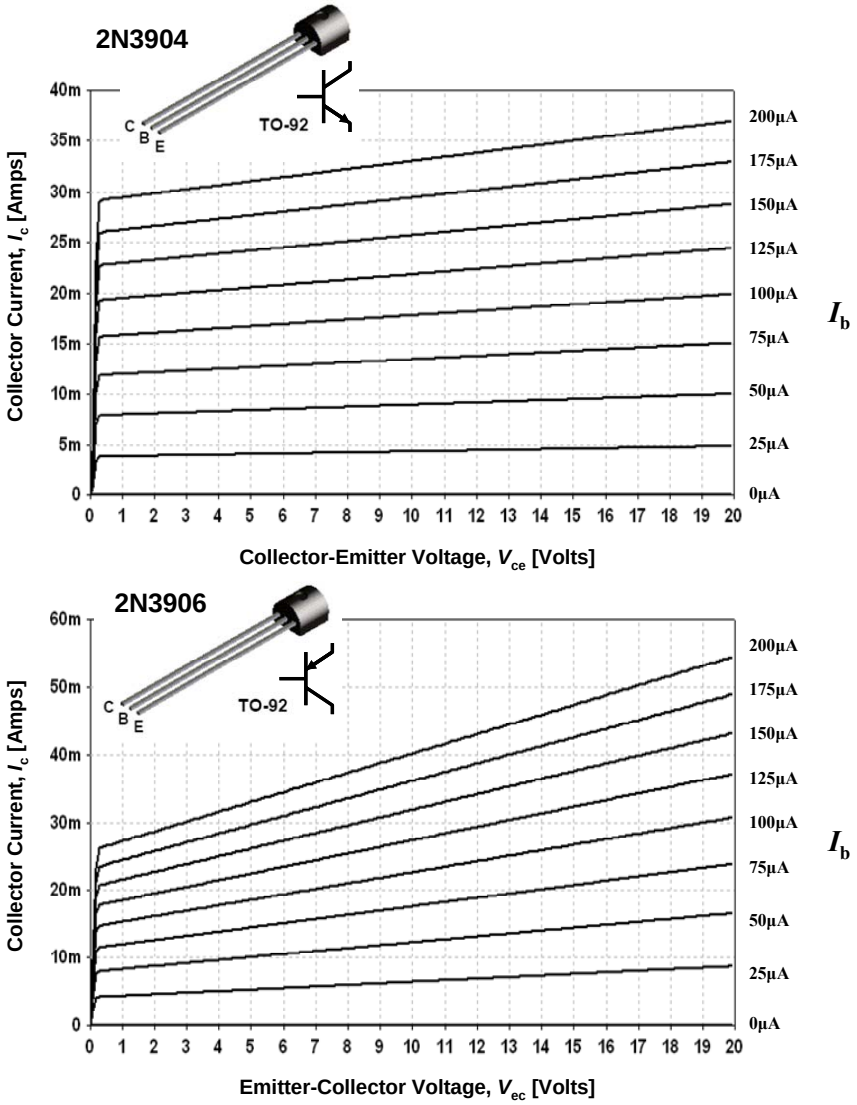

Figure 3-18 – Representative I-V curves for the 2N3904 and 2N3906.

3.4 Bipolar Junction Transistors (BJTs)

Biasing BJTs is a little different than FETs because it is a current-controlled device, but otherwise, most of the circuit techniques we have discussed above for FETs translate

reasonably well to BJT circuits. So let's just make a couple of simple BJT circuits here to demystify them a bit.

We will use the 2N3904 (NPN) and the 2N3906 (PNP), two of the most commonly-used discrete BJTs, suitable for a variety of low-level amplification and switching functions. Representative I-V curves for these devices are shown in Figure 3-18. From these curves we can see that the current gain is on the order of $\beta \approx 200$ for both devices (the data sheets specify a minimum of 100 and maximum of 300).

Like the FETs, the variation of device parameters with temperature, manufacturer, etc. make the four-resistor bias network a better choice than some simpler techniques. But for simple switching functions, simple bias networks are often used. Consider the circuit in Figure 3-19. The resistor R_b determines the base current according to

$$R_b = \frac{5\,\text{V} - 0.7\,\text{V}}{I_b} \tag{3.10}$$

□ For the circuit shown in Figure 3-19, the design goal is $I_c = 20$ mA and $V_{out} = 6\,\text{V}$. Find the base-resistance and collector resistance to make this happen (assume $\beta = 200$). Then build the circuit and verify. How close did you come?

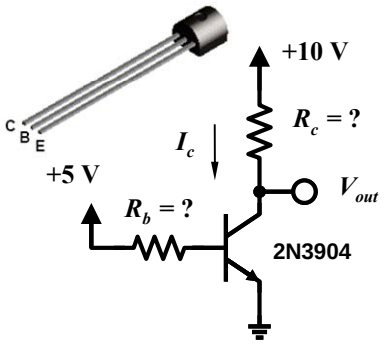

Figure 3-19 – Simple BJT circuit.

Hopefully you will find that working with BJTs isn't too different from working with FETs. Although MOSFETs are more common these days, it is important to become comfortable designing circuits with any kind of transistor.

Let's finish with a simple circuit that highlights the difference between NPN and PNP BJTs. In the PNP, all the polarities are reversed: the emitter is biased higher than the base to turn the device on, and current flows from emitter to collector. Otherwise, the behavior is similar. Consider the simple circuit shown in Figure 3-20, what does this do? Build it and find out!

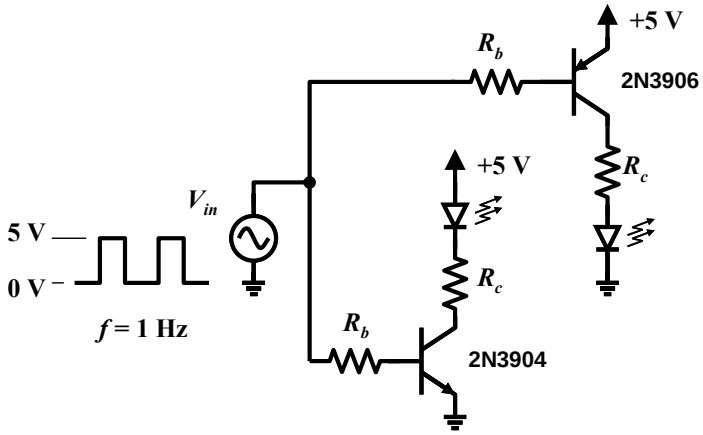

Figure 3-20 – Circuit using NPN and PNP devices.

Congratulations!
You have now completed Lab 3