4

Transistor Switching Circuits

This lab continues our exploration of basic transistor switching circuits. We will examine some considerations for driving capacitive and inductive loads, and put this to use in creating a simple DC fan driver and DC-DC Boost converter. In the process we will tie in a lot of what you learned about 1st and 2nd-order circuit responses.

Pre-lab Preparation

Before Coming to the Lab

- □ Read through the lab experiment to familiarize yourself with the components and assembly sequence.
- □ Calculate the drain resistor that achieves critical damping on the leading edge (on-off transition) for the circuit in Figure 4-7
- □ Each group should obtain a parts kit from the ECE Shop.

Parts List

The ECE2 lab is stocked with resistors so do not be alarmed if you kits does not include the resistors listed below. Some of these parts may also have been provided in an earlier kit.

Laboratory #4	
Transistor Switching Circuits	
Qty	**Description**
2	2N7000 NMOS
1	2N3904 NPN BJT
1	2N3906 PNP BJT
1	CD4007 CMOS pair/inverter
2	1N4005 diode rectifier
1	12V DC brushless fan, 1.6 in. (40mm), 100mA
1	2in strip of double-sided foam tape
4	0.1uF capacitor (CKO5 low-volt. Ceramic)
1	10uF capacitor (electrolytic, 25V, radial)
1	100uH toroidal inductor (vertical)
2	10-Ohm 1/4 Watt resistor
1	22-Ohm 1/4 Watt resistor
1	100-Ohm 1/4 Watt resistor
1	470-Ohm 1/4 Watt resistor
1	1-KOhm 1/4 Watt resistor
1	3.3-KOhm 1/4 Watt resistor
3	10-KOhm 1/4 Watt resistor
2	100-KOhm 1/4 Watt resistor

Background information

Suggested background reading:

- Sedra & Smith: Sections 4.2-4.5, 5.2-5.5 (excellent stuff on MOS and BJTs, although somewhat more rigorous in detail than we need here).
- Posted material on DC-DC boost converters

Constant-Current Charging of Capacitors

In our study of 1st-order RC circuits the capacitors were always charged/discharged through a resistor as in the circuit of Figure 4-1a. If the battery voltage V_{DD} is applied at $t = 0$, the capacitor voltage is given by the familiar *exponential* dependence

$$V_{out}(t) = V_{DD}\left(1 - e^{-t/RC}\right) \tag{4.1}$$

Initially (for small *t*) the capacitor voltage increases linearly, but then the charging rate slows and the capacitor voltage approaches its final steady-state value asymptotically. This is because the charge transfer to the capacitor is limited by the resistor; as the capacitor voltage increases, the voltage drop across the resistor decreases and hence the current also decreases.

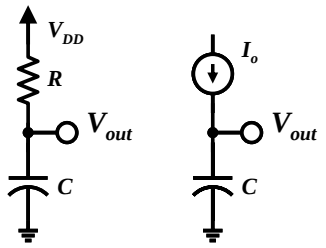

Figure 4-1 – (a) Capacitor charged by a resistor. (b) Capacitor charged by a constant current source

What would happen if the capacitor were charged by a *constant* current source, as in Figure 4-1b? Starting with the I-V relationship for a capacitor we can show in this case that the output voltage rises *linearly* with time,

$$I_0 = C\frac{dV_{out}}{dt} \quad \Rightarrow \quad V_{out}(t) = \frac{I_0}{C}t \tag{4.2}$$

Under certain conditions transistors behave like constant current sources, so it is possible to generate linearly increasing voltage over short time periods using transistors to charge and discharge a capacitor. This technique is the basis for generating triangular and sawtooth waveforms in some function generators. Of course an ideal current source would keep pumping the same current forever and the voltage would eventually become enormous, whereas a transistor-based current source will simply stop functioning when the voltages become too large. So it is understood that the equivalent circuit in Figure 4-1b is only a crude model for a transistor-based charging circuit under the appropriate bias conditions.

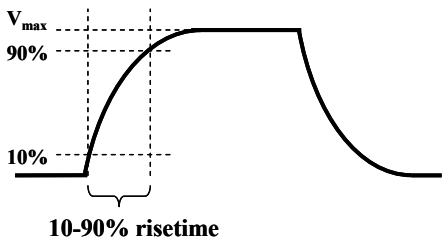

Figure 4-2 – Definition of 10-90% risetime.

Measuring Rise-Time in Switching Waveforms

In digital electronics or other applications involving signals that switch between two states, a good practical measure of the switching transient is the 10-90% rise-time or fall-time. This is the time is takes for the signal to transition between 10% and 90% of its total swing, as illustrated in Figure 4-2.

If the waveform is exponential as in (4.1) then there is a very simple relationship between the 10-90% risetime and the time-constant in the circuit. The time it takes to reach 10% and 90% of the final value is found using (4.1) as

$$\begin{aligned} 0.1 &= 1 - e^{-t_{10\%}/RC} \quad \Rightarrow \quad t_{10\%} = -RC\ln(0.9) \\ 0.9 &= 1 - e^{-t_{90\%}/RC} \quad \Rightarrow \quad t_{90\%} = -RC\ln(0.1) \end{aligned} \tag{4.3}$$

so the 10-90% risetime is given by

$$T_{10-90\%} = t_{90\%} - t_{10\%} = RC\ln\left(\frac{0.9}{0.1}\right) \approx 2.2RC \tag{4.4}$$

with a similar result for the fall-time. Clearly we can measure a 10-90% waveform for any monotonically varying transition, not just exponential transitions. The relationship (4.4) is a good one to commit to memory; better yet, try to remember how it is derived!

Switching Response of RLC Load

In transistor switching circuits we can often gain insight into the behavior of the circuit by modeling the transistor as a nearly ideal switch, so that the Laplace transform methods can be applied. Figure 4-3a shows an example of a MOS inverter stage driving an LC load.

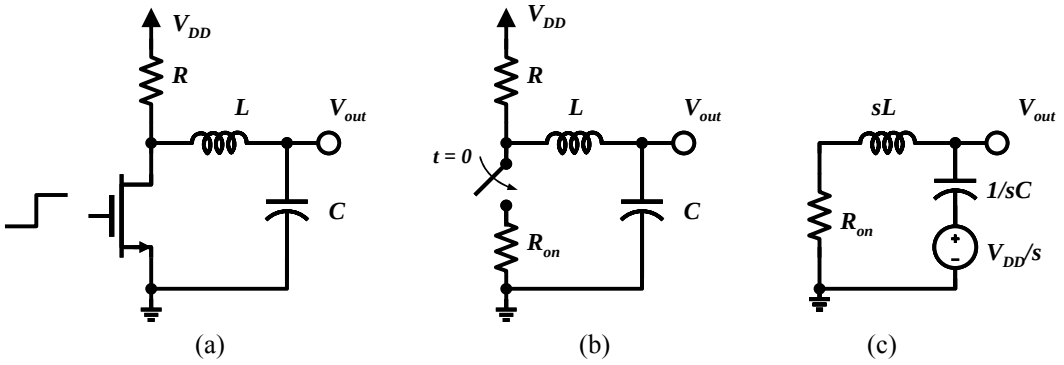

Figure 4-3 – (a) Inverter driving an LC load. (b) Equivalent circuit for off-on transition. (c) s-domain equivalent circuit.

In the off-state the transistor is effectively an open-circuit, and in the on-state it can be modeled by a small resistance, R_{on}, so we can replace the transistor by the simple switch circuit shown in Figure 4-3b. From this point it is a standard linear circuit problem that we can solve using Laplace techniques. Lets consider the high-to-low transition where the transistor turns "on" from an initially "off" state, corresponding to the switch being closed at $t = 0$. The initial condition in this case will be a constant voltage of V_{DD} across the capacitor, no initial current in the inductor, and the s-domain equivalent circuit is shown in Figure 4-3c. Solving for $V_{out}(s)$ we get

$$V_{out}(s) = V_{DD}\frac{s + R_{on}/L}{s^2 + sR_{on}/L + 1/LC} \tag{4.5}$$

a classic second-order response. The roots of the denominator are at

$$s = -\frac{R_{on}}{2L} \pm \sqrt{\left(\frac{R_{on}}{2L}\right)^2 - \frac{1}{LC}} \tag{4.6}$$

from which we can determine the following conditions for over-damping, under-damping, and critical damping:

$$R_{crit} = 2\sqrt{\frac{L}{C}} \qquad \begin{array}{l} \text{over-damped: } R_{on} > R_{crit} \\ \text{critically-damped: } R_{on} = R_{crit} \\ \text{under-damped: } R_{on} < R_{crit} \end{array} \tag{4.7}$$

Recall that for a MOSFET the on-resistance is given by

$$R_{ds(on)} \approx \frac{1}{2K_n(V_{gs} - V_t)} \tag{4.8}$$

So the on-resistance can be controlled by the gate-source voltage. Thus we see that for the circuit in Figure 4-3a with an LC load, the on-state resistance of the device will determine the shape of the response for a given inductance and capacitor. Or alternatively, the characteristic impedance $\sqrt{L/C}$ of the load will determine the response for a given device and bias point.

Note that we just consider the off-to-on transition in the circuit above. If the switch was initially closed and then opened at $t = 0$, we would have a slightly different equivalent circuit. The form of the response will be similar to (4.5), but with R_{on} replaced by the drain resistance R. So the transient response associated with the on-to-off transition will be controlled by the drain resistance. It would be helpful for you to convince yourself of this before coming to lab.

In-Lab Procedure

4.1 Driving Capacitive Loads

BJT Inverter

We've already discussed the simple BJT inverter circuit shown in Figure 4-4. Here we've chosen a bias resistor in the base to give $I_b \approx 50\,\mu\text{A}$ with a 5V input signal, so with $\beta \approx 200$ the transistor will pull more than enough current to drive the output low with the 1kΩ collector resistor shown. Now let's add some capacitance across the output node and see what happens:

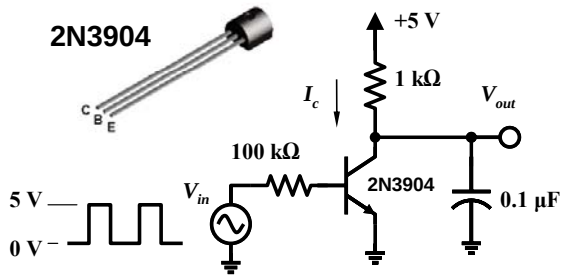

Figure 4-4 – BJT inverter driving a capacitive load.

- □ Build the circuit in Figure 4-4, and adjust the function generator to produce a 0-5V square wave. Start with 100Hz, and record the output waveform.
- □ Now increase the frequency to 1kHz and observe the waveforms again. You should now see significant deterioration of the leading and falling edges of the waveform. Estimate the 10%-90% rise- and fall-times on the leading and trailing edges of the output waveform.

How can we improve the circuit to allow it to operate at higher frequencies with a capacitive load? Clearly the capacitor has introduced a charging/discharging time constant in the circuit, so we need to find a way to charge and discharge the capacitor more quickly.

Let's start with the falling edge of the output waveform: in this case the transistor is switching "on", and the capacitor discharges through the transistor. We can speed up this part of the waveform by increasing the on-state collector current in the transistor. This way the transistor pulls charge off the capacitor at a faster rate:

- □ Change 100kΩ base resistor to 10kΩ and repeat the last step. You should see an improvement in the falling edge of the output waveform. Record your observations; can you quantify the time constant on the falling edge now?

Do you understand why this last step works? An equivalent way to think about this problem is to consider the on-state resistance of the transistor, which forms a simple RC circuit with the load capacitor. The on-state resistance of a BJT is approximately $R_{on} \approx 0.3\,\text{V}/I_c$, so increasing the collector current decreases the resistance.

Now, how can we improve the charging time associated with the leading edge of the waveform? In this case the transistor is turning off, so the capacitor must charge through the collector resistor, forming a different RC time constant (verify that your rise time is consistent with the circuit values). We "could" improve the rise-time by decreasing the value of the collector resistor, but that approach has a problem: if the collector resistor too small, then the output voltage will not go to zero when the transistor is "on".

Ideally we would like to have a collector resistance that is small when the transistor is "off", and large when the transistor is "on". Figure 4-5 shows how we can do this: simply replace the collector resistor by a complementary transistor! Now when the input signal is low, the lower transistor (2N3904) turns off and the upper transistor (2N3906) turns on, so the capacitor is now charged through a low-resistance path. When the input signal is high, the upper transistor turns off, and the lower transistor turns on, discharging the capacitor through a low-resistance path.

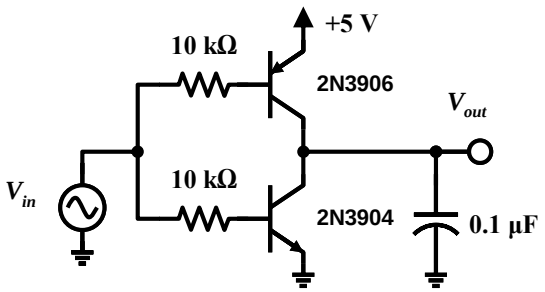

Figure 4-5 – Improved BJT inverter using complementary devices.

- □ Build the circuit in Figure 4-5 and record the output waveforms for 1 kHz input signal. You should see a significant improvement in the rise and fall times.
- □ Increase the frequency to 10kHz. The inverter should still perform reasonably well, but the rise and fall times will be more easily observable. Note that the leading and falling edges are very linear, evidence of constant-current charging of the load capacitor as described in the Background section. Record your observations.
- □ Lastly, increase the input frequency to >100kHz and record your observations. Clearly the output no longer resembles the input signal, but there are occasional uses for such triangular waveforms.

CMOS Inverter (Optional, for Extra Credit)

The complementary BJT inverter shown in Figure 4-5 is obviously similar to the CMOS inverter you built in the previous lab using the CD4007 IC. How do the two compare in terms of switching speed?

- □ Build the CMOS inverter using the CD4007 from Lab #3, and attach a capacitive load as shown. At an input frequency of 1kHz, how does this circuit compare with the BJT inverter you just built?

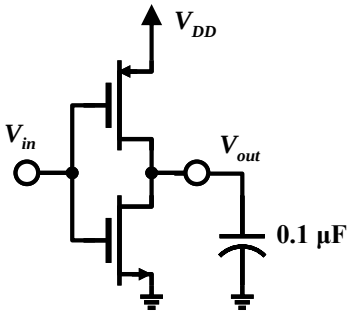

Figure 4-6 – CMOS inverter with capacitive load

You will see that this circuit does not perform well, even at 1kHz. This isn't a condemnation of CMOS circuits, it simply reflects the fact that the CD4007 was designed using transistors that can not drive as much current, and therefore cannot charge and discharge capacitive loads very quickly. A conclusion to draw from this exercise is that you *always* need to consider the kind of load on your circuit. The constraints imposed by the load will often limit the performance.

4.2 Inductive Loads

Ringing Response

The fun really begins when the transistor is attached to an inductive load. Let's start by considering a simple LC network as shown in Figure 4-7. Here we will use the 2N7000 for reasons that will become clear later.

The simple voltage divider network on the gate reduces the 5V square wave to a lower peak value, but the components values shown will still overdrive the gate so that the device has a low on-state resistance. The output current in the on-state will then be limited by the drain resistor.

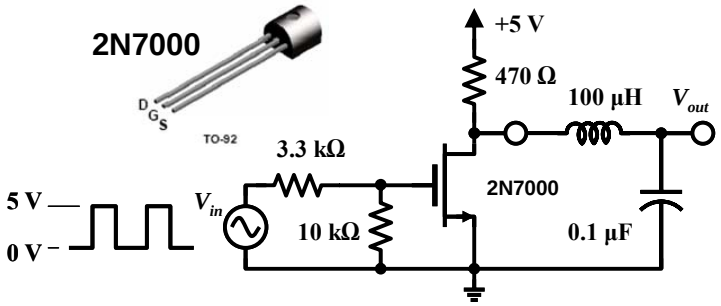

Figure 4-7 – MOS inverter driving an LC load.

□ Build the circuit in Figure 4-7 with the component values shown, and use an input frequency of 2kHz. Record your output waveforms.

Unless your 2N7000 has an unusually high threshold voltage, you should see evidence of ringing on the trailing edge of the output waveform. Why? Well, in this case the circuit is doing EXACTLY what we modeled in the Background section of this lab: when the device switches on, it is operating just as if a switch shorts out the drain and source terminals. The capacitor then discharges through the inductor and the low on-state resistance of the device. Evidently the on-state resistance satisfies the condition for an under-damped (ringing) response. The leading edge of the output waveform is in the opposite extreme: the drain resistor is large enough so that the output response is over-damped.

How can we clean up the response so that the output waveform looks like a nice square wave? The fastest rise/fall times will occur when the resistances in the circuit are at the condition for critical damping:

□ First, replace the drain resistor with one of a value required to achieve critical damping on the leading edge of the waveform. Then tinker with the 3.3kΩ resistor in the gate bias network to increase the on-state resistance of the device to eliminate the ringing. Record your output waveforms with this "optimized" circuit.

Clearly this is another case where the nature of the load circuit has a strong effect on the design and operation of the entire circuit.

Inductive Spiking and Diode Clamp

Inductive loads can also lead to significant voltage spikes in some switching circuits. Consider the MOSFET circuit shown in Figure 4-8. Here the inductor has replaced the drain resistor, so to limit the current that flows in the transistor in the "on" state, we are using a

more robust biasing scheme with a source resistance (you may recall that this technique reduces the variation in drain current that may result from threshold voltage variations from device to device, and thus is a safer way to bias the circuit when there is no drain resistance to bail us out). With the source resistor shown, the drain current should be around 100-150mA in the on-state. It is probably easier to appreciate how this circuit behaves if we build it first:

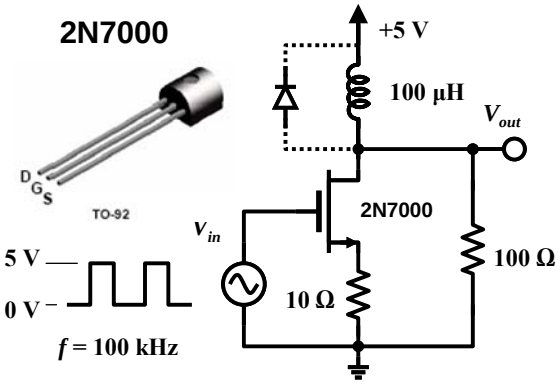

Figure 4-8 – Circuit for demonstrating inductive spiking and the use of diode clamps.

□ Build the circuit in Figure 4-8 using your 2N7000. Leave out the diode clamp in this first step. Adjust the frequency of the input signal to 100kHz, and record your waveforms.

Try to understand what is happening before you go any further. The large positive spike in the output voltage occurs when the transistor switches off. Remember, in an inductor the current can not change instantaneously, so when the transistor turns off, all the current that was flowing in the inductor must now divert through the 100Ω load resistor.

□ Demonstrate this last point by replacing the 100Ω load resistance with a 220Ω resistor. What is the peak voltage in this case?

□ Now add in the diode clamp (you can use a 1N4005 or a 1N4148 for this purpose). How does the output voltage change?

Depending on the circuit, such large voltage spikes may be wanted or unwanted. In the next section we will discuss a circuit that exploits these spikes, but often they are undesirable, and place a terrific stress on the switching device, so the diode clamp is a nice trick to prevent the device from being destroyed by such excessive voltage.

Motor Driver Circuit

Often the inductance is not an intentional part of the circuit but rather a consequence of the kind of load that is being switched on and off. Motors and relays are examples of devices that are inductive. The simple motor-driver circuit shown in Figure 4-9 is thus potentially similar in behavior to the inductive circuit we just built in Figure 4-8.

We call this circuit a "driver" because motors and relays often require a large amount of current, and this current is forced or "driven" through the load by the transistor stage. These are also sometimes called "current boosters", since they allow a high-current load to be driven by a low-current source. Thus the first step in making one of these stages is choosing a transistor that can handle the current that is required by the motor.

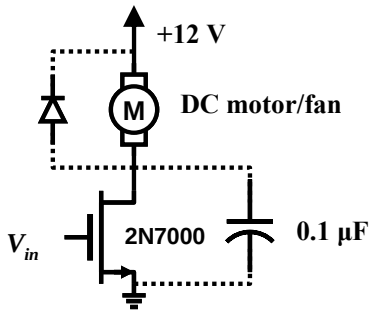

Figure 4-9 – Driver for simple DC motor.

Fortunately the little DC fan in your lab kit requires a modest ~100mA, so the 2N7000 is a fine choice.

Notice that we have eliminated the source resistance here; the motor itself is designed to be operated directly from a 12V supply and draw its rated current, so we need not worry about setting the gate bias for a particular current level here. All we need to do is drive the transistor hard so that its on-state resistance is small compared with the equivalent resistance of the motor.

- □ Build the circuit in Figure 4-9. Note the +12V supply. You can insert jumper wires into the little connector on the fan leads to hook up to your protoboard. You will not need the diode clamp here, and leave out the capacitor for now. Apply a +5V DC bias to the gate to turn on the fan.
- □ Now make the input signal a 100Hz 0-5V square wave. The fan should slow down noticeably compared to the previous step. Observe the drain voltage waveform on the oscilloscope. If there is evidence of ringing in the output, see if you can quench this by adding the capacitor as shown.

The fact that we can change the speed of the motor by varying the "on"-time of the input waveform is the basis of many motor speed controllers, and we will explore this more careful in a later lab. Note that other motors or fans may be significantly more inductive than this one and hence may require a diode clamp to avoid inductive spiking.

4.3 DC-DC "Boost" Converter

We mentioned that the voltage spikes observed in the circuit of Figure 4-8 may in fact be desirable in some cases. One example is the DC-DC boost converter, which is a circuit that can create large DC voltage from a smaller one with very high efficiency. The basic idea is to combine the inductive spike generator with a rectifier circuit, as shown in Figure 4-10. Whenever the drain voltage spikes up, the diode is forward biased and current will flow to charge up the big storage capacitor. When the drain voltage subsequently drops below the capacitor voltage, the diode is reverse biased and the output voltage stays constant. Just as in the power supply from Lab #2, the output capacitor must be sized appropriately to minimize the droop relating to current flow in the load. We will just use a small capacitor here and hence the circuit will not be able to source much output current.

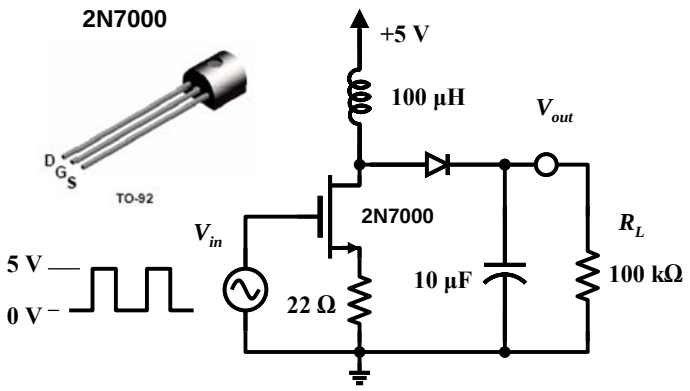

Figure 4-10 – DC-DC Boost converter

- □ Build the circuit in Figure 4-10 Note the +5V supply. You can use a 1N4005 or a 1N4148 for the rectifier diode. Start with a load resistance of 100kΩ and a switching frequency of 10kHz. What DC output can you obtain?
- □ Increase the frequency to 50kHz and measure the output voltage. Can you understand why it changed? One advantage we have here is that we can control the time period between the peaks of the signal going into the rectifier; in the power supply lab, we were stuck with a 60Hz source.
- □ Now decrease the load resistance to 10kΩ and measure the output voltage.

Clearly what is needed here is some active regulation to keep the output voltage constant when the load impedance varies, not to mention a larger output capacitance. There are some simple ways to implement the active regulation, and indeed there are a number of other interesting design considerations for DC-DC boost converters that you can read about if you are interested, but our goal here is really just to illustrate the concept, so the circuit shown here is not optimal in any sense. With more careful design, boost converters can drive a much larger output current at very high conversion efficiency (very little wasted power).

Note that the DC-DC converter requires a square-wave generator to drive it. Ordinarily this square-wave generator is part of the circuit and also powered by the +5V supply, such that the circuit is completely self-contained. We will discuss the design of oscillators in the next lab.

Congratulations!
You have now completed Lab 4

