UNIVERSITY OF CALIFORNIA, SANTA BARBARA Dept. of Electrical and Computer Engineering

ECE124A VLSI Principles

Homework #1 Review of Digital Design

Due Date: 10/05/2011 Friday by 5:00pm

Problem 1 Binary and 2-Complement Number

(A) Convert $(21)_{10}$ and $(26)_{10}$ into Binary

(B) Convert $(-21)_{10}$ and $(-26)_{10}$ into 2-complement number. Suppose each number has 8 digits and the highest digit is sign digit.

(C) Calculate26+(-21) and 21+(-26) using 2-complement numbers. Show your process. And explain the reason why we use 2-complement number in digital systems.

Problem2 Boolean algebra and Simplification

(A) Use algebraic manipulation to simplification $F = \overline{AB + \overline{C}} + A\overline{C} + B$

(B) Use algebraic manipulation to convert the following equation to sum-of-product and product-of-sum forms: $X\left(\overline{Y} + \overline{Z}\right) + YZW + \overline{\overline{Y}\,\overline{Z} + Z} + X\overline{Y}\,\overline{W}$

Hint: don't forget consensus.

(C) Make use of a Karnaugh Map to simplify:

$$F = \overline{A}\overline{B}C\overline{D} + A\overline{B}C\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}B\overline{C}D + \overline{A}BCD$$
$$d = \overline{A}\overline{B}CD + A\overline{B}CD + AB\overline{C}D + ABCD$$

Note that d corresponds to the don't cares. Choose the values of the don't cares to minimize the logic function. Be sure to show the values of the d's you choose.

Problem 3 Implement Boolean functions

(A) Implement the boolean expression below in a complementary CMOS gate

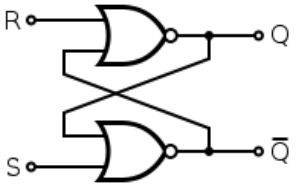
$$X = \overline{(A+B)(CD+EF)+G}$$

(B) Realize the following 4-input switching function using an 8-1 multiplexer:

$$F(A,B,C,D) = ABC + AD + AC$$

Hint: Make a truth table. Use D to implement the result F. Connect A, B, C to MUX address lines.

Problem 4 Sequential Circuit



(A) What is this? What is the Input/Output properties?

(B) If input is changing from (0,0) to (1,1), what will happen?

(C) How to use it to implement a D-latch with Enable signal?

(D) How to use two of the latches in (C) to implement an edge-triggered D-Flip-Flop?

(E) Explain setup time and hold time using a time diagram of D-Flip-Flop.

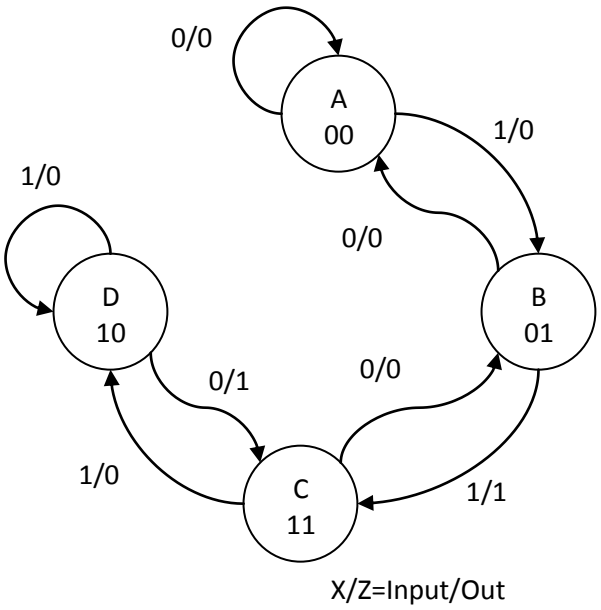
Problem 5 Finite State Machine

Consider the following state-transition graph which is to be implemented as a clocked, synchronous sequential circuit. If state d is the reset state and the states are encoded as State a = 00, State b = 01, State c =11, and State d = 10:

(A) Construct a state transition table for the machine in terms of input X and present-state (Y1 Y2) for output Z and next-state (Y1+ Y2+).

(B) Use Karnaugh maps to obtain the reduced next-state and output equations for the machine. Show your K-maps.

(C) Use the reduced set of equations to obtain a circuit diagram for an implementation of the machine. Use the minimum number of logic gates (AND, OR, NAND, NOR, XOR, XNOR, or inverters) and positive-edge-triggered JK flip flops.



Problem 6

(A) Write half page of review for the article listed below. The article can be found in the "Lecture Notes and Reference" section of the course webpage.
G. E. Moore, "Cramming more components onto integrated circuits," in Electronics, 38(8):114 -- 117, April 1965.

Also answer the following questions based on the paper:

(B) Why is integrated electronics better than "conventional" electronics?

(C) According to G. Moore, integration will not change linear systems as radically as digital systems. Explain.

(D) Search the Web for transistor counts of Intel and AMD's more recent microprocessors. Make a graph of transistor count vs. year of introduction from their Processors in 1990 to the present on a semilog scale. How many months pass between doubling of transistor counts?